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A study on dc-dc resonant switched-capacitor converters for LED driving and one application as a VLC transmitter

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Vinícius Moraes de Albuquerque

A Study on dc-dc Resonant Switched-Capacitor Converters for LED Driving and One Application as a VLC Transmitter

Dissertação apresentada ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Juiz de Fora como requisito parcial à obtenção do título de Mestre em Engenharia Elétrica. Área de concentração: Sistemas Eletrônicos.

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ABSTRACT

This work presents a family of Resonant Switched Capacitor (RSC) dc-dc converters operating as both high efficiency power converter and fast-response data transmitter for Visible Light Communications (VLC) applications. By operating under soft-switching, the topologies allow for higher switching frequency and higher slew rate, so that the VLC functionality can be embedded into the power stage without an auxiliary switch, which it is a major efficiency bottleneck for higher transmission rates due to its inherent hard-switching operation. This justify new efforts in enabling Pulse-Based Transmission (PBT) without this additional switch. Seven fast-response resonant converters are presented in this work, implemented with a proposed Switched Capacitor Cell and inspired on classic DC-DC topologies (Buck, Boost, Buck-Boost, Flyback, Cuk, SEPIC and Zeta). A $10\,W$ prototype was built to demonstrate such feasibility, operating at a switching frequency of $500\,kHz$, resulting in nominal efficiency of 85% during data transmission under VPPM scheme, achieving up to $100\,kpbs$ for various brightness levels, over a distance up to $1\,m$. Given the switching frequency conditions, this prototype is realized using GaN-FETs and Schottky diodes.

Keywords: Resonant Switched Capacitor. Dc-dc Converters. Visible Light Communication.

RESUMO

Este trabalho apresenta uma família de conversores cc-cc Ressonantes a Capacitor Comutado (RSC, do inglês *Resonant Switched Capacitor*) operando como conversor de potência de alta eficiência e transmissor de dados de rápida resposta para aplicações em Comunicação por Luz Visível (VLC, do inglês *Visible Light Transmission*). Ao operar sob comutação suave, as topologias permitem alta frequência de comutação e alta velocidade de resposta, tal que a funcionalidade VLC possa ser inserida no estágio de potência sem o requerimento de um interruptor semicondutor adicional, que contribui para limitar a eficiência para altas taxas de transmissões devido à sua inerente operação em comutação forçada. Tal característica justifica esforços que possibilitam Transmissões Por Pulso (PBT, do inglês *Pulse-Based Transmission*) que excluam a necessidade de tal semicondutor adicional. Sete conversores ressonantes de alta velocidade de resposta são apresentados neste trabalho, implementados com uma Célula de Capacitor Comutado e inspirados nas clássicas topologias CC-CC (Buck, Boost, Buck-Boost, Flyback, Cuk, SEPIC e Zeta). Um protótipo de $10\,W$ foi construído para demonstrar a capacidade de tal conversor, operando com frequência de comutação de $500\,kHz$, resultando em uma eficiência nominal de $85\,\%$ durante transmissões de dados sobre modulação VPPM, atingindo até $100\,kbps$ para vários níveis de brilho e em distâncias de até $1\,m$. Devido às condições de frequência de operação, a realização do protótipo se dá por transistores GaN-FETs e diodos Schottky.

Palabras-chave: Capacitor Comutado Ressonante . Conversores cc-cc. Comunicação por Luz Visível.

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SUMMARY

1 INTRODUCTION

The methods of light production and control had always evolved alongside human development, as both cause and effect of it. Not occasionally, these methods can be, in general terms, divided historically accordingly to its physical categories: man-made light production was limited within the effect of incandescence prior to the control of electricity around the 19th century. Electricity, however, was as much of a game changer for lighting as it was for everything else. Not only it allowed for incandescence to be produced through electric current, but also allowed for the effects of gas-discharge, (and far later, electroluminescence) to become viable for light production in scale as well.

These effects are fundamentally different in the manner that light is produced. While incandescence produces the photons through heat, and electrical lamps made use of electric currents as heat source, the gas-discharge method uses the electric current directly to collide electrons into neutral gases and vaporized metals forming ions, which proceeds to create photons when returning to their previous state. The major noticeable difference between such methods are that while the spectrum of the emitted light through incandescence is primarily dependent on the temperature of the heated object, the emitted light spectrum through gas-discharge depends on the gas mixture inside the bulb or tube. This allowed for a better light performance, with emissions being widespread throughout the light spectrum.

Structurally, however, electrical incandescent and gas-discharge lamps also had much in common. An incandescent lamp, despite presenting a solid wire as the heating element, demanded an enclosure of inert gaseous material/vacuum that stopped it from its complete burn out. At the same time, gas-discharge lamps presented the light source element itself in gaseous form, where several different elements could be used given the application. For instance, sodium lamps are commonly used for street lighting, variating in high- and low-pressure forms. In the meantime, mercury vapor can be used to create an ultraviolet light, which can be further transformed into the visible spectrum given proper coating at the lamp walls. Mercury-based lamps are used for both outdoor and street lighting through mercury-vapor lamps and in lower power for indoor application as fluorescent lamps.

The similarities between electrical lamps throughout the 20th century (incandescent and gas-discharge) is of great relevance for the understanding of the lighting revolution that is currently undergoing throughout the first decades of the 21st century. Mainly because this revolution is occurring through the so-called solid-state lighting (SSL), that uses properly-enriched semiconductors in order to achieve electroluminescence and thus, for the first time, excludes the necessity of a gaseous/vacuum chamber in electric lamps, giving place to the Light-Emmiting Diodes (LEDs) instead. Unlike previous light production

methods, electroluminescence uses electrons to produce light directly through differences in their energy levels, and thus the spectrum of the emitted light is defined by the bandgap of the excited material. This section introduces advancements in LEDs through its characteristics and advantages.

1.1 ON LED LIGHTING

Solid-state lamps present several advantages when compared to its traditional gaseous competitors. Its reduced use of toxic elements and heavy metals present technologies with much simpler waste disposal requirements, and its inherent solid-state components represents an easier containment for possible harmful elements. For instance, indoor lamps for domestic use have transitioned in previous years from incandescent lamps to fluorescent lamps, which contain a certain amount of mercury that can be easily dispersed in the environment. Such environmental concern is not present in LEDs.

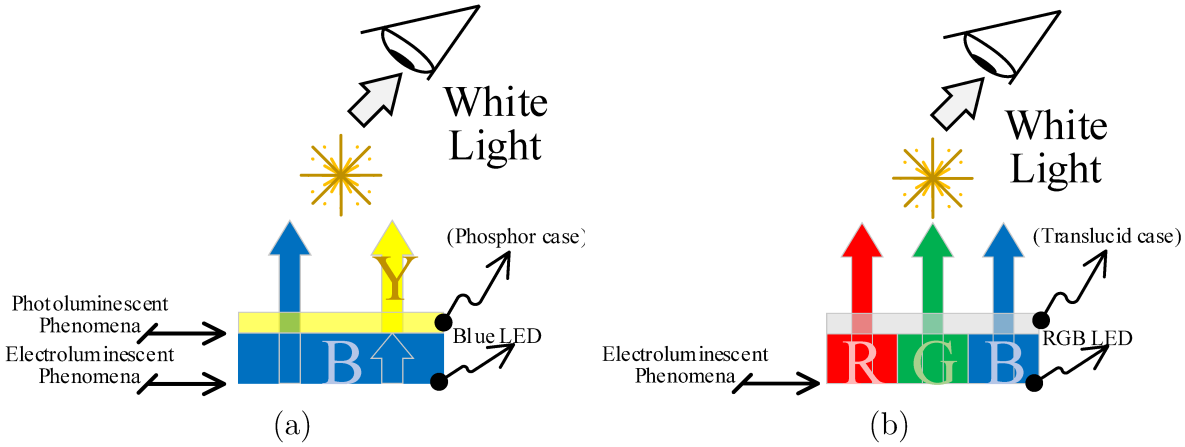
Another clear advantage presented by solid-state elements lies in its robustness, and therefore, lifespan. While gaseous chambers and filaments can be fragile (susceptible to break or burn-out), LEDs can present enough sturdiness to resist higher degrees of impact and physical stress. Added to its higher efficiency, the lamp's lifespan represents a much bigger return in the investment, increasing the viability of LEDs. Finally, such lamps present a very direct relation between current and radiance, meaning that light emitted is more easily predicted given the known applied electric power. This advantage is highlighted by increased possibilities in control, such as dimming.

This revolution, however, was only possible due to the advent of the blue LED, developed in 1990s. Until such time, LED lighting was not feasible not only by its power limitations but also due to the impossibility of synthesizing white light, which is essential for achieving good lighting performance.

Given the development of the blue LED, the synthesis of white light is present in LED lamps through two commercially available alternatives based on superposition of light rays. The first realization is by means of RGB lamps, in which the sum of red-green-blue emissions at the right ratio results in white light. The alternative uses phosphor-based devices, in which a blue LED is enclosed by a phosphor layer that, in contact with the blue light, goes through a photoluminescent phenomenon that re-emits part of such light as yellow. When added to the original blue light from the LED, the resulted emission is perceived as white. The contrast between white light production is summarized in its broader mechanisms in Figure 1.

The availability of white light as a product of solid-state electroluminescence completely changed the market of illumination and continues to do so, by challenging non-SSL technologies in financial viability owing to extended lifespan and higher efficiency. The Department of Energy of the United States predicts that LED technology will represent

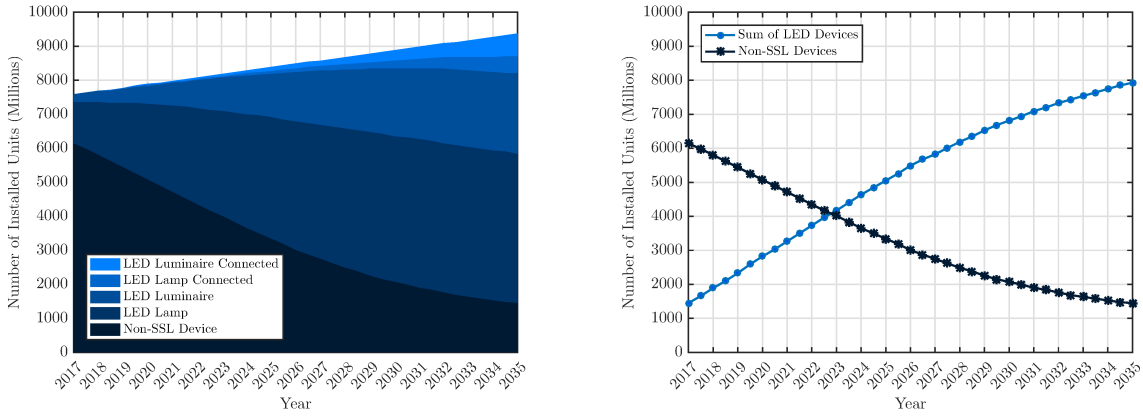
Figure 1 – LED differences for (a) blue LED with yellow phosphor coating and (b) RGB LED.



Source: Author (2020).

84% of lighting devices in 2035 (OFFICE OF ENERGY EFFICIENCY & RENEWABLE ENERGY, 2019). This is shown in the forecast of Figure 2, which presents a clear reduction of non-SSL devices over the next fifteen years. At the same time, the total sum of LED devices presents a steady growth, surpassing traditional technologies around 2023.

Figure 2 – Lighting technology (a) penetration forecast and (b) comparison.

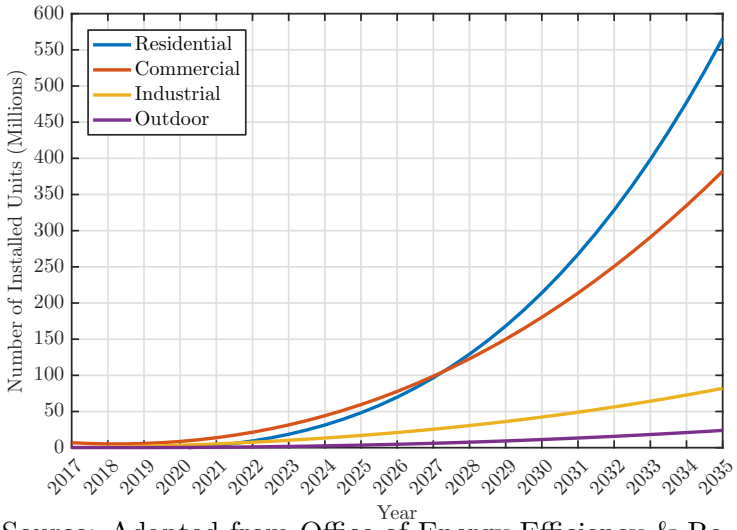


Source: Adapted from Office of Energy Efficiency & Renewable Energy (2019).

But even beyond lighting, the importance of SSL lies on its conformity with connectivity tendencies of the 21st century. Nowadays, technologies are expected to be increasingly connected and controllable, and LED technology allows for a more flexible user experience: LED lamps can not only have their light levels or turn-on/off hours programmed but also present the user the possibility of color control accordingly to people's comfort during various activities. For such reason, LEDs are truly appropriate for a connected era, and several smart LED bulbs are already for sale with Bluetooth or wi-fi connectivity that allows the user to control ambient light to a completely new extent. On

those lenses, The U.S. Department of Energy additionally predicts an exponential growth of connected LED devices in the next years for the different sectors lighting devices are applied, as shown in Figure 3.

Figure 3 – Connected LEDs forecast for different sectors.



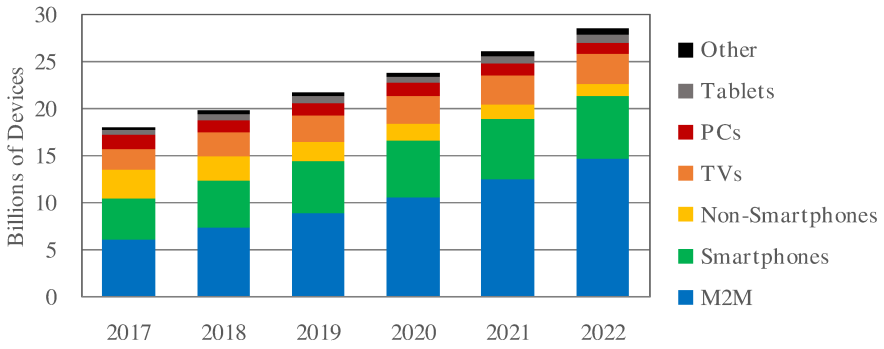
Source: Adapted from Office of Energy Efficiency & Renewable Energy (2019).

1.2 VISIBLE LIGHT COMMUNICATION SYSTEMS

Over the last years Light-Emitting Diode (LED) technology has been steadily increasing its market penetration by excelling over conventional lighting methods in energy consumption and lifespan, becoming a more viable alternative as production costs falls. More recently, such technology has not only become a major contender in financial viability but it is also presenting new applications for light emission. In these vanguard fields, applications in communications have been showing a promising prospect for widening wireless bandwidth, previously contained mostly in the Radio Frequency spectrum. By making use of this so far underused spectrum comprised in Visible Light for Communication (hence the common abbreviation VLC) a form of relief for the overgrowing congestion on RF spectrum as technologies become increasingly connected (CISCO SYSTEMS, 2019) is expected.

For instance, as shown in Figure 4, the overgrowing trend of connectivity is not limited by the number of connected devices but is also most prominent in some specific applications. Machine-to-machine (M2M) communication is a unique case that should represent over half (51 %) of all connected devices by 2022 (as oppose to 34 % in 2017). This kind of application, substantially expanded due to the use of Internet of Things (IoT), comprises several domestic and commercial technologies such as video surveillance and smart meters, required equipment to supply the overgrowing trend of connectivity.

Figure 4 – Global IP Traffic Forecast 2017-2022.



Source: Adapted from CISCO SYSTEMS (2019).

For a few reasons, the use of VLC becomes an attractive solution to supply this demand of overgrowing connectivity comprised mostly of devices in closed spaces transmitting over short distances. Firstly, because although VLC systems take severe setbacks with mobile equipment due to the requirement of constant light irradiation (which means variable distances and angles can induce a major reception problem), the tendency of the next demand of connectivity comes from stationary equipment with minimal to no mobility. Secondly, as the data is sent through irradiate light, physical opaque objects can be viewed as safety measures, stopping private data to spread to undesired locations. As a result, privacy breaches would demand physical contact with the irradiated light, requiring an undesired receptor to be placed inside buildings and thus adding a difficulty level to ill-intentioned data collectors.

Finally, the use of VLC takes advantage of installations already in place, as VLC transmitters can occupy with virtually no change the space of traditional lamps. As a matter in fact, even the luminous aspects of the current LED lamps can remain unchanged, with the required technological update being comprised solely on the electronic LED driver, thus not adding extra difficulty or cost to LED manufacturers.

These prospects are made possible by the fast dynamic response of LEDs, which can achieve up to 100's of MHz (MA; LAMPE; HRANILOVIC, 2013). This is an important feature to mention since white LEDs are commercially available in two forms, and although RGB LEDs maintain the natural high modulation bandwidth of the electroluminescent phenomena, phosphor-based LEDs present a slower response (between 2 and 3 MHz) owing to the photoluminescent phenomena used to generate yellow light. This limitation can be corrected by blue filtering at the receptor which can neglect the yellow light and allow only the fast-response blue light component to be detected. Along with appropriate equalization techniques, modulations from 25 MHz (MINH *et al.*, 2008) to 50 MHz (MINH *et al.*, 2009) can be achieved, enabling VLC with phosphor-based white LEDs (KARUNATILAKA *et al.*, 2015). This is an important step for VLC since these types of lamps are more prominent in the market, being preferred for lighting purposes in relation to the RGB

options because of their driving simplicity and lower cost.

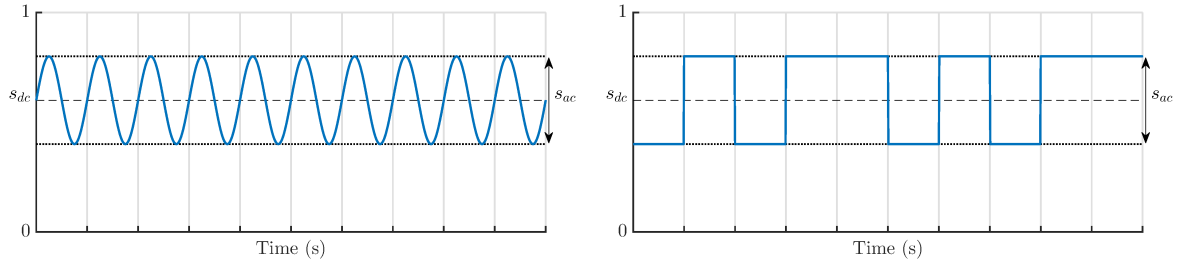
1.2.1 Light Modulations and Data Transfer

The workings of sending information through visible light are based on a modulation scheme that comprises a dc level, essential to perform the LED's dc bias and the illumination aspect of the lamp, and an ac level at a high frequency, imperceptible to the human eye, responsible for the information content (RODRÍGUEZ *et al.*, 2018a) (RODRÍGUEZ *et al.*, 2019). The light signal $s(t)$ can be as described by

$$s(t) = s_{dc} + s_{ac}(t). \tag{1.1}$$

The variables are illustrated in Figure 5

Figure 5 – Modulating variables illustrated in (a) sinusoidal and (b) pulsed signals.



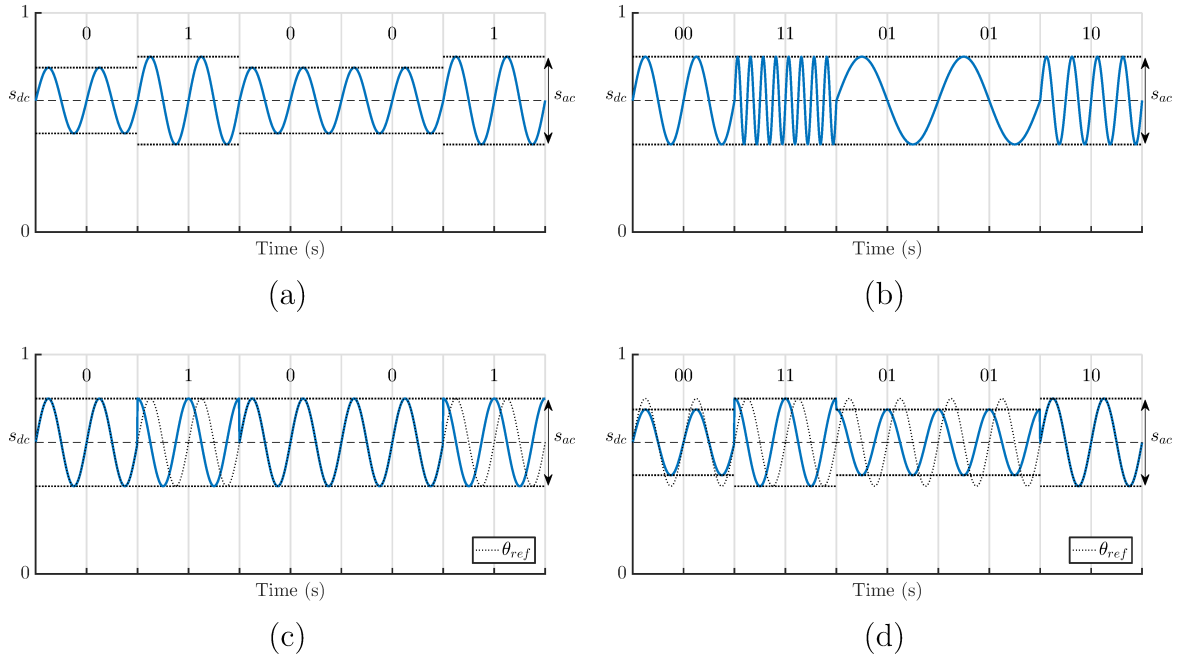
(a) (b)

Source: Author (2020).

The different possible modulations strategies are mainly comprised in single-carrier modulated transmission (SCMT), multiple-carrier modulated transmission (MCMT) and pulse-based transmission (PBT) (SEBASTIÁN *et al.*, 2018). SCMT contains modulations inspired by traditional methods of information transmission that use pure sine carrier waveform as the oscillating part of the signal, where the digital information (data bits) is coded by either amplitude (ASK), phase (PSK) or frequency (FSK) keying. Furthermore, simultaneously keying both amplitude and phase allows for the more complex Quadrature Amplitude Modulation (QAM) method (RODRÍGUEZ *et al.*, 2018a). These SCMT modulations are illustrated in Figure 6. As can be seen, frequency keying presents the advantage of allowing higher number of symbols due to the multiple values of frequency achievable. On the other hand, keying amplitude and phase presents more limitation that reduces the number of symbols. The QAM method increases the number os possible symbols by combining the amplitude and phase variations.

In addition to single-carrier options, MCMT conbines two or several carriers transmitting multiple sequences of bits instead of a single stream, presenting better response in transmission with multipaths, which would otherwise introduce a major signal attenuation problem (RODRÍGUEZ *et al.*, 2019) (RODRÍGUEZ *et al.*, 2018b).

Figure 6 – SCMT examples with (a) amplitude switching (ASK), (b) frequency switching (FSK), (c) phase switching (PSK) and (b) quadrature amplitude modulation (QAM).



Source: Author (2020).

For SCMT and MCMT transmissions, the sinusoidal waveform presents null average value by definition, demanding a mandatory sum of a dc level, usually provided by a slow-response dc-dc converter with a low-pass filter, while the alternating component is injected to the LEDs through a power amplifier (usually linear) that presents faster response but low efficiency. An alternative to the aforementioned scheme uses a single fast-response converter to provide both alternating and constant aspects of the current, a challenging task that demands more intricate converters (SEBASTIÁN *et al.*, 2018).

In contrast to carrier-based philosophies, the PBT method uses current pulses of sufficiently high frequency in order to transmit data. The PBT method can also be implemented by either a slow-response converter for the dc bias, with an amplifier adding the square waveform, or by a fast-response converter that performs both functions simultaneously. Once again, the former alternative requires fast-response converters that are usually complex and costly alternatives. Furthermore, the simplicity of the PBT modulation itself presents a trade-off in performance with more complex carrier-based methods, in both single carrier (such as PSK and QAM) and the aforementioned multi carrier that excels in multipath transmission and spectral efficiency (SEBASTIÁN *et al.*, 2018). Additionally, PBT also introduces the problem of high electrical stress at the LEDs due to continuous on-off switching, which introduce losses due to the continuous charge and discharge of the LED's intrinsic capacitor (TSIATMAS *et al.*, 2015) (DENG *et al.*, 2014).

Despite such problems, pulse-based transmission are still pursued in VLC studies

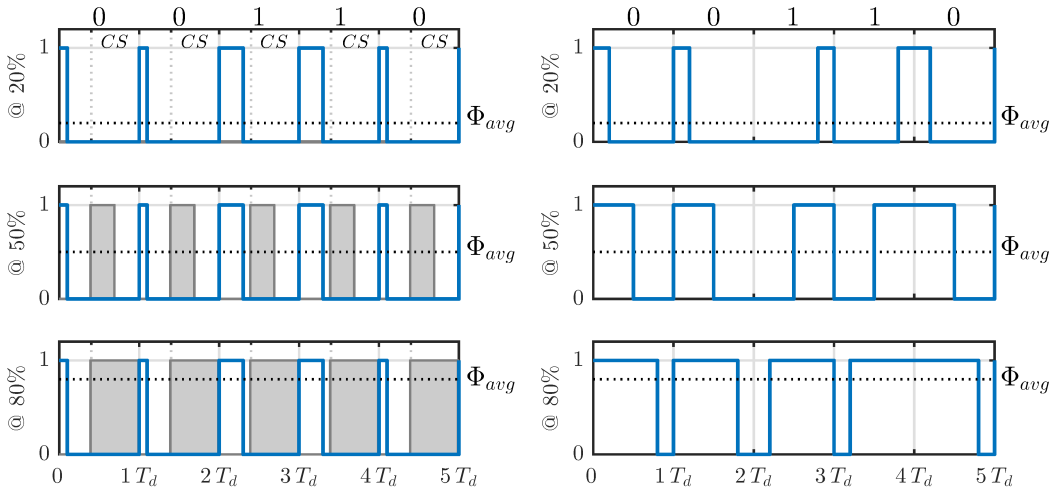
by opening a singular capacity of simplified light dimming through pulse width variation, which allows for direct light level modulation. Considering this addition of dimming to the VLC modulation, the IEEE standard 802.15.7 (IEEE STANDARDS, 2019) describes three modulation schemes to implement data transmission at different light levels, On-Off-Keying (OOK), Variable Pulse Position Modulation (VPPM) and Color-shift Keying (CSK), characterized as the physical layer (PHY) of the VLC system. Each of the three physical layers describes the application and expected data rate. While layers PHY I and II both allow for OOK and VPPM modulations and differentiate among them in frequency range, PHY III exclusively comprises CSK modulation for high data-rate applications. Since CSK requires RGB LEDs and multiple light detectors, it is beyond the scope of this work, which aims at high-brightness white LEDs (HB-LEDs) that are usually comprised by a single blue LED covered with a yellow phosphor layer. Therefore, such modulation will not be covered in this paper.

The IEEE standard 802.15.7 describes the On-Off-Keying modulation by the differentiation between bits '0' and '1' through the pulse-width, where a pulse with larger width represents logical high and a smaller width represents logical low. This modulation is the most straightforward yet it introduces the problem of different transmitted bits presenting different average values. In practice, this means that depending on the signal transmitted and the amounts of '0's and '1's the overall brightness of the LED can vary, and in order to achieve the precise required dimming, a compensation pulse with variable width will be required. Invariably, this modulation limits the transmitted data rate according to the data itself, which is not optimal.

The VPPM method, on the other hand, skips this problem by differentiating '0' and '1' bits not by pulse width, but by location of the pulse inside the signal period. This means that given a constant transmission rate at a given frequency, '0' is perceived by the receptor whenever the pulse is located at the beginning of the signal period, while the bit '1' is perceived by the receptor whenever the pulse is located at the end of the period. This method maintains the average of the signal constant each period despite whatever bit is being sent, maintaining the light output constant. Furthermore, light dimming can be achieved by altering the pulse width of the transmitting signal without affecting the bit transferred. As a result, the signal transmitted by the LED, and therefore the current it receives, can be described not as a sum of a dc level with an ac level as implied by (1.1), but rather, a specific kind of a pulse-width modulated (PWM) signal where the width of a pulse depends purely on the desired level of average light, while the location of the pulse inside the transmission period carries information.

The operations of these main PBT modulations are highlighted in Figure 7, which shows that the OOK strategy demands a compensation symbol (CS) for ensuring the desired lighting level. It is worth noting that the dc level does not need to be supplied by a separate converter. Rather, it is a consequence of the pulse width of the data signal.

Figure 7 – Example for PBT modulations for (a) OOK and (b) VPPM given three different brightness levels.



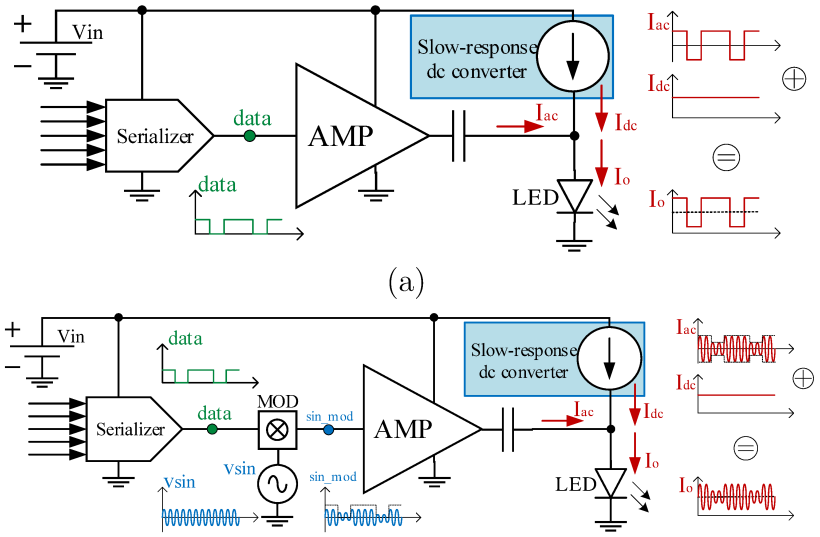
Source: Author (2020).

1.3 VLC CONVERTERS

Once an additional dc level is not required in the modulations proposed by IEEE standard 802.15.7, the operation can be summarized by the LED turning on and completely off at a rate proportional to the data transmission, which greatly simplifies the transmitter topologies. For instance, SEBASTIÁN *et al.* (2018) presents a thorough and comprehensive review of converters for the main modulation modes that require a dc level (PBT or SCMT), divided between multiple strategies of LED current synthesis. Mainly, the two more common strategies are discussed with examples: a) a superposition scheme involving a power converter for the LED DC bias with an added amplifier for the data capabilities and b) direct synthesis, a single-converter strategy involving fast-response power converters.

The general solutions offered through the superposition scheme are illustrated on Figure 8 for both PBT and SCMT transmissions. The main advantage of this solution lies in the union of well-established circuits, known to work well. As a result, the slow-response converter will process energy at the highest possible efficiency available, while the fast-response linear amplifier will add the low-power modulation signal, albeit at a much lower efficiency. A capacitor at the end of such amplifier illustrates the exclusion of any dc level, assuring that the slow-response power converter will be solely responsible for the illumination feature without interference from the modulation circuit. MCMT transmission can be achieved by summing the result of different modulators+amplifiers, thus adding multiple sinusoidal signals to the modulation.

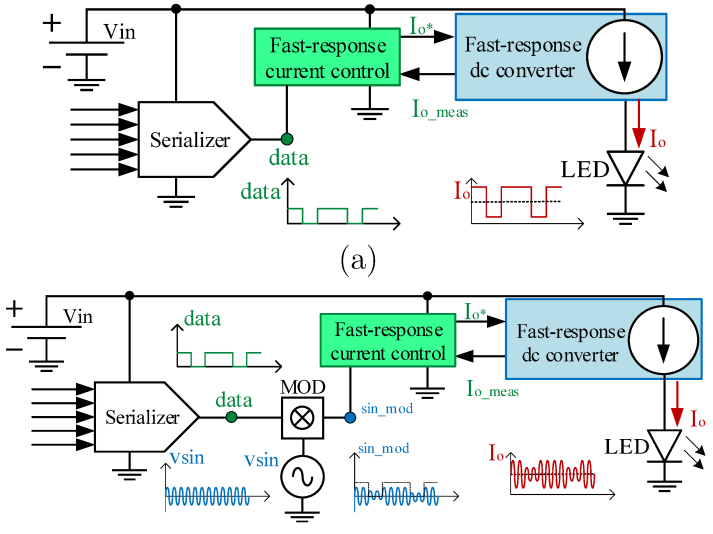
Figure 8 – Schematic illustration of the superposition strategy for VLC transmitters on (a) PBT and (b) SCMT modulations.



Source: Adapted from SEBASTIÁN *et al.* (2018).

On the other hand, the direct synthesis of current proposed in (SEBASTIÁN *et al.*, 2018) is achieved by fast-response power converters, capable of both biasing the LED and controlling its illumination capabilities as well as its data transmission through modulation. As a result, an amplification step is not requires, as shown in the schematic illustration of such strategy shown in Figure 9.

Figure 9 – Schematic illustration of the direct synthesis strategy for VLC transmitters on (a) PBT and (b) SCMT modulations.

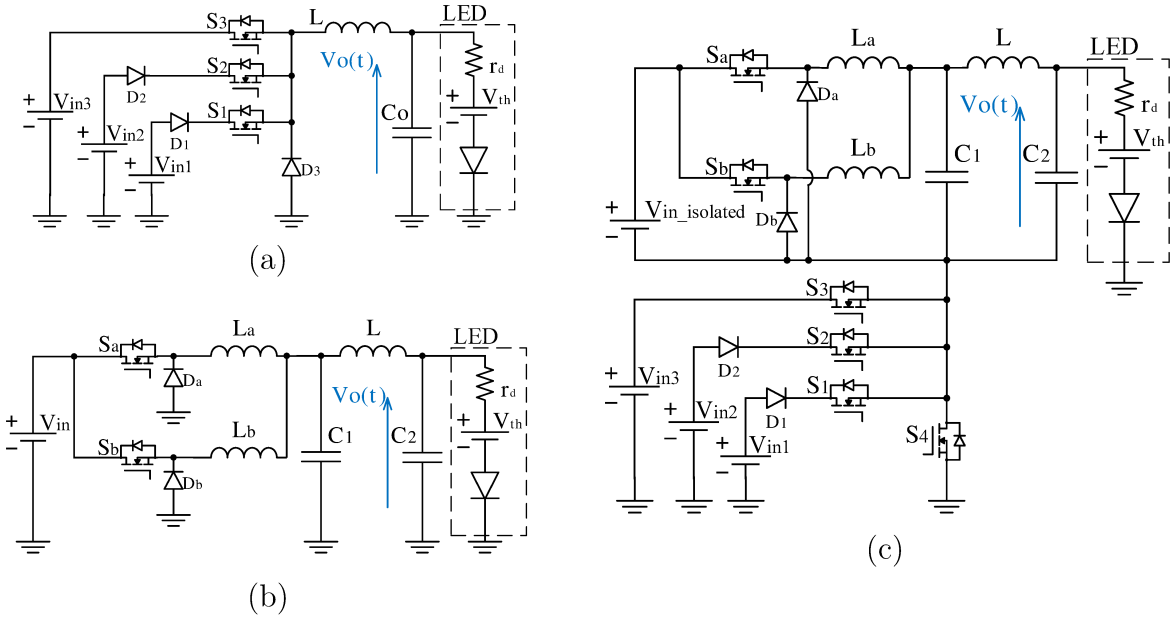


Source: Adapted from SEBASTIÁN *et al.* (2018).

These topologies, however, tends to be costly and complex, containing multiple active switches and, in some cases, multiple voltage sources, aside from a lower efficiency at power processing than the superposition alternative. As an example, (SEBASTIÁN *et al.*, 2018) suggests the use of converters proposed originally for envelope tracking (ET) and envelope elimination and restoration (EER) techniques, currently employed for RF transmission and capable of output voltage variations at the required rate.

On Figure 10 the three appropriate examples shown in SEBASTIÁN *et al.* (2018) for fast-response dc-dc converter are highlighted. In Figure 10a, a multiinput buck converter controls the output voltage through the duty cycles on the S_1, S_2 and S_3 switches. Similarly, in 10b, a two-phase buck converter has its output voltage controlled by the duty cycle of the switch S_a, while the switch S_b works synchronously. A Forth-order filter is added to the output. Finally, in Figure 10c shows a floating multiphase buck converter where the output voltage is controlled by the duty cycle on every switch through a conditional statement.

Figure 10 – Examples of fast-response converters capable of direct synthesis for VLC transmitters on (a) Multiinput buck converter, (b) Two-phase buck converter with a fourth-order filter and (c) Floating multiphase buck converter.

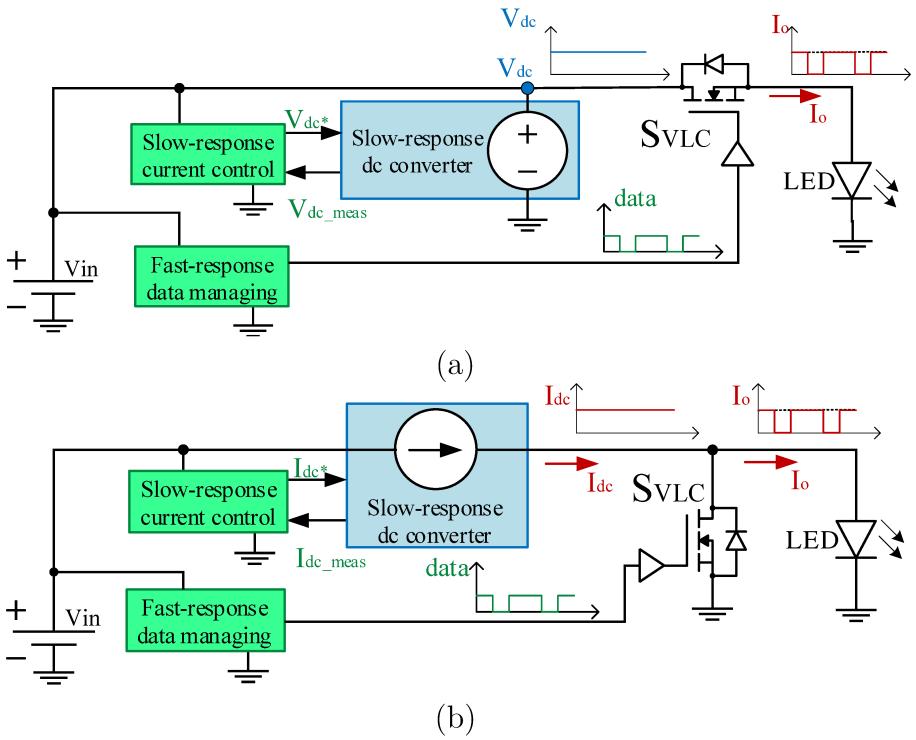


Source: Adapted from SEBASTIÁN *et al.* (2018).

As noted by Tsiatmas *et al.* (2015), however, VLC is only considered as a viable functionality by lighting engineers when little complexity is added to the driver when comparing to a purely lightning device, once separate communication and illumination solutions are well established and available at relative low cost. The aforementioned solutions of direct synthesis with a single-converter are not well suited through such lenses. A simple solution lies, however, in the use of the modulations proposed by IEEE standard 802.15.7. Once its modulation lies in a dual-state switching between a positive value

and zero, all it takes for a converter to produce such behaviour is to switch the LED load on and off. Thus, several solutions on literature have been proposing the use of well established power converters with high efficiency (responsible for the power processing) added to a semiconductor switch that modulates the energy with the fast response required for data transfer. The general scheme of such strategy is illustrated in Figure 11, with the auxiliary VLC switch being positioned in either series or parallel with the LED load.

Figure 11 – Schematic illustration of the on-off keying strategy for VLC transmitters with auxiliary VLC switch in (a) series and (b) parallel with the LED load.



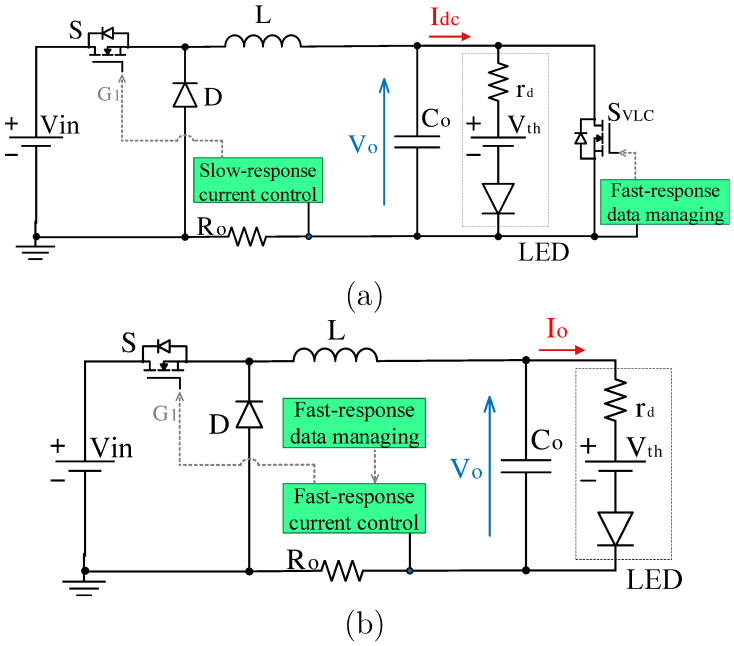
Source: Author (2020).

In (DENG *et al.*, 2014), a theoretical study compares the performance of a buck converter operating at on-off switching modulation scheme and at direct synthesis, where both dc level and data transfer capabilities are performed by a single converter without an additional amplifier, which the paper calls "slow modulation". The differentiation is illustrated on Figure 12. With the modelling of both cases complete in theoretical equations (alongside modelling of the optical channel and photodetector), a numerical comparison was performed in the plotted curves.

The slow modulated converter was shown to be more efficient due to the additional switching losses of the auxiliary VLC switch and due to the fast charge and discharge of the LED's intrinsic capacitance, both present at the on-off switching modulation scheme. Nevertheless, the on-off keying scheme presented better data transmission performance in most cases, with one exception where the "slow modulation" performed slightly better

under high pulsed amplitude. It is also important to note that the tests presented were performed under low transmission rates (10 $kbps$) specifically due to limitations on the slow modulation scheme, where PWM frequency is limited. Therefore, despite not being the most efficient option, the on-off keying modulation with the auxiliary VLC switch is the only of the studied alternative viable for higher data transmission rates.

Figure 12 – Schematic illustration of the buck converter as VLC transmitter in (a) on-off keying modulation and (b) slow modulation.

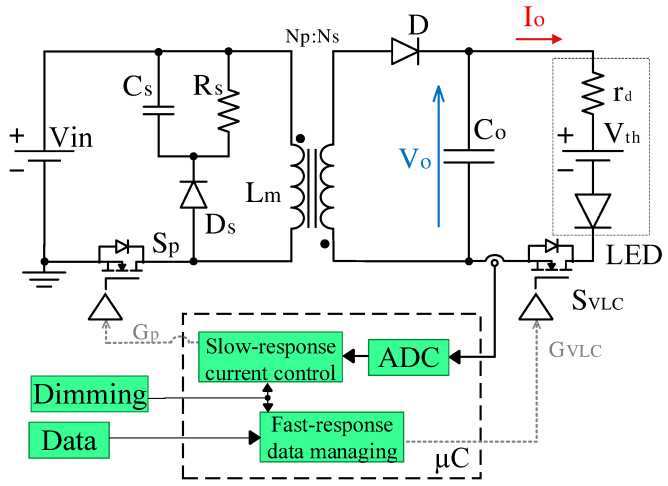


Source: Adapted from Deng *et al.* (2014).

Several other works have proposed the use of an additional active switch at the LED load for VLC transmission with adequate results. Effectively, this additional switch adapts lower-complexity, slow-response converters into single VLC-transmitters, taking advantage of the standardized PBT modulation techniques. As such, even ac-dc converters are benefited from such solution.

In (SALMENTO *et al.*, 2017), a dc-dc flyback converter as illustrated on Figure 13 is used as a preliminary study of a VLC transmitter with VPPM modulation. While the flyback converter is responsible for the power processing for a 20 W LED load, through a closed-loop current control. A microcontroller generates the switching signals for the converter switch at 35 kHz and for the auxiliary VLC switch, responsible for the data transfer, in series with the LED load ar 2.2 kHz. Thus, a transmission is achieved of 2.2 $kbps$. The efficiency is evaluated throughout a dimming window of 20% to 80%, and with data transfer the converter reaches efficiency levels between 85% and up to 88%. The added power loss caused by the on-off keying can be perceived since the same efficiency evaluation was performed with data transfer turned off. The efficiency result ranges from 86.2% to 89%.

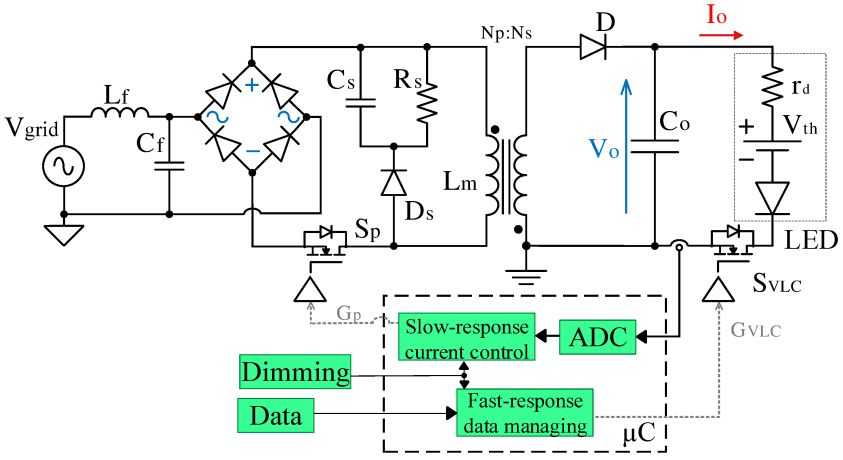
Figure 13 – Dual-purpose dc-dc Flyback converter as lighting device and VLC transmitter.



Source: Adapted from Salmento *et al.* (2017).

A subsequent study presented in (BRIER *et al.*, 2018) was made, detailing a flyback proposal though a $127\,V/220\,V$ ac prototype a shown in Figure 14. A design method is proposed and exemplified, proceeded by simulated and experimental analysis. Once again, the flyback converter supplies the power for the LED load at $63\,W$ at a switching frequency of $50\,kHz$. The data transfer is performed by an auxiliary VLC switch in series with the load, with switching frequency ranging from $1\,kHz$ up to $1\,MHz$. The power quality characteristics of the converter are evaluated, as well as the efficiency. The maximum achieved efficiency while transmitting data lies around 89% to 90% at $220\,V$. The efficiency is shown to increase with the brightness level, while the increase of transmission data rates decreases the efficiency due to the higher switching losses at the auxiliary VLC switch.

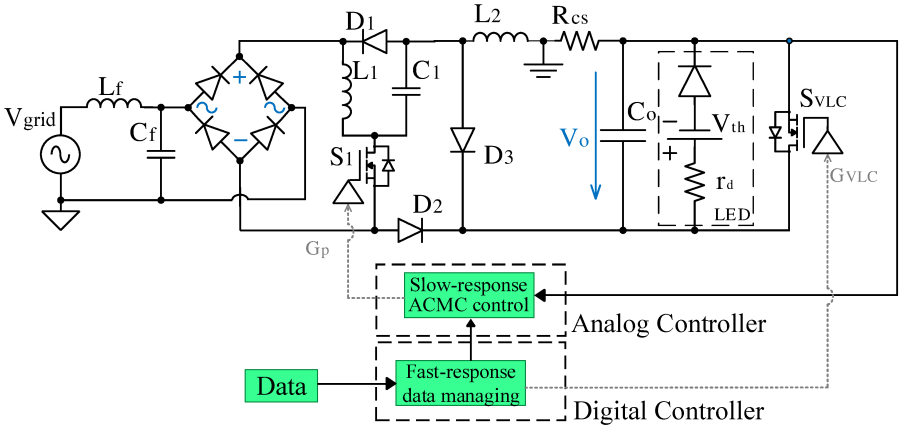
Figure 14 – Dual-purpose ac-dc Flyback converter as lighting device and VLC transmitter.



Source: Adapted from Brier *et al.* (2018).

A dual-purpose ac-dc LED driver with VLC capabilities through a auxiliary switch in parallel to the LED load is exemplified in (MODEPALLI; PARSA, 2017), where a $(S^2 - B^3)$ circuit is proposed as shown in 15. The buck portion of the circuit is designed to operate in continuous current mode (CCM), delivering an average current to the output loop, while the buck-boost portion is designed to operate in discontinuous current DCM mode (DCM) to assure power factor correction. The main converter switch operates at a $100\,kHz$ switching frequency, while the auxiliary VLC switch presents a $2\,MHz$ frequency, and thus, capable of transmission rates of up to $2\,Mbps$ at VPPM modulation. A prototype of around $6.8\,W$ achieved 85.2% efficiency without data transmission (no dimming) and up to around 80% while transmitting data at the highest brightness step possible.

Figure 15 – Dual-purpose ac-dc $(S^2 - B^3)$ converter as lighting device and VLC transmitter.

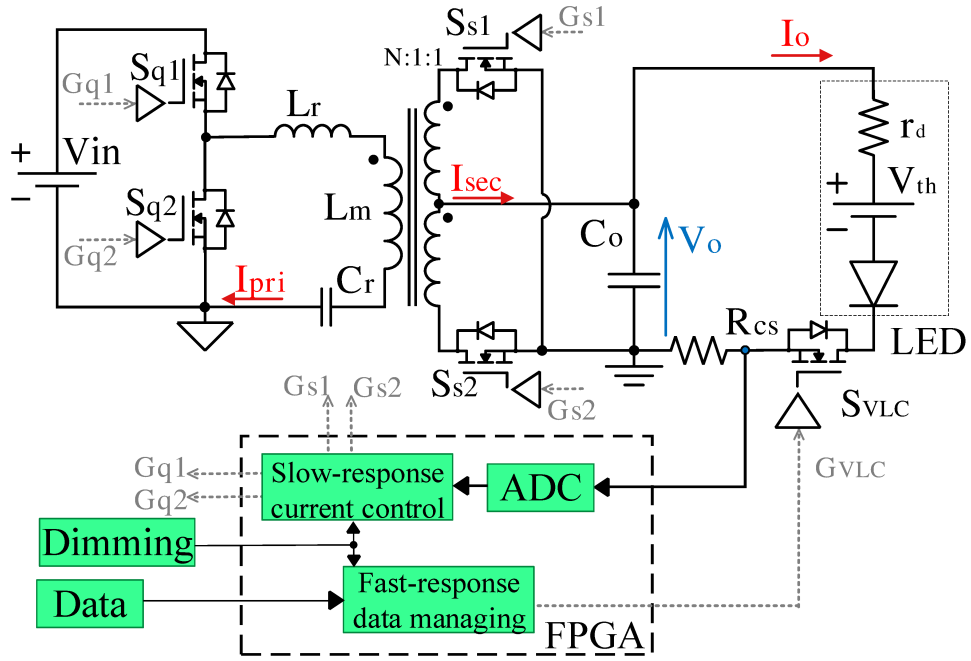


Source: Adapted from Modepalli e Parsa (2017).

The use of the auxiliary VLC switch simplifies the transmitter topology to such a degree that even resonant LLC converters were shown to employ it (ZHAO; XU; TRESCASES, 2014), as shown in Figure 16. The isolated dc-dc $400\,V$, $80\,W$ converter operates at $470\,kHz$, with the auxiliary VLC switch in series with the LED load operating a 1/10 of the switching frequency. Therefore, a transfer rate of around $47\,kbps$ is achieved with dimming steps from 10% to 90% for VPPM modulation. The measured efficiency ranges from 91% to 95%.

As can be seen, this application presents, however, significant drawbacks as the auxiliary VLC switch will, inevitably, operate in hard-switching mode in order to instantaneously stop the driver from providing current to the LEDs at a high frequency. The effect of this switch on efficiency is not only significant by itself, but will also escalate with data transmission rate. For instance, in (BRIER *et al.*, 2018) a converter operating at a switching frequency of $30\,kHz$ has its efficiency decreased from 90 % at lower data transmission rates (with the auxiliary switch at $50\,kHz$) to 81 % at higher data transmission rates (with the auxiliary switch reaching $1\,MHz$).

Figure 16 – Dual-purpose dc-dc resonant LLC converter converter as lighting device and VLC transmitter.



Source: Adapted from Zhao, Xu e Trescases (2014).

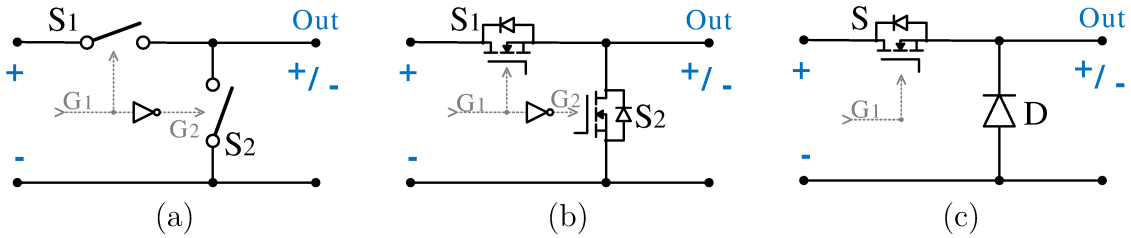
So, as can be seen, the auxiliary switch enables a new function to slow-response converters with a trade-off in efficiency, which is not ideal for an equipment meant to transfer data as well as efficiently process energy for illumination purposes.

1.4 PROPOSED SWITCHING CELL

The "Switching Cell" is the given name to a specific arrangement of two semiconductor switches in which at least one of them is an active component controlled by a control signal G_1 when the other can either be a passive or an active semiconductor switch operating in complementary mode ($G_2 = \overline{G_1}$). The arrangement, shown in Figure 17, allows the output to assume at a given instant the value of either the positive pole or the negative pole depending on the control signal at that instant. Due to that behavior, the "Switching Cell" can also be known as the "Switching Power-Pole" (MOHAN, 2011). The realization of this circuit is done using MOSFETs as active switches. An alternative solution is to use a diode in place of the second switch, simplifying the driving circuit to a single signal, albeit increasing conduction losses.

This cell and its variations in element polarity has been the base of many known dc-dc converters and allowed to the development of different circuit topologies that are still in study today for either DC applications or ac-dc converters. However, the classic topology of the "Switching Cell" presents significant drawbacks. For the case in point, data

Figure 17 – The traditional switching cell (a) idealized, in (b) bidirectional realization and in (c) unidirectional realization.



Source: Author (2020).

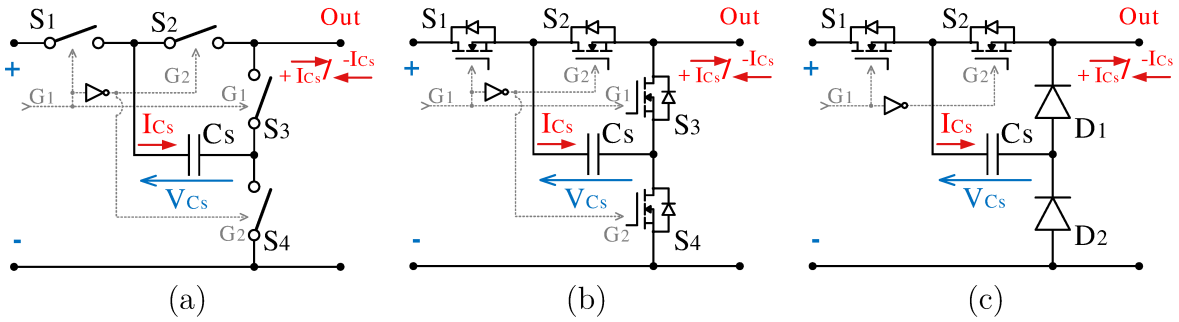
transfer through light modulation demands converters with at least medium switching frequencies (between 300 kHz and 3 MHz according to International Telecommunication Union (2016)), and up to the MHz range in order to produce significant data rates. This increase in switching frequency is limited, however, by the concomitant desire of higher efficiency for the converters, tied to lower costs of energy consumption. The inverse relation between these two requirements are given by the non-idealities of the semiconductors that causes a certain amount of energy dissipation as heat at every switching cycle.

Over the last years, a growing prospect in the technological development regarding frequency increase lies on the employment of GaN-based semiconductors, which present a faster response at higher efficiency compared to the previous technologies (DE PAULA *et al.*, 2017) (DUARTE *et al.*, 2016) (DUARTE *et al.*, 2017). However the problem of switching loss remains, indicating that new circuit topologies must be studied to minimize these effects, taking advantage of the trend of frequency increase.

In that scenario, a "switched capacitor cell" is proposed, composed by a capacitor and four switches as shown in Figure 18. The S_1 and S_3 switches are synchronously controlled with the same signal G_1, whereas the remaining S_2 and S_4 switches are activated complementary ($G_2 = \overline{G_1}$). The practical version of this circuit, using MOSFETs in place of the idealized active switches, is also displayed, as well as the alternate simplified version that uses passive diodes in place of the S_3 and S_4 switches. Once again, this realization with passive semiconductors simplifies the driving circuit by reducing the required signal outputs, but the diodes present increased conduction losses when compared to the MOSFETs.

The classic switching cell operates such that depending on the control signal and therefore the state of the active semiconductor, the output voltage is changed. While the switch is closed, the diode is reverse biased and the output signal is the same as the positive pole. On the other hand, an open switch allows the diode to enter conduction (given the presence of a magnetized inductor) and the output voltage is the same as the negative pole. By continuously switching the state of the semiconductor an average value of voltage can be synthesized based on the duty signal d of the control signal.

Figure 18 – The switched capacitor cell (a) idealized, in (b) bidirectional realization and in (c) unidirectional realization.



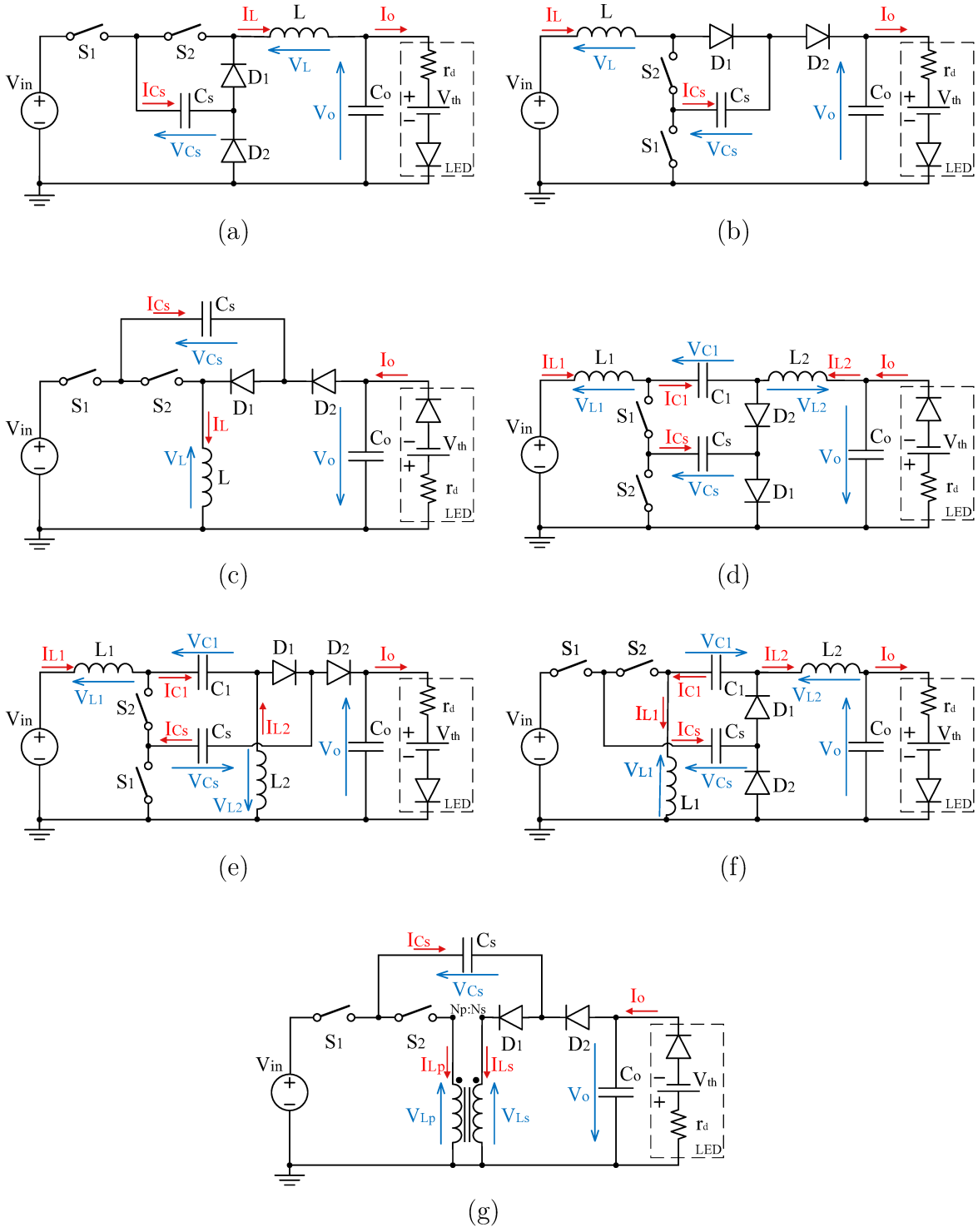
Source: Author (2020).

In opposition, the proposed switching cell does not changes the output voltage, but rather, the capacitor current. By closing the switch S_1 and maintaining S_2 open, the output current is the same as the capacitor current as defined by its positive current flow. On the opposite condition, with S_1 open and S_2 closed, the output current is the negative of the capacitor current accordingly to its assigned positive flow. The output current, however, does not change its direction flow during the switching state. It is the capacitor current itself that does, as the commutation is actually charging and discharging the capacitor every switching period. The amount of transferred energy is directly related to the amount of charges and discharges performed by the capacitor, which is then related to the switching frequency. The duty cycle of the control signal must remain constant at $d = 0.5$ once charging and discharging times of the capacitor are the same.

This characteristic of continuous charge and discharge of the capacitor gives the name for the proposed new power-pole circuit as the “Switched Capacitor Cell", allowing a revision of the classic dc-dc converters that operate with the lower-frequency “Switched Power Pole”. Using the switched capacitor cell with the magnetizing elements in the configurations presented on the six traditional dc-dc converter (Buck, boost, buck-boost, Ćuk, SEPIC and Zeta) results in resonant versions of such converters. This new resonant switched-capacitor (RSC) versions presents soft-switching when working in discontinuous-conduction mode (DCM), which enables high-frequency operation and therefore, low volume and higher efficiency in addition to the fast dynamic response.

In this work, the six classic dc-dc converters will be studied given their implementation with the simplified RSC cell (using two diodes in place of two switches) and DCM operation, which allows soft-switching. These topologies are shown in Figure 19. It is important to note that the RSC buck (FERREIRA *et al.*, 2017) and RSC boost (SHUAI *et al.*, 2010) topologies have been previously described in literature yet the thought process regarding their modeling will be reworked in this work in order to fit with the methodology presented and used for the additional topologies. Additionally, the CCM operation for the RSC buck converter has also been studied (NERES *et al.*, 2019).

Figure 19 – Resonant Switched-Capacitor converter family: (a) RSC buck, (b) RSC boost, (c) RSC buck-boost, (d) RSC Ćuk, (e) RSC SEPIC, (f) RSC Zeta and (g) RSC flyback.



Source: Author (2020).

1.5 CONTENT

Aiming in producing fast-response converters for VLC applications as alternative to the current method of additional switch, a new family of resonant switched-capacitor converters is proposed, based on the switched-capacitor cell and on the classic topologies of dc-dc converters. As these RSC converters (as well as the classic ones) can be divided in lower and higher order given the number of energy-storing elements, so they will be divided by their mathematical descriptions. Doing so, it will be possible to comprise rules and general step-by-step analysis mechanisms that can be used according to the order of the converter. Such rules are described in Chapter 2, and used to present extended analysis to the RSC buck converter and briefer analysis of the other converters. Detailed descriptions of the remaining converters are left for Appendix A.

In Chapter 3, a VLC design guideline will be shown, explicitly conditioning the design of RSC buck converter as a transmitter for such application as an example. In the same section, the overall set up of the experiment is described, including the receiver. Chapter 4 will discuss the results of the several measurements performed.

Finally, Chapter 5 will present conclusions over the achieved results.

1.6 PUBLICATION

The work performed during the Master's Degree discussed in this dissertation resulted in a journal publication on the same subject. Additionally, two other papers have been accepted for conference publication in different power electronic fields:

a) ALBUQUERQUE V. M. de, SOARES G. M., ALONSO J. M. and ALMEIDA P. S., A Simple Resonant Switched Capacitor LED Driver Employed as a Fast Pulse-Based Transmitter for VLC Applications, *In*: **IEEE Journal of Emerging and Selected Topics in Power Electronics**, 2020;

b) NASCIMENTO S. O., ALBUQUERQUE V. M.,RENDÓN M. A.,OLIVEIRA J. G. and ALMEIDA P. S., Modeling and Control of a Back-to-Back system for turboelectric propulsion, *In*: IEEE SOUTHERN POWER ELECTRONICS CONFERENCE, 5.; IEEE BRAZILIAN POWER ELECTRONICS CONFERENCE, 15., 2019, Santos, **Proceedings** [...]. Santos: IEEE, 2020. p. 1-6;

c) TORRES V. C. S, ALBUQUERQUE V. M., RENDÓN M. A., ALMEIDA P. S. and OLIVEIRA J. G., Interleaved Bidirectional dc-dc Converter for Application in Hybrid Propulsion System: Modeling and Control, *In*: IEEE SOUTHERN POWER ELECTRONICS CONFERENCE, 5.; IEEE BRAZILIAN POWER ELECTRONICS CONFERENCE, 15., 2019, Santos, **Proceedings** [...]. Santos: IEEE, 2020. p. 1-6.

2 MATHEMATICAL ANALYSIS ROUTINE FOR RSC DC-DC CONVERTERS AND BUCK RSC ANALYSIS EXAMPLE

The traditional DC-DC converters can be divided in two groups regarding the order of the converter, which is related to the amount of energy storing elements they posses. Each energy storing element is associated with a state in the converter analysis, and the number of states defines the order of the converter. For instance, the traditional buck, boost and buck-boost converters are second-order circuits, presenting one magnetizing element and an output capacitor. Ćuk, SEPIC and Zeta converters are fourth-order converter due to one additional magnetizing element and one input capacitor C_1.

On the same note, a similar division can be drawn to the analyzed RSC converters, where the switched capacitor present at the switched capacitor cell adds the order of each converter in one state. This division is useful as the analysis of the circuits in each group share many similarities, allowing general guidelines to be suggested.

2.1 LOWER-ORDER RSC CONVERTERS

The Lower-Order RSC converter are the analogous versions of the classic buck, boost, and buck-boost converters, with the latter having a traditionally isolated variant, the flyback converter, that can also be adapted in RSC form. These converters present a single magnetic component, and ZCS is achieved by operating in DCM mode. The switched capacitor C_s and the inductance L from the magnetic component form a resonant network, with its resonant angular frequency ω_o defined by

$$\omega_0 = \sqrt{\frac{1}{L\,C_s}}. \tag{2.1}$$

In order to simplify the analysis, the output node will be considered as constant-voltage. This assumption is drawn based on two main factors: a) the load will be considered an LED with negligible series resistance r_d, such that the output voltage remains constant at $V_o \approx V_{th}$ and b) the output capacitance C_o will be considered high enough in order to maintain the resonant frequency, with respect to the output capacitor C_o, at a low enough value such that it can be neglected in the resonant process. The static voltage gain G of the converter is then defined as $G = V_o/V_{in}$. At Chapter 4, however, the output capacitor's dynamics will be considered in order to calculate rise and fall times of the LED current considering PBT modulation.

The operation of each RSC converter can be divided into six basic stages, where only stages 1 and 4 contain simultaneously the switched capacitor C_s and inductor L, making them the resonant stages. Stages 2 and 5 are the free-wheeling stages, where two diodes are kept conducting due to the magnetized inductor. Stages 3 and 6 are zero energy stages, where the states of the circuit remain unchanged:

a) Charging of the switched capacitor C_s up until forward biasing of diode D_2;

b) Closed loop through diodes allow discharge of remnant inductor energy;

c) Off-time of null inductor current;

d) State change in both active switches, allowing discharge of switched capacitor C_s down to forward biasing diode D_1;

e) Closed loop through diodes allow discharge of remnant inductor energy;

f) Off-time of null inductor current.

Every stage begins and ends with the switched capacitor C_s either fully charged to a certain plateau voltage or fully discharged. Therefore, in order to begin the operational analysis, the initial conditions for the stages must be found and hence the voltages across the switched capacitor C_s while fully charged and discharged must be determined. It is then necessary to calculate the voltage at the switched capacitor capable of forward biasing the blocking diodes in stages 1 and 3 which results in the maximum and minimum voltages at the switched capacitor respectively.

Once the initial conditions are known, differential equations are found describing switched capacitor voltage V_{Cs} and inductor current I_L, being then simplified through direct and inverse Laplace Transforms. The results are time-domain equations describing the state of the circuit in each stage.

Given such equations, several variables of interest can be found, including the time duration of each stage and average values of inductor and output current, as well as output power. Such relations will allow the future design of the converter for required loads. Thus, the analysis of RSC converter of lower order follows the according sequence:

a) Analysis of the resonant capacitor voltage;

b) Analysis of each of the six operating stages;

c) Analysis of time delay between stages;

d) Analysis of average inductor current;

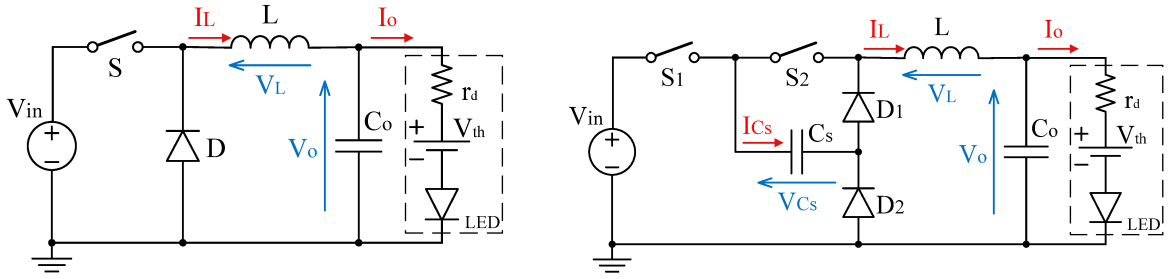
e) Analysis of average output current;

f) Analysis of output power.

2.2 RSC BUCK ANALYSIS

The RSC buck converter can be seen in Figure 20, where it is compared to the traditional buck converter. As can be seen, both are similar regarding the inductor position in relation to the switching cell, both at its respective output.

Figure 20 – Classic buck converter (a) and RSC buck converter (b).

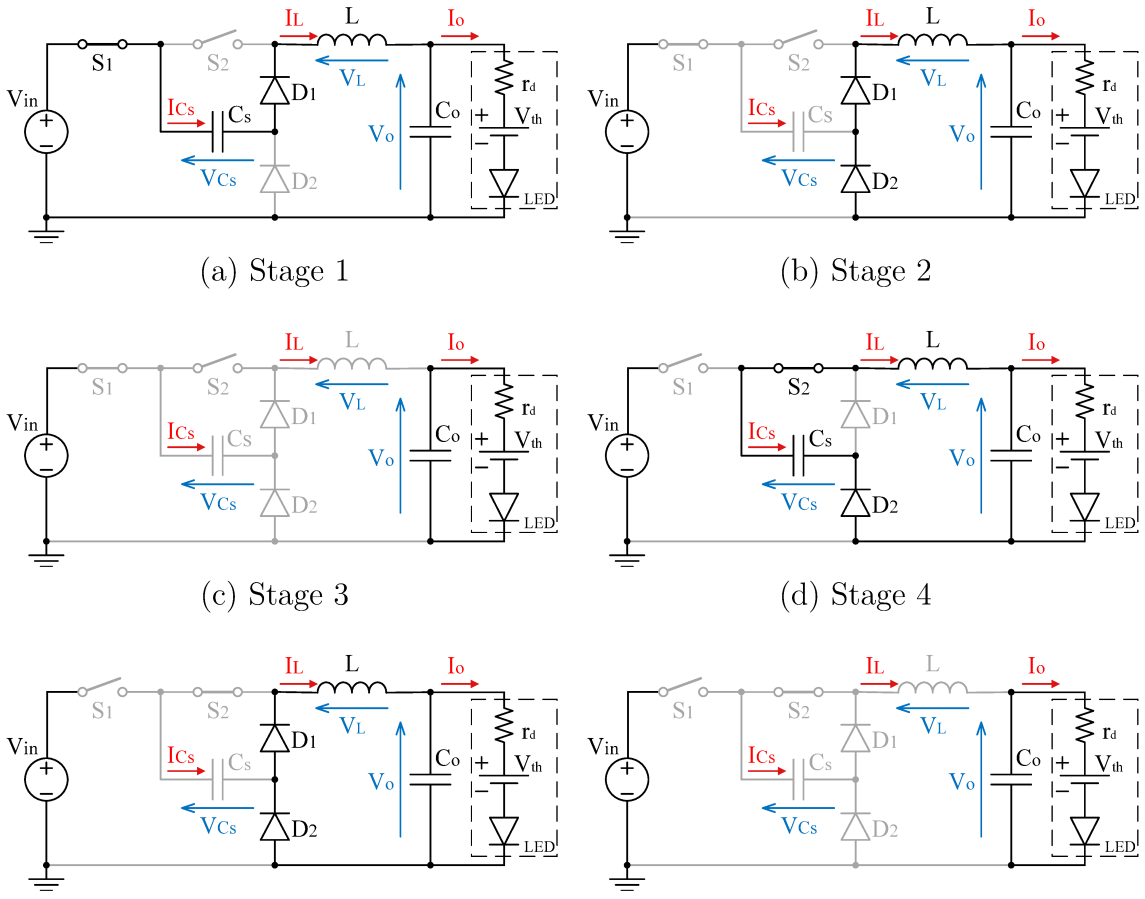


(a) (b)

Source: Author (2020).

The six distinct stages are highlighted in Figure 21.

Figure 21 – Stages of operation of the RSC buck converter.



(a) Stage 1 (b) Stage 2

(c) Stage 3 (d) Stage 4

(e) Stage 5 (f) Stage 6

Source: Author (2020).

2.2.1 Switched capacitor analysis

With the stages well-established it is possible to calculate the voltage at the switched capacitor capable of forward biasing the blocking diodes in stages 1 and 4, which results in the maximum and minimum voltages at the switched capacitor respectively. For the RSC buck converter this is achieved through the analysis of the $[V_{in} - S_1 - C_s - D_2]$ loop in Figure 22a and the $[C_s - D_1]$ loop in Figure 22d.

For the stage 1, the blocking diode is D_2, and its blocking voltage is described as

$$v_{D2}(t) = V_{in} - v_{Cs}(t). \tag{2.2}$$

Therefore, maximum voltage at the switched capacitor is $V_{Cs} = V_{in}$, where the blocking diode D_2 becomes forward-biased. In stage 4, the blocking diode is D_1, with a blocking voltage described by

$$v_{D1}(t) = v_{Cs}(t). \tag{2.3}$$

Thus, the switched capacitor can only discharge down to null voltage, not being to achieve negative values due to the forward bias of the previous blocking diode D_1. It is found that for the RSC buck converter, the charged and discharged conditions of the switched capacitor are given by

$$V_{Cs\,max} = V_{in}\ ;\ V_{Cs\,min} = 0. \tag{2.4}$$

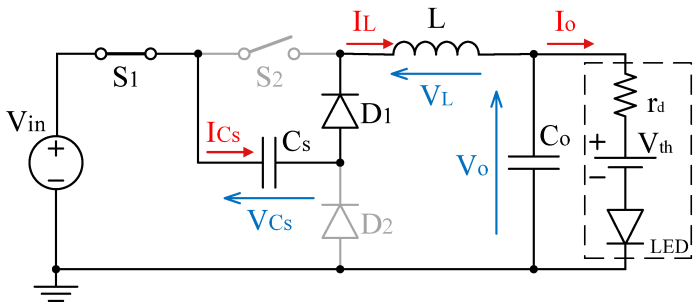
With the initial conditions of the described, the operational analysis of each of the states are drawn in the following.

2.2.2 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor through the path highlighted in Figure 22. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = 0 \\ i_L(t_0) = 0 \end{cases} \tag{2.5}$$

Figure 22 – Buck RSC: stage 1.



Source: Author (2020).

Through the loop and node equations, the current and voltages at the semiconductors are determined and summarized in Table 1.

Table 1 – Semiconductor Conditions for RSC buck: stage 1.

	State	Voltages	Currents
$\mathbf{S_1}$	Conducting	$v_{S1} = 0$	$i_{S1} = i_L(t)$
$\mathbf{S_2}$	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
$\mathbf{D_2}$	Blocking	$v_{D2} = V_{in} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described in (2.6) and (2.7).

Time Domain		Frequency Domain	
$V_{in} = v_{Cs}(t) + L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + s\,L\,I_L(s) + \frac{Vo}{s}$	(2.6)
$C_s\,\frac{d}{dt} v_{Cs}(t) = i_L$	$\xrightarrow{\mathcal{L}}$	$s\,C_s\,V_{Cs}(s) = I_L(s)$	(2.7)

Substituting the $I_L(s)$ equivalence given in (2.7) at (2.6) and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_{in} - V_o}{s}\,\frac{1}{C_s\,L\,s^2 + 1} = \frac{V_{in} - V_o}{s}\,\frac{\omega_0^2}{s^2 + \omega_0^2} \tag{2.8}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = (V_{in} - V_o)\,(1 - \cos(t\,\omega_0)) \tag{2.9}$$

On the other hand, isolating the inductor current from the (2.6) and (2.7) yields

$$I_L(s) = C_s\,(V_{in} - V_o)\,\frac{1}{C_s\,L\,s^2 + 1} = C_s\,(V_{in} - V_o)\,\frac{\omega_0^2}{s^2 + \omega_0^2} \tag{2.10}$$

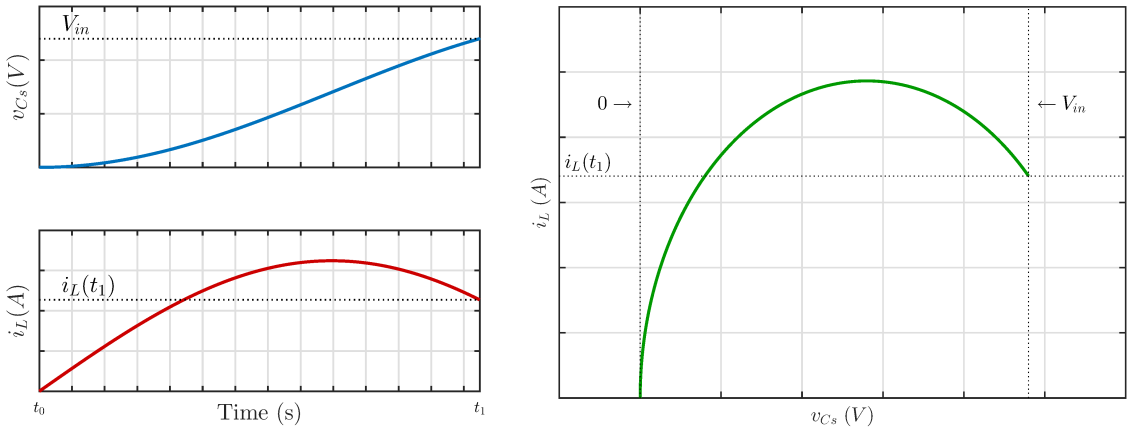
And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\,\omega_0\,(V_{in} - V_o)\,\sin(t\,\omega_0) \tag{2.11}$$

The resulted waveforms described are shown in Figure 23.

When the capacitor reaches sufficient voltage to forward bias the diode D_2 the remaining energy on the inductor forces a current through the passive semiconductors, by the closed path highlighted in Figure 24. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum

Figure 23 – Buck RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



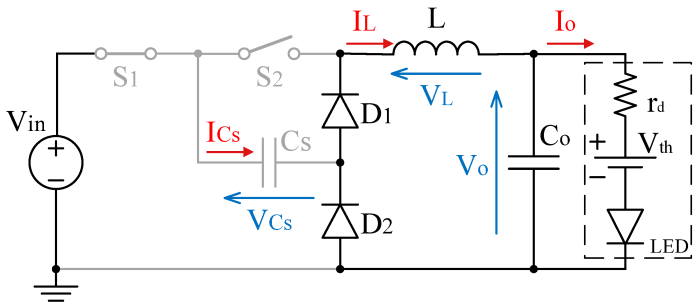
(a) (b)

Source: Author (2020).

value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_{in} \\ i_L(t_1) = I_{L\,(t1)} \end{cases} \tag{2.12}$$

Figure 24 – Buck RSC: stage 2.



Source: Author (2020).

The current and voltages at the semiconductors are summarized in Table 2.

Table 2 – Semiconductor Conditions for RSC buck: stage 2.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described as

Time Domain		**Frequency Domain**	
$L\,\frac{d}{dt}i_L(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L\,(s\,I_L(s) - I_{L(t1)}) = -\frac{V_o}{s}$	(2.13)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max} = V_{in} \tag{2.14}$$

The inductor behavior can be solved by isolating $I_L(s)$ from (2.13), which yields

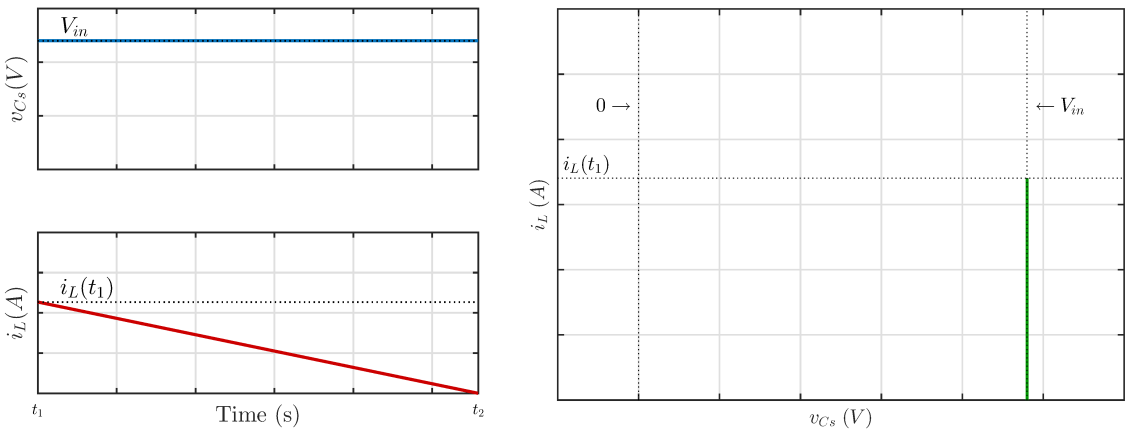
$$I_L(s) = \frac{I_{L(t1)}}{s} - \frac{V_o}{L\,s^2} \tag{2.15}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_L(t) = I_{L(t1)} - \frac{V_o}{L}\,t \tag{2.16}$$

The resulted waveforms described are shown in Figure 25.

Figure 25 – Buck RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



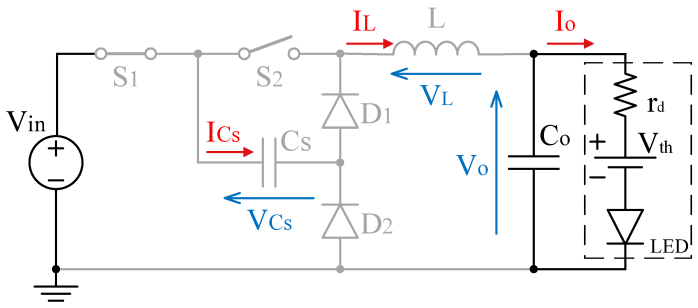
(a) (b)

Source: Author (2020).

This stage is characterized by the complete depletion of energy on the inductor. Given the required DCM operation, this study considers that the current on the inductors does reach zero while still on the first half of the switching period, resulting in the circuit shown in Figure 26. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_{in} \\ i_L(t_2) = 0 \end{cases} \tag{2.17}$$

Figure 26 – Buck RSC: stage 3.



Source: Author (2020).

Table 3 displays the current and voltages at each semiconductor for stage 3.

Table 3 – Semiconductor Conditions for RSC buck: stage 3.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = V_{in} - V_o$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t) - (V_{in} - V_o)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_{in} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage 3 both capacitor voltage and inductor current are constant and presenting the values of

$$v_{Cs}(t) = V_{Cs\,max} \tag{2.18}$$

and

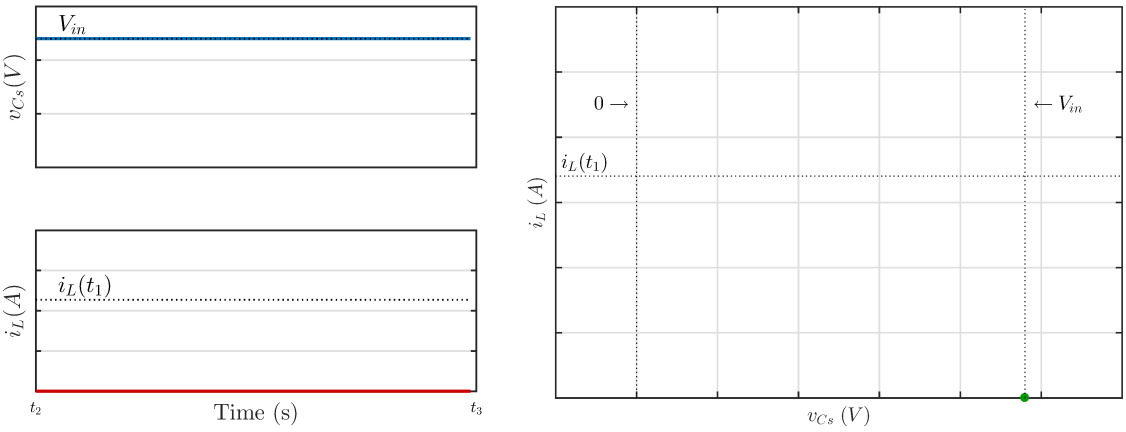
$$i_L(t) = 0. \tag{2.19}$$

The resulted waveforms described are shown in Figure 27.

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1 as shown in Figure 28. The switched capacitor is once again added to the active part of the circuit allowing its storage energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_{in} \\ i_L(t_3) = 0 \end{cases} \tag{2.20}$$

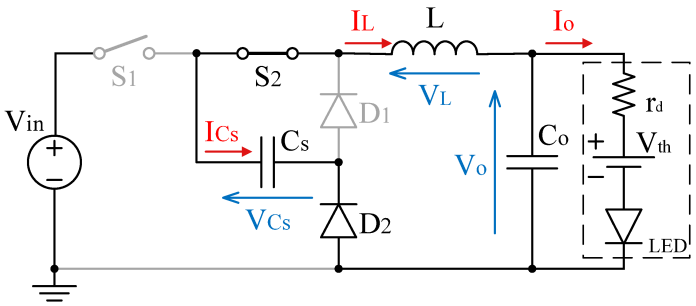
Figure 27 – Buck RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

Figure 28 – Buck RSC: stage 4.



Source: Author (2020).

The semiconductors currents and voltages for stage 4 are shown in Table 4.

Table 4 – Semiconductor Conditions for RSC buck: stage 4.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = i_L(t)$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The node and loop equations for this stage are described in (2.21) and (2.21).

Time Domain		Frequency Domain	
$v_{Cs}(t) = L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = s\,L\,I_L(s) + \frac{V_o}{s}$	(2.21)
$C_s\,\frac{d}{dt} v_{Cs}(t) = -i_L$	$\xrightarrow{\mathcal{L}}$	$C_s\,(s\,V_{Cs}(s) - V_{Cs\,max}) = -I_L(s)$	(2.22)

Using both equations and isolating the capacitor voltage yields

$$V_{Cs}(s) = V_{in}\,\frac{C_s\,L\,s}{C_s\,L\,s^2+1} + \frac{V_o}{s}\,\frac{1}{C_s\,L\,s^2+1} = V_{in}\,\frac{s}{s^2+\omega_0^2} + \frac{V_o}{s}\,\frac{\omega_0^2}{s^2+\omega_0^2}. \tag{2.23}$$

Applying the inverse Laplace transform, the capacitor voltage on stage 4 is defined at the time domain by

$$v_{Cs}(t) = V_o + (V_{in} - V_o)\,\cos(t\,\omega_0). \tag{2.24}$$

On the other hand, isolating the inductor current from the (2.21) and (2.22) yields

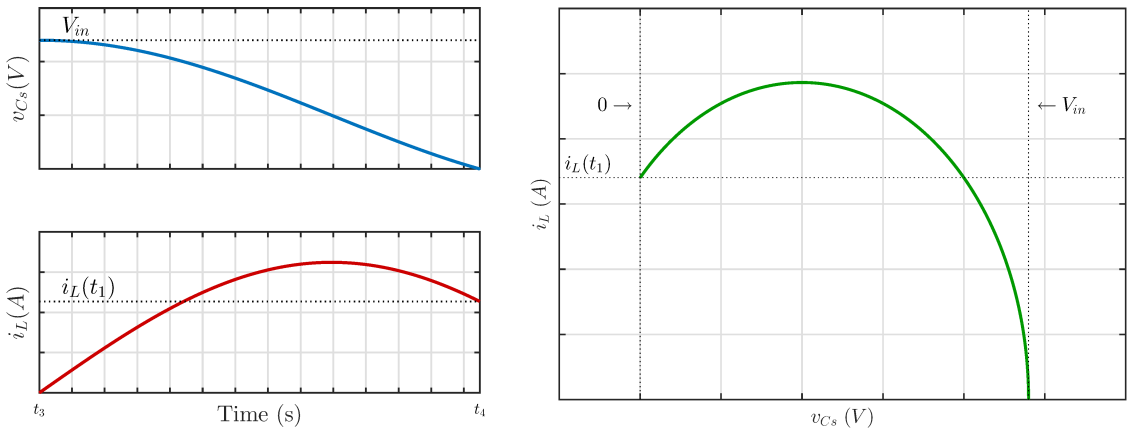
$$I_L(s) = C_s\,(V_{in} - V_o)\,\frac{1}{C_s\,L\,s^2+1} = C_s\,(V_{in} - V_o)\,\frac{\omega_0^2}{s^2+\omega_0^2}, \tag{2.25}$$

and, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\,\omega_0\,(V_{in} - V_o)\,\sin(t\,\omega_0). \tag{2.26}$$

The resulted waveforms described are shown in Figure 29.

Figure 29 – Buck RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



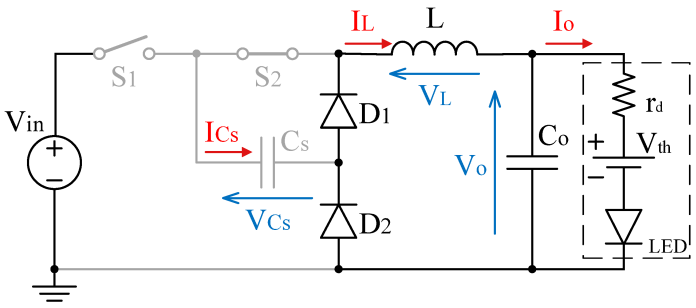
(a) (b)

Source: Author (2020).

With the complete discharge of the switched capacitor its voltage is maintained in zero, allowing the diode D_1 to be forward biased as shown in Figure 30. Once again, remnant energy on the inductor forces a current flow into both diodes. The initial conditions to this stage are described by

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = 0 \\ i_L(t_4) = I_{L\,(t4)} \end{cases} \tag{2.27}$$

Figure 30 – Buck RSC: stage 5.



Source: Author (2020).

The current and voltages at each semiconductor are summarized in Table 5.

Table 5 – Semiconductor Conditions for RSC buck: stage 5.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described as

Time Domain		Frequency Domain	
$L\,\frac{d}{dt} i_L(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L\,(s\,I_L(s) - I_{L(t4)}) = -\frac{V_o}{s}.$	(2.28)

With diode D_1 in conduction, the capacitor voltage is maintained its null value, that is,

$$v_{Cs}(t) = V_{Cs\,min} = 0. \tag{2.29}$$

The inductor behavior can be solved by isolating $I_L(s)$ from (2.28), which yields

$$I_L(s) = \frac{I_{L(t4)}}{s} - \frac{V_o}{L\,s^2}. \tag{2.30}$$

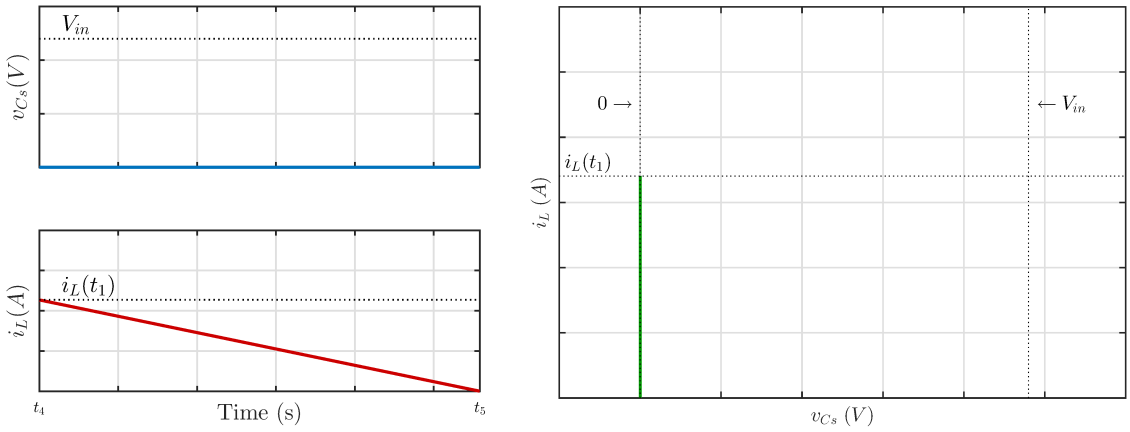
Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_L(t) = I_{L(t4)} - \frac{V_o}{L}\,t. \tag{2.31}$$

The resulted waveforms described are shown in Figure 31.

Finally, with the end of the energy at the inductors, its current reach zero before the ending of the switching cycle, resulting in the circuit shown in Figure 32. The time

Figure 31 – Buck RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



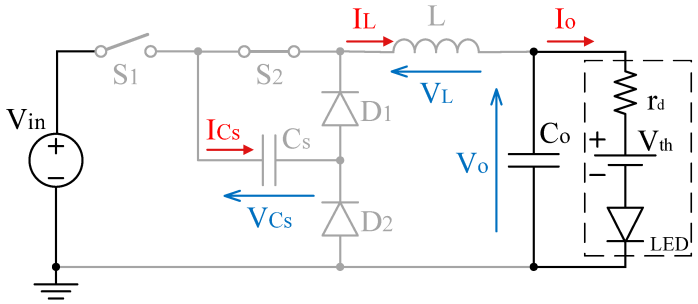
(a) (b)

Source: Author (2020).

between these two events characterizes the stage 6, which presents as initial condition the following

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = 0 \\ i_L(t_5) = 0. \end{cases} \tag{2.32}$$

Figure 32 – Buck RSC: stage 6.



Source: Author (2020).

Once again, through loop and node equations the state of each semiconductor can be described, as shown in Table 6.

Table 6 – Semiconductor Conditions for RSC buck: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} - V_o$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = V_{in} - V_o$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage 6 both capacitor voltage and inductor current are constant as

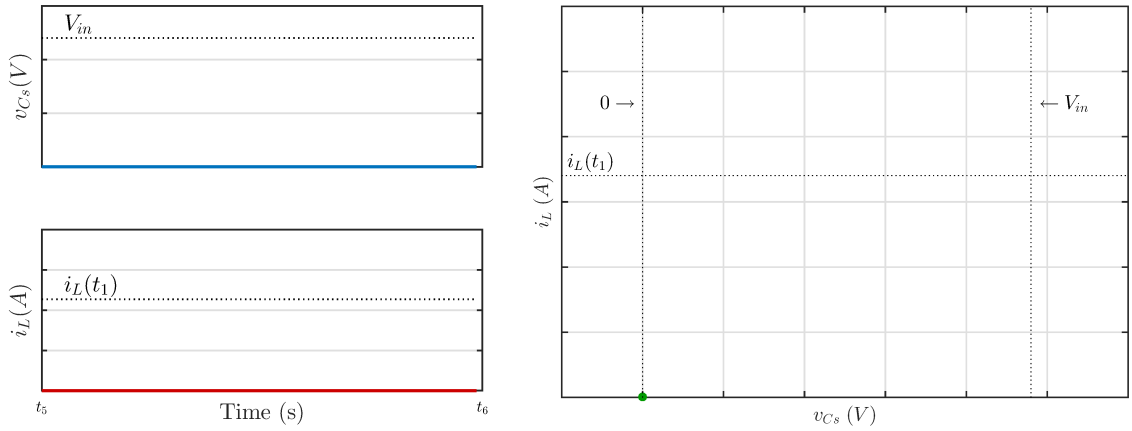
$$v_{Cs}(t) = V_{Cs\,min} = 0 \tag{2.33}$$

and

$$i_L(t) = 0. \tag{2.34}$$

The resulted waveforms described are shown in Figure 33.

Figure 33 – Buck RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

2.2.3 Time Analysis

In order to fully characterize the behavior of the converter, the time delay of each state must be determined.

2.2.3.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using the Eq (2.9) it is known that

$$v_{Cs}(t_1) = (V_{in} - V_o)\,(1 - \cos(\Delta t_1\,\omega_0)) = V_{in}. \tag{2.35}$$

Isolating Δt_1 and considering the value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$:

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{V_o}{V_o - V_{in}}\right) = \frac{1}{\omega_0}\,acos\left(\frac{G}{G-1}\right). \tag{2.36}$$

Applying the time duration for stage 1 into (2.11) it is possible to find the inductor current by the end of that stage, required as one of the initial conditions for stage 2:

$$i_L(t_1) = C_s\,\omega_0\,(V_{in} - V_o)\,\sin(\Delta t_1\,\omega_0) = C_s\,\omega_0\,(V_{in} - V_o)\,\sin\left(\frac{1}{\omega_0}\,acos\left(\frac{G}{G-1}\right)\,\omega_0\right). \tag{2.37}$$

The result is given by (2.38):

$$I_{L\,t1} = C_s\, V_{in}\, \omega_0 \sqrt{1-2G}. \tag{2.38}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1-2G>0$, which results in a design requirement given in (2.39):

$$G > \frac{1}{2}. \tag{2.39}$$

2.2.3.2 Stages 2 and 5

The second stage is characterized by the discharge of the remnant energy on the inductors. From (2.16) and (2.38) it is known that

$$i_L(t_2) = I_{L(t1)} - \frac{V_o}{L}\,\Delta t_2 = C_s\, V_{in}\, \omega_0 \sqrt{1-2G} - \frac{V_o}{L}\,\Delta t_2 = 0. \tag{2.40}$$

Isolating the time duration of the stage two, its value can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\, G}\sqrt{1-2G}. \tag{2.41}$$

2.2.3.3 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}, \tag{2.42}$$

which expands to

$$\frac{1}{\omega_0}\, acos\left(\frac{G}{G-1}\right) + \frac{1}{\omega_0\, G}\sqrt{1-2G} < \frac{1}{2\, f_s}. \tag{2.43}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\, f_s \left(acos\left(\frac{G}{G-1}\right) + \frac{1}{G}\sqrt{1-2G}\right). \tag{2.44}$$

2.2.4 Average Inductor Current

The average inductor current is found by integrating the current waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period

$$I_L = \frac{1}{T_s/2}\left(\int_{t_0}^{t_1} i_L(t)_1 dt + \int_{t_1}^{t_2} i_L(t)_2 dt\right). \tag{2.45}$$

Substituting current waveforms yields

$$I_L = 2\, f_s \left(\int_{t_0}^{t_1} C_s\, \omega_0\, (V_{in} - V_o)\, \sin(t\,\omega_0)\, dt + \int_{t_1}^{t_2} I_{L\,(t1)} - \frac{V_o}{L}\, t\, dt\right). \tag{2.46}$$

Solving the equation above and making use of the relations given by (2.36), (2.38) and (2.41), the average inductor current can be simplified as (2.47):

$$I_L = C_s\, f_s\, \frac{V_{in}}{G}. \tag{2.47}$$

2.2.5 Average Output Current

For the buck converter, the output current is the same as the inductor current. Therefore, the output current is given by (2.48):

$$I_o = C_s\, f_s\, \frac{V_{in}}{G}. \tag{2.48}$$

2.2.6 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\, V_o = C_s\, f_s\, \frac{V_{in}}{G}\, V_o. \tag{2.49}$$

Using the static gain definition stated as $V_o = G\, V_{in}$ the output power is given by

$$P_o = C_s\, f_s\, V_{in}^2. \tag{2.50}$$

The capacitor must be sized accordingly to the output power, using the relation given by (2.51):

$$C_s = \frac{P_o}{f_s\, V_{in}^2}. \tag{2.51}$$

2.2.7 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 7.

Table 7 – RSC boost simulation values for (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
output power	P_L	$10\,W$

(a)

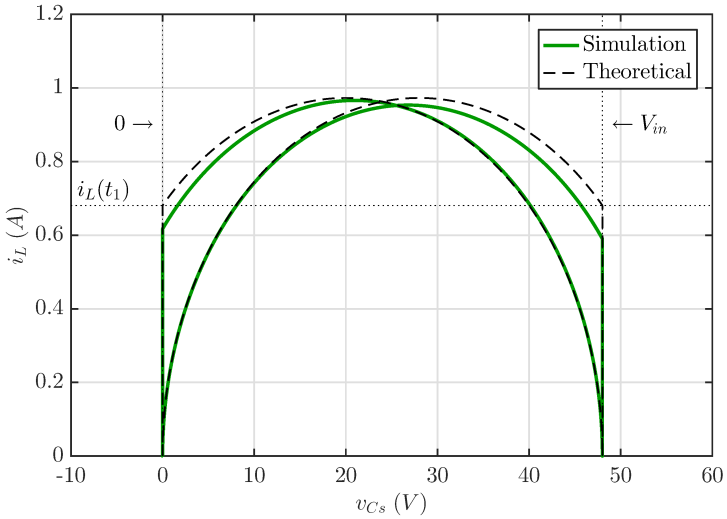
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$9.9\,nF$
Inductance	L	$8.2\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 34 yields a precise comparison between theoretical prediction and simulation result, highlighting differences imperceptible in the comparison on the time domain. More specifically, the resonant stages (1 and 4) were shown to diverge slightly in current level from the prediction, due to the inclusion of the previously simplified output loop.

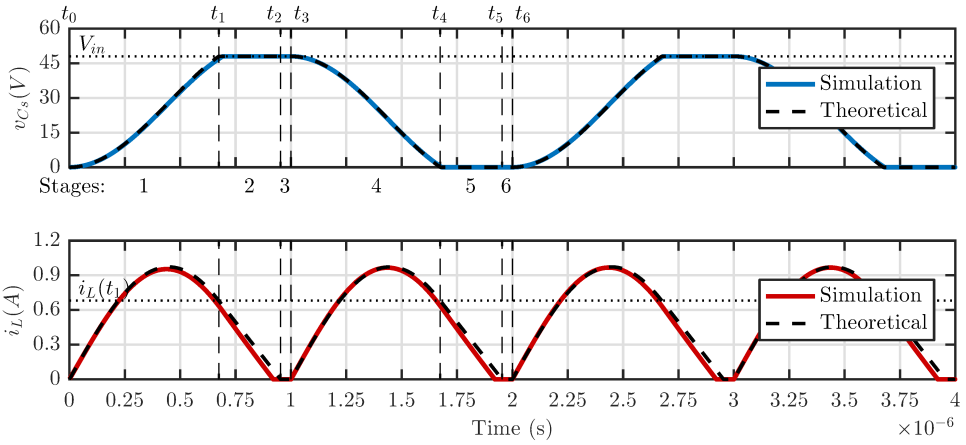
Figure 34 – State Plan for the RSC buck Converter.



Source: Author (2020).

Thus, the waveform comparison of the RSC buck converter states for each stage in their respective timespans is shown in Figure 35. The major noticeable difference resides in stages 2 and 5, where the demagnetizing of the inductor happens faster then predicted due to the effect of the output loop, which was considered as constant-voltage in the theoretical analysis. The small difference, however, highlights the consideration as a valid simplification of the circuit for its concise analysis.

Figure 35 – Theoretical waveforms of the state variables for the RSC buck converter.

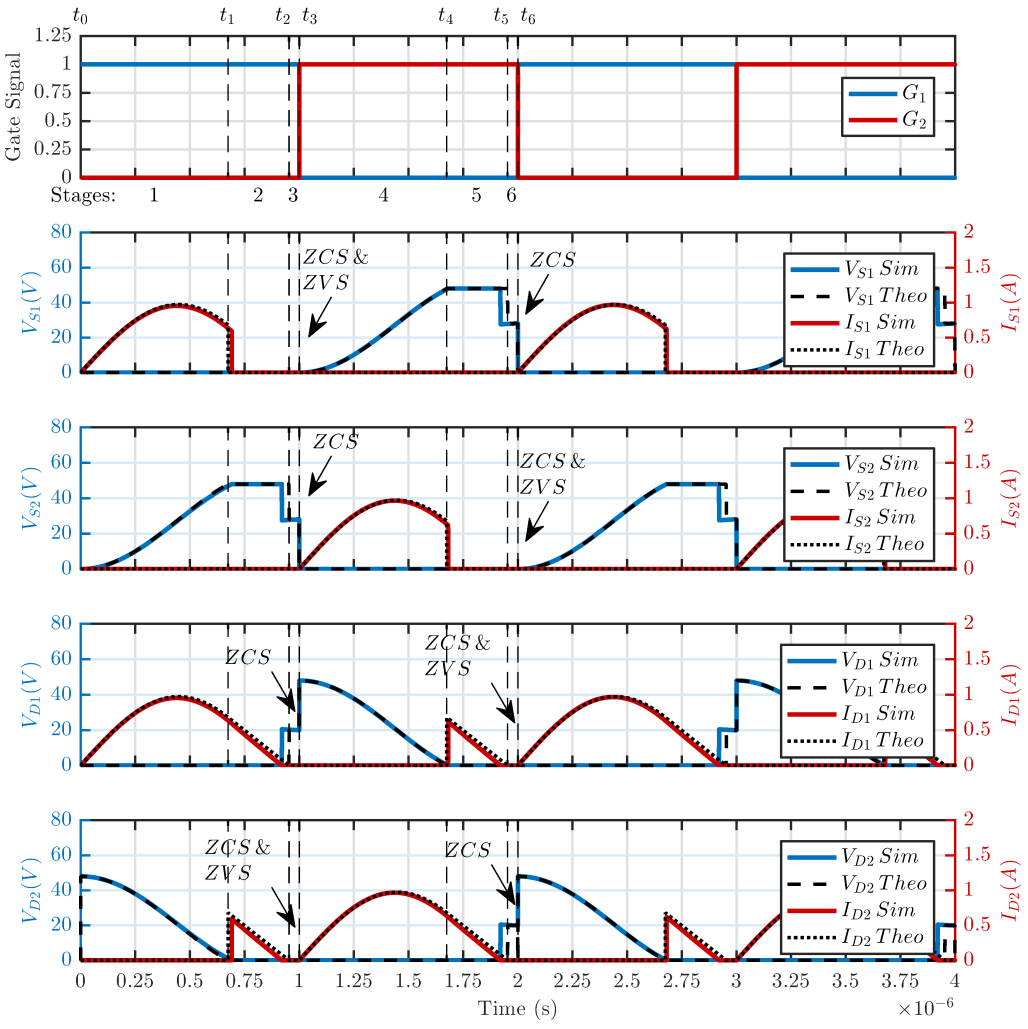


Source: Author (2020).

Finally, Figure 36 displays the voltage and current waveforms in each semiconductor

switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 36 – Soft-switching validation on the semiconductors for the RSC buck converter.



Source: Author (2020).

2.3 REMAINING LOWER-ORDER CONVERTERS

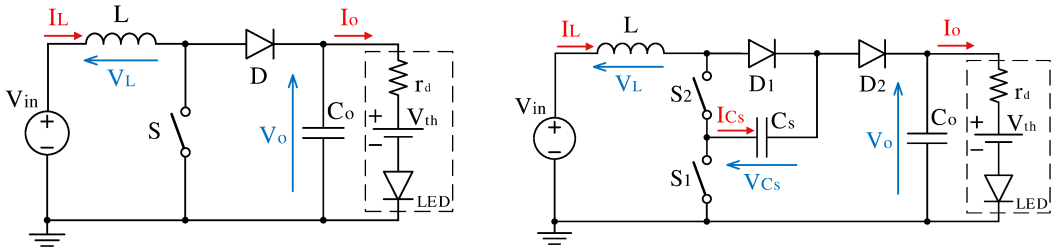
In order to keep this work concise and on point, the mathematical treatment realized for the buck Converter will be applied to the remaining converters on the Appendix. However, relevant discussion points will be discussed in this section in order to fully characterize the RSC Family as proposed. This discussions will be grounded on the results of the studies displayed on the appendix.

2.3.1 RSC boost

The RSC boost converter is based on the classical boost Converter element disposition, where the switching cell has been changed to the discussed switched capacitor cell.

Both versions can be seen on Figure 37.

Figure 37 – Classic boost converter (a) and RSC boost converter (b).

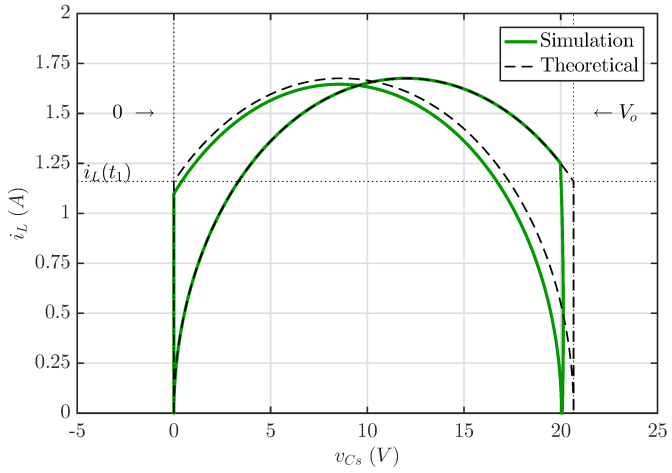


Source: Author (2020).

This converter follows the operational stages described in Section 2.1 by continuous charge and discharge of the switched capacitor, varying its voltage from $V_{Cs\,min} = 0$ to $V_{Cs\,max} = V_o$. The output voltage V_o is greater than the input voltage V_{in}, characterizing step-up mode, although its maximum possible value is capped at $V_{o\,max} = 2\,V_{in}$.

Simulation results showed operation as expected, with the state plane for such converter following the expected behavior, as shown in Fig. 38. Small disparities between theoretical prediction and simulated results can be attributed to the presence of the previously-simplified output loop. On the switched capacitor discharge stage (4), the output loop presents the effect of diminishing the inductor current slightly, an effect not present during the other resonant stage (1) since it effectively opens the circuit from the output loop, excluding its influence. Similarly, the charged states of the capacitor (2 and 3) are also affected once the output voltage is not exactly constant as predicted.

Figure 38 – State Plan for the RSC boost Converter.



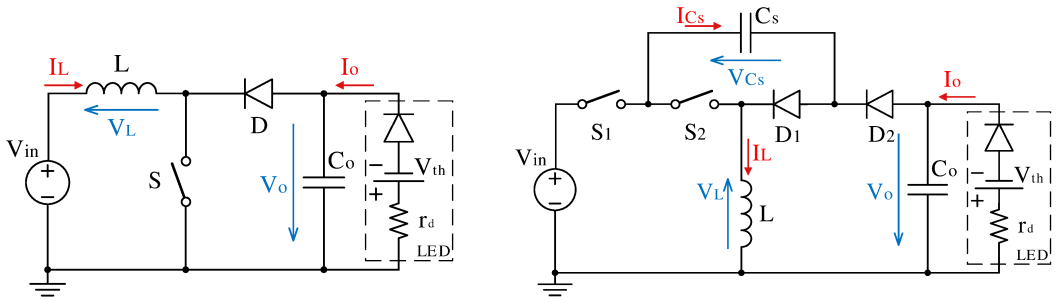
Source: Author (2020).

Nevertheless, such dissonances between theoretical prediction and simulation verify the expected behavior of the converter, fully displaying the simplification of constant output voltage as a valid modeling tool for this circuit.

2.3.2 RSC buck-boost

Both classic and RSC versions of the buck-boost converter can be seen on Figure 39, highlighting clearly its similar element disposition.

Figure 39 – Classic buck-boost converter (a) and RSC buck-boost converter (b).



(a) (b)

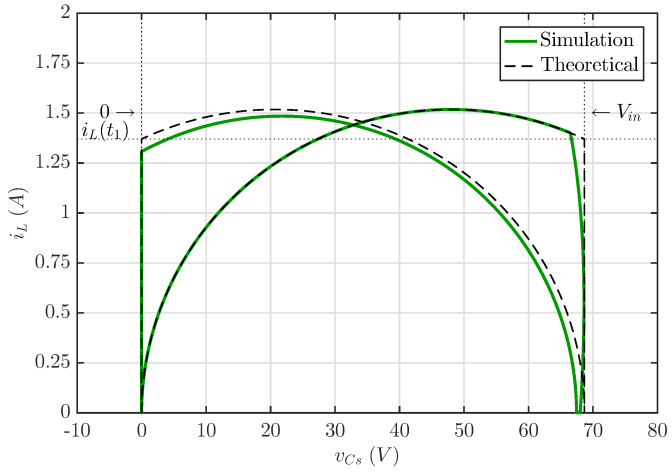
Source: Author (2020).

The RSC buck-boost converter charges and discharges the switched capacitor as expected by the description in Section 2.1, changing its voltage between $V_{Cs\,min} = 0$ to $V_{Cs\,max} = V_{in} + V_o$. The maximum possible output voltage, however, is limited to $V_o = V_{in}$, limiting the RSC buck-boost converter to step-down operation, unlike its classic version that could operate in step-up mode.

The state plane for such converter is shown in Figure 40, allowing comparison between simulation and mathematical analysis. Once again, the small disparities are attributed to the presence of the output loop, once they only occurs on the stages where such loop is active. Mainly, the resonant discharging stage (4) is differentiated from the resonant charging state (1) by the inclusion of the output loop into the converter, resulting in a a slightly smaller inductor current than expected. Additionally, the variable nature of the output voltage V_o, previously considered constant, is made clear on the switched capacitor charged stages (2 and 3).

Nevertheless, such dissonances between theoretical prediction and simulation verify the expected behavior of the converter, fully displaying the simplification of constant output voltage as a valid modeling tool for this circuit.

Figure 40 – State Plan for the RSC buck-boost Converter.

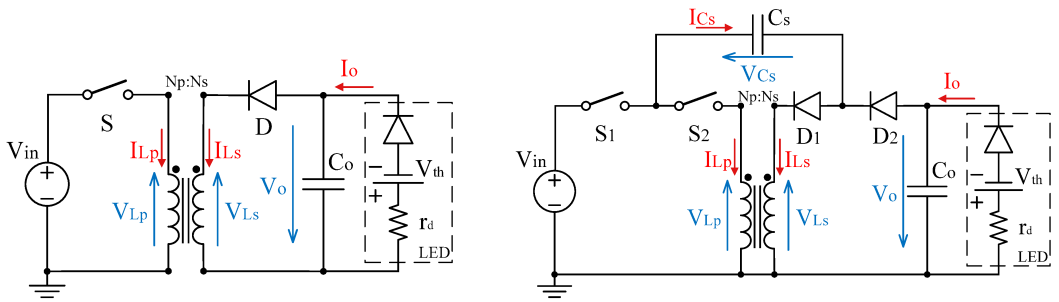


Source: Author (2020).

2.3.3 RSC flyback

In both classic and RSC versions, the flyback converter comprises on a buck-boost converter where the magnetizing element has been changed to two elements magnetically coupled, as shown in Figure 41.

Figure 41 – Classic flyback converter (a) and RSC boost converter (b).



(a) (b)

Source: Author (2020).

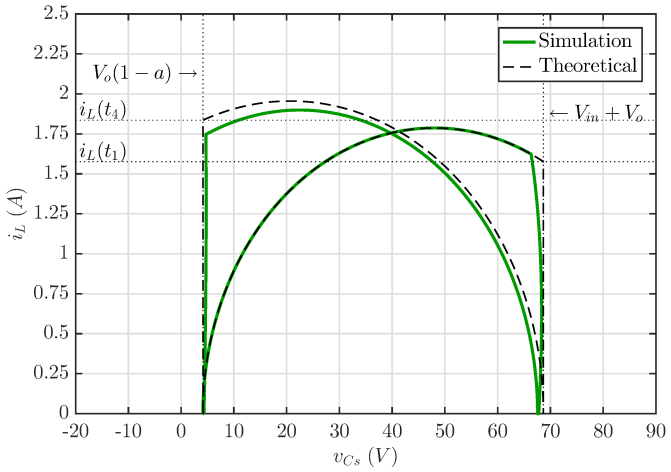
The presence of the coupled inductors causes the flyback RSC converter to presents a singular characteristics on the RC Family: the asymmetrical resonant stages. Since the inductance of the magnetizing element is seen differently from either side of the transformer according to the turns-ratio, the charge and discharge of the switched capacitor occurs at different current levels. Because of the reason, the voltage at the discharge state is not capped at zero, but rather, at $V_{Cs\,min} = V_o(1 - a)$. The buck-boost converter remains a singular case of the flyback converter, where $a = 1$. Furthermore, the maximum voltage at the switched capacitor is the same for the Flyback as it is for the buck-boost converter: $V_{Cs\,max} = V_{in} + V_o$.

Disparities between simulation and theoretical prediction can be seen on the state plan shown in Figure 42. This disparities occur in the stages in which the output loop

(theoretically simplified as constant-voltage) is include in the current path. For instance, the discharging resonant stage (4) presents a disparity in current level from the theoretical prediction, which does not occur in the charging stage (1). On the same note, the variance of the output voltage can be explicitly seen on the stages where the switched capacitor is charged (2 and 3), where the consideration of constant output voltage is made clear. In the stages where the switched capacitor is discharged, the output voltage is also shown to be different than predicted, but this difference is attenuated by the factor $(1 - a)$.

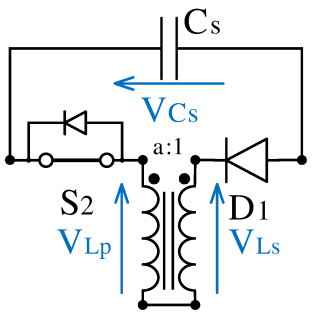
Unlike the classic flyback, the RSC flyback is not galvanic isolated due to the mandatory presence of the switched capacitor. Furthermore, the addition of the coupled magnetic elements does not grant step-up capabilities for this converter, being limited to step-down operation as the buck-boost converter. The asymmetrical resonant stages result in two DCM requirements that must be met, as shown in Figure 44. And even though this requirements depend on the turns ratio a, its value is limited at $a_{max} = 1$ due to the intrinsic diode present on the active switch S_2, that must be reversed biased on the L_p-S_2-C_s-L_s loop highlighted in Figure 43.

Figure 42 – State Plan for the RSC flyback Converter.



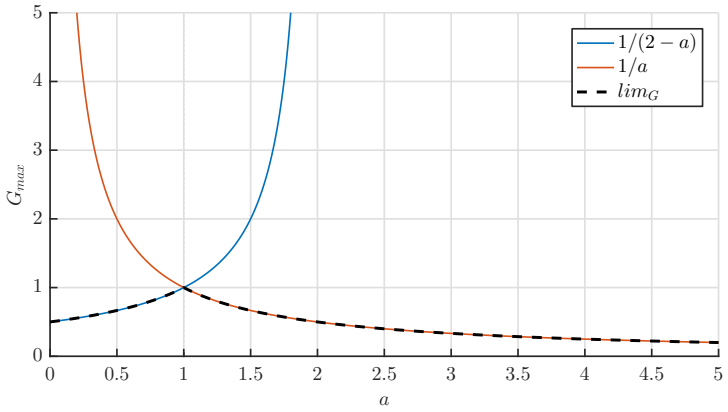
Source: Author (2020).

Figure 43 – Limiting loop for turns ratio a.



Source: Author (2020).

Figure 44 – Static gain limitations regarding turns-ratio 'a' for the flyback RSC converter.



Source: Author (2020).

2.4 HIGHER-ORDER RSC CONVERTERS

The Higher-Order RSC converter are the analogous versions of the classic Ćuk, SEPIC, and Zeta converters. These converters present in their classic form two inductors (L_1 and L_2) and an input capacitor C_1 as reactive elements, besides the previously discussed output capacitor C_o. ZCS is achieved by operating in DCM mode, which in contrast to the lower-order converters, do not imply in null inductor current. Rather, DCM is characterized by the condition where both inductor currents reach opposite values, achieving mutual cancellation. For these classic higher-order converters, DCM mode can be described by the diode current reaching zero, since it represents the sum of both inductor's currents. A similar assumption can be made for the RSC converters by defining an equivalent diode current $i_d(t)$ as $i_d(t) = i_{L1}(t) + i_{L2}(t)$. It is important to note that this current is not a representation of neither the currents on the diodes of the switched capacitor cell, but a mathematical construct used to better define DCM mode and the different stages.

Regarding the input capacitor C_1, the use of a high enough value of capacitance allows for a simplification of constant voltage that excludes this additional state from the model. This simplification is important in order to reduce the complexity of these circuits without affecting the accuracy of the model. Due to this consideration, the voltage at the input capacitor C_1 must be determined prior to the circuit analysis. Lastly, the resonant frequency for the high-order converters is defined by

$$\omega_0 = \sqrt{\frac{1}{L_e\, C_s}}. \tag{2.52}$$

Where the equivalent inductor L_e is defined by the association between inductors L_1 and L_2 by

$$L_e = \frac{L_1\, L_2}{L_1 + L_2}. \tag{2.53}$$

The operation of the RSC converter can be divided in six basic stages:

a) Charging of the switched capacitor C_s up until forward biasing of diode D_2;

b) Closed loop through diodes allows the demagnetizing of the inductors down to mutual current cancellation;

c) Off-time of null equivalent diode current i_d;

d) State change in both active switches, allowing discharge of switched capacitor C_s down to forward biasing diode D_1;

e) Closed loop through diodes allows the demagnetizing of the inductors down to mutual current cancellation;

f) Off-time of null equivalent diode current i_d.

As can be seen, each stage begins with the capacitor either at its maximum or minimum values, which is determined by the reverse biased diodes in stages 1 and 4. Thus, similarly to the lower-order RSC converters, the analysis of the higher-order RSC converters also demands firstly the analysis of the voltage loops between switched capacitor C_s and reverse biased diodes in stages 1 and 3, allowing then the initial conditions of the converter to be met. However, in order to complete such analysis, it is important to prior determine the constant voltage at the input capacitor C_1.

By knowing the initial conditions, it is possible to mathematically describe the state equations of the circuits V_{Cs}, I_{L1} and I_{L2} in the time domain by making use of direct and inverse Laplace Transforms. The resulted description is required for the study and design of such converters. In summation, the analysis of the higher-order RSC converters follows the according sequence:

a) Analysis of the input capacitor voltage;

b) Analysis of the resonant capacitor voltage;

c) Analysis of each of the six operating stages;

d) Analysis of time delay between stages;

e) Analysis of Average Equivalent Diode Current;

f) DCM Current Offset;

g) Analysis of average output current;

h) Analysis of output power.

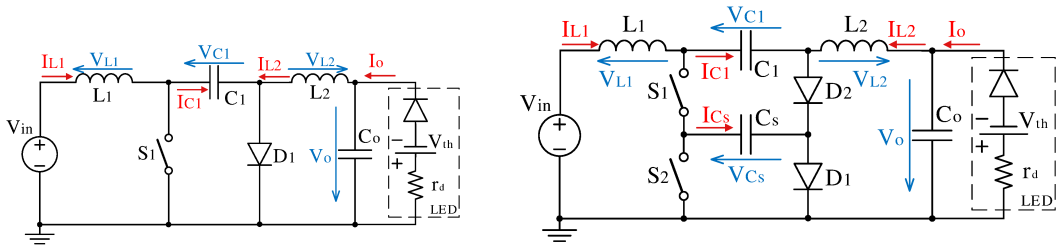
The relations of power, frequency, inductance and capacitance derived for the higher order RSC converter follows roughly the same form of the lower-order RSC converters, meaning that the additional elements must be designed in accordance with different parameters. This element sizing can be performed in several different ways. Two alternatives for inductance design are discussed in this section, as well as an example of input capacitor

design. The procedure and results discussed in this section applies to all three higher-order RSC converters presented.

2.4.1 RSC Ćuk, SEPIC and zeta converters

The classic and resonant versions of the higher order converters are shown in Figures 45, 46 and 47, where the disposition of the elements can clarifies how such RSC converters were derived.

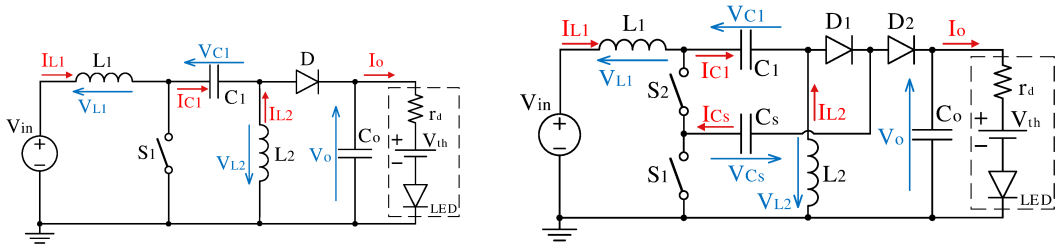
Figure 45 – Classic Ćuk converter (a) and RSC Ćuk converter (b).



(a) (b)

Source: Author (2020).

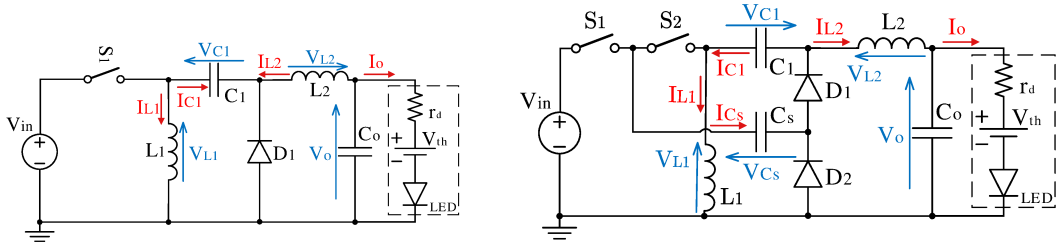
Figure 46 – Classic SEPIC converter (a) and RSC SEPIC converter (b).



(a) (b)

Source: Author (2020).

Figure 47 – Classic Zeta converter (a) and RSC Zeta converter (b).



(a) (b)

Source: Author (2020).

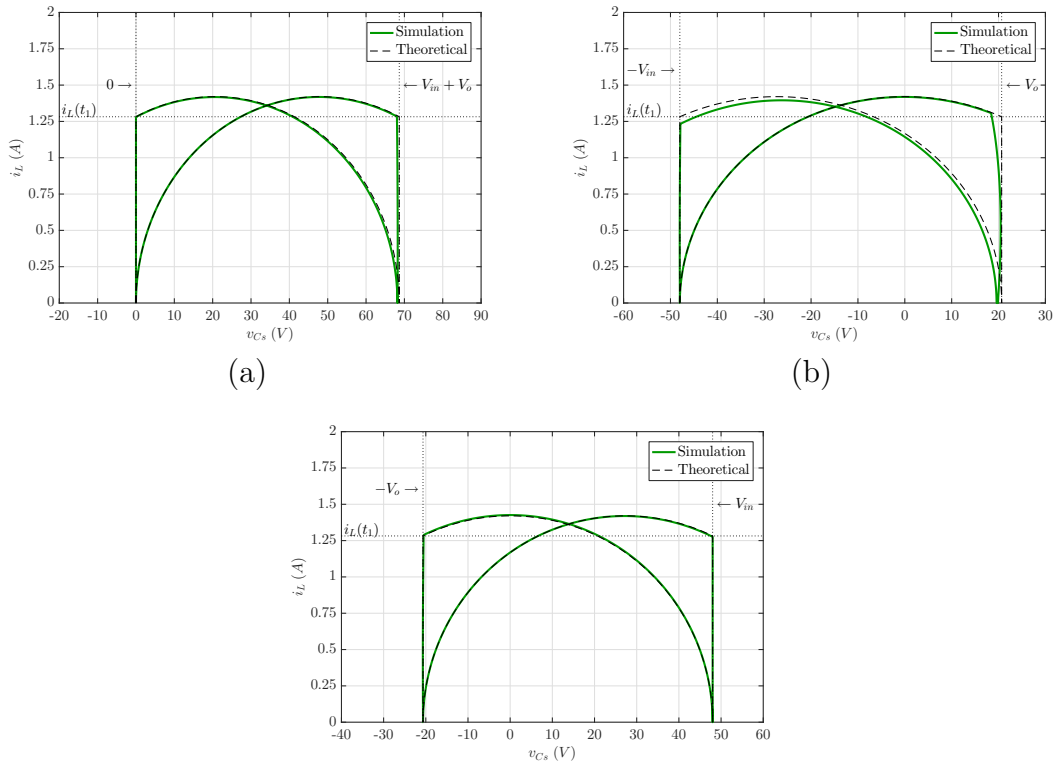
The higher-order RSC converter operate by following the six-stages descrbed in 2.4, where the main difference with the lower-order converters lies on the presence of a second inductor. As a result, DCM operation can not be characterized through a single inductor current, but rather, to the sum $i_d = i_{L1} + i_{L2}$. The variable i_d is created to represent

such sum, relating to the diode current that characterizes DCM operation in the classic higher-order converters.

Similarly to the lower-order converters, the higher-order converters continuously charge and discharge the switched capacitor, with the minimum and maximum voltage values depending on each topology. In all three cases, the absolute voltage variation is the same as the one of the buck-boost converter ($\Delta V_{Cs} = V_{in} + V_o$). Again as the buck-boost converter, the higher-order converters are unable to operate in step-up mode, unlike their classic versions, being limited to step-down operation.

The state plane for each converter can be seen on Figure 48. For the converters were the output loop is isolated from the circuit through an inductor (Ćuk and Zeta), the effects of the non-ideal output loop are stopped from affecting the circuit, and the simulated converter follows the theoretical prediction exactly. For the SEPIC converter, where the output loop is connected directly through the switching cell, the effects of the output loop can be perceived as seen in the lower-order converters.

Figure 48 – State Plan for the (a) RSC Ćuk converter (b) RSC SEPIC converter and (c) RSC Zeta converter.



Source: Author (2020).

2.4.2 Inductances

While the equivalent inductance L_e is locked by the resonance frequency and capacitance, there is certain flexibility for the choice of the individual inductor. This is

because there are infinite different combinations of L_1 and L_2 inductances that can yield the same equivalent inductance L_e. Furthermore, the inductor size can be determined by a couple of different methods that can be chosen due to given application.

2.4.2.1 Current Variation

For applications in which the maximum current variation for a given inductor must be set, the equation for the inductor current can be used with the assumption of maximum current. For instance, using (A.186), (A.272) or (A.357) and assuming the time instant t that yields maximum current, the current variation and be described as

$$\Delta I_{L1} = I_{L1\,max} - I_{L\,DCM} = \frac{V_{in}}{L_1\,\omega_0}. \tag{2.54}$$

An equivalent equation can be found for the second inductor, as the design can be made considering whichever inductor current must be limited in terms of maximum variation. For instance, the RSC Ćuk converter presents inductors in both input and output, and depending on the application, limiting current variation in either (or both) input and output is imperative.

The remaining inductance is then sized by the L_e definition described in (2.53), which does imply in a trade-off in terms of current variation between both inductors.

2.4.2.2 Minimum DCM Current Offset

An alternative method for sizing the inductances can be derived from the requisite of minimizing the constant current on the inductors during stage three. Using the relation found by (A.246), (A.332) or (A.417) it can be noted that null DCM current can be achieved when

$$G\,L_1 - L_2 = 0 \rightarrow L_2 = G\,L_1. \tag{2.55}$$

Applying such relation at the definition of L_e introduced in (2.53) the inductance L_1 can be isolated resulting in

$$L_1 = L_2\,\frac{G+1}{G}. \tag{2.56}$$

2.4.3 Input Capacitor

The calculation presented considered that the input capacitor C_1 does not affect the high-frequency behavior of the converter. The presence of the capacitor does however create a low-frequency behavior which will only not affect the high-frequency behavior by a large band separation between each resonant frequency. Mathematically, this restriction can be written as

$$\omega_o \gg \omega_{low\,freq}. \tag{2.57}$$

While the high-frequency behavior is set by the switched capacitor which is connected in parallel with inductances L_1 and L_2, the low frequency behavior is related to the input capacitor, which is connected in series with the same inductors. Finding the resonant frequencies yields the relation between components given by

$$\frac{1}{C_s\, L_2} \gg \frac{1}{C_1\, (L_1 + L_2)}. \tag{2.58}$$

By isolating capacitor C_1 and considering a band factor ω_{band} equivalent to the disparity between both resonant frequencies, the capacitor C_1 can be found by

$$C_1 = \omega_{band}\, \frac{L_1\, L_2}{(L_1 + L_2)^2}\, C_s. \tag{2.59}$$

Where the greater value of ω_{band} the more accurate the high-frequency behavior will be due to the high attenuation of the low-frequency behavior.

2.5 PARTIAL CONCLUSIONS

In hindsight, having the mathematical analysis of the seven converters in question allows for brief comparisons. The summary of the main characteristics for each converter is presented in Table 8. A few characteristics must be highlighted.

First, the RSC converters can be differentiated by its static gain, with the RSC boost converter being the single one out able to achieve step-up mode, unlike other converters of its family. In the other hand, this static gain shows a limitation not present on the conventional buck converter at $V_o/V_{in} \leq 2$, which can significantly compromise its application.

For the remaining RSC converters, it must be noted that step-up mode is impossible even for the topologies that allows such mode in its conventional form. However, such topologies still differentiate themselves from the RSC buck converter in their range of static gain, where the latter is limited at $V_o/V_{in} \leq 0.5$.

It is also imperative to note that the RSC flyback converter, due to inherent limitations in the turns-ratio of the transformer, is still unable to achieve step-up mode. Furthermore, this converter imperatively loses its isolated characteristic present in its conventional form due to the addition of the switched capacitor C_s. In summation, the attractiveness of the conventional flyback converter is severely damaged, if not completely lost, in its switched capacitor form.

The RSC buck-boost type, although still unable to present step-up operation, remains with its clear similarities with the higher-order converters of its switched capacitor family, presenting same average inductor current, output current and output power, given the same converter design. The differentiation remains in its simplicity and number of

components, specially in regards to the Ćuk converter, where even switched capacitor minimum and maximum voltages remains the same.

The last remaining RSC converters, SEPIC and Zeta, are both of higher order, and differentiation remains on the minimum and maximum voltages at the switched capacitor. Equally, these converter differentiate themselves and between the Cuk converter by the voltage required at the input capacitor C_1.

Finally, presenting many similar characteristics, it is important to note that the RSC converters will, at most cases, shadow themselves into the same applications, and the optimal design will depend on the advantages of inductor placement and input capacitor availability.

Table 8 – Summarized main characteristics of RSC converters.

	Static Gain		**Capacitor Voltages**			**Current and Power**			**Semiconductor Stress**			
	G_{min}	G_{max}	$v_{Cs\,min}$	$v_{Cs\,max}$	v_{C1}	$I_{L\,avg}$	$I_{o\,avg}$	P_o	$I_{d\,max}$	$I_{s\,max}$	$V_{d\,max}$	$V_{s\,max}$
Buck	0	1/2	0	V_{in}	–	$C_s\,f_s\,V_{in}\,\frac{1}{G}$	$C_s\,f_s\,V_{in}\,\frac{1}{G}$	$C_s\,f_s\,V_{in}^2$	$C_s\,\omega_0\,(V_{in}-V_o)$	$C_s\,\omega_0\,(V_{in}-V_o)$	V_{in}	V_{in}
Boost	1	2	0	V_o	–	$C_s\,f_s\,V_{in}\,\frac{G^2}{G-1}$	$C_s\,f_s\,V_{in}\,\frac{G}{G-1}$	$C_s\,f_s\,V_{in}^2\,\frac{G^2}{G-1}$	$C_s\,\omega_0\,V_{in}$	$C_s\,\omega_0\,V_{in}$	V_o	V_o
Buck-Boost	0	1	0	$V_{in}+V_o$	–	$C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}$	$C_s\,f_s\,V_{in}\,\frac{G+1}{G}$	$C_s\,f_s\,V_{in}^2\,(G+1)$	$C_s\,\omega_0\,V_{in}$	$C_s\,\omega_0\,V_{in}$	$V_{in}+V_o$	$V_{in}+V_o$
Flyback	0	1	$V_o\,(1-a)$	$V_{in}+V_o$	–	$C_s\,f_s\,V_{in}\,\frac{(a\,G+1)^2}{G}$	$C_s\,f_s\,V_{in}\,\frac{(a\,G+1)}{G}$	$C_s\,f_s\,V_{in}^2\,(a\,G+1)$	$C_s\,\omega_0\,(V_{in}-V_o\,(1-a))$	$C_s\,\omega_0\,(V_{in}-V_o\,(1-a))$	$(V_{in}+V_o)/a$	$V_{in}+V_o$
Cuk	0	1	0	$V_{in}+V_o$	$V_{in}+V_o$	$C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}$	$C_s\,f_s\,V_{in}\,\frac{G+1}{G}$	$C_s\,f_s\,V_{in}^2\,(G+1)$	$C_s\,\omega_0\,V_{in}$	$C_s\,\omega_0\,V_{in}$	$V_{in}+V_o$	$V_{in}+V_o$
SEPIC	0	1	$-V_{in}$	V_o	V_{in}	$C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}$	$C_s\,f_s\,V_{in}\,\frac{G+1}{G}$	$C_s\,f_s\,V_{in}^2\,(G+1)$	$C_s\,\omega_0\,V_{in}$	$C_s\,\omega_0\,V_{in}$	$V_{in}+V_o$	$V_{in}+V_o$
Zeta	0	1	$-V_o$	V_{in}	V_o	$C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}$	$C_s\,f_s\,V_{in}\,\frac{G+1}{G}$	$C_s\,f_s\,V_{in}^2\,(G+1)$	$C_s\,\omega_0\,V_{in}$	$C_s\,\omega_0\,V_{in}$	$V_{in}+V_o$	$V_{in}+V_o$

Source: Author (2020).

3 VLC-DRIVEN DESIGN AND EXPERIMENTAL SETUP

As previously mentioned in Chapter 1, several alternatives have been proposed for VLC implementation. Mostly, the straightforward strategy for both carrier-based (single or multi) and pulse-base transmissions is to embed both required functions (lighting and data transfer) into a single fast-response power converter. These solutions are, however, complex.

Alternatively, it is possible to separate the data transfer functionality into a single low-power linear amplifier that can operate at higher speeds. The LED biasing is then achieved through a slow-response power converter, responsible for the lighting aspect of the lamp. This strategy presents circuits with lower complexity than the single fast-response power converter, albeit the system is not significantly simplified since it requires multiple circuits.

Through some PBT techniques, however, it is possible to bypass this high-complexity circuits by taking advantage of the inherent dc level contained in pulsed currents, such as those obtained by pulse-width modulation. This property allows for the blending of both lighting and data transfer function into a unique high-power, variable width pulsed signal. Achieving such signal demands circuits with significant lower complexity, as has been shown in literature. Adequate transmission performance can be achieved simply through a slow-response power converter and an auxiliary output switch.

With this proposition, the slow-response power converter is responsible for energy processing, keeping the output capacitor charged at required voltage. Meanwhile, the auxiliary output switch is responsible for determining the instants where this energy is allowed to be transferred to the LED, creating a high-frequency pulsed signal accordingly for the data transferred. Furthermore, the width of the pulsed signal determines the average light level. So not only this strategy is simpler in terms of electronics, it is also simpler in terms of light modulation, as a low-power single signal is responsible for both dimming and data transfer functions.

Good performance has already been shown in the literature with the auxiliary VLC switch for dual-purpose converters. For instance, a resonant LLC converter is proposed by Zhao, Xu e Trescases (2014), achieving high efficiency ($> 90\%$) for a $80\,W$ LED lamp, with a transmission rate of up to $47\,kbps$. In the meantime, Modepalli e Parsa (2015) studies a smaller load ($\approx 5.8\,W$) over a higher transmission rate of $2\,Mbps$ controlled by an ac buck converter. The result is a lower efficiency of 83% (at 80% brightness), with the auxiliary switch comprising nearly 15% of that losses. At the same transmission rate ($2\,Mbps$), Modepalli e Parsa (2017) shows a $\approx 9.5\,W$ buck-boost-buck converter operating with around 80% efficiency (at brightness of 80%). Finally, Salmento *et al.* (2019) achives an efficiency of 92% at 80% brightness, with a $20\,W$ prototype at different types of modulation,

reaching up to 1.1 $Mbps$. This result is achieved with a buck-boost converter, proposing a new modulating scheme (all the other aforementioned papers operate in VPPM).

Most importantly, Salmento *et al.* (2019) displays theoretical and experimental data of the switching losses at the auxiliary switch for different transmission rates, highlighting the most important problem with the auxiliary VLC solution: the inherent inverse relation between efficiency and transmission rate. As the auxiliary switch must supply and stop energy to be transferred to the LED at high speeds, it will invariably operate in hard switching. This is a significant problem not only as data transfer rate tends to increase (thus increasing its switching frequency) but also as the light sources tend to increase in power.

Foremost, by eliminating the sum of a dc level and leaving solely to the data signal, the converter inevitably forces a high stress to the LED due to the constant on-off switching. Regardless, it is important to notice that this high-stress does not translate to harmful ripples levels (flickering) once the operating frequency is far beyond the perceived by the human eye.

On the long run, although the strategy of the auxiliary switch has been proven to be effective, presenting invariably drawbacks in efficiency with both increase of power and switching frequency is not the optimal characteristics for a device that should perform both power and data processing. As such, optimally, a converter of fast response capable of complete power-up/shut-down at high frequencies is a desirable approach to the synthesis of the high-power data signal demanded by the PBT techniques.

In order to operate in high speed turn-on and -off, such converter would, as a requirement, present high efficiency at high frequencies. With all the semiconductors operating under constant ZCS due to the DCM operation and still presenting ZVS in half the switching instants, the resonant switched-capacitor converters presented in Sections 2.1 and 2.4 are adequate candidates for such function.

This chapter describes both the theoretical design and practical prototyping of a VLC transmitter focused on the RSC buck-type converter described in Section 2.1. Through DCM operation, the inductance value of the magnetizing element falls considerably, resulting in higher current slew rate. Additionally, by allowing efficient high-frequency operation through soft switching, such converter allows for fast dynamic response, adding to a reliable burst-mode, and thus nullifying the need of an auxiliary switch. VPPM is the chosen modulation scheme given its simplicity of not requiring a compensation symbol.

3.1 TURN-ON AND TURN-OFF DYNAMICS

With the absence of a VLC switch, the output loop will always form a closed path for circulating current, allowing for the discharge of the output capacitor C_o. In steady

state, this should not be a problem once stages 3 and 6 are ideally much shorter than their predecessors in order to ensure smallest inductor current peaks. However, for VLC applications employing burst-mode operation, this outer loop must be taken into account, once the required off-times of the burst mode will lead to possible significant discharge of the output capacitor C_o. As a result, the pulses will suffer delays during both turn on and turn off, which can affect how the signal is interpreted in the receptor if not properly taken into account.

3.1.1 Turn-off/Shut-down behavior

The turn off of the converter will ideally occur alongside stage 6, assuming DCM operation for maximum efficiency. The output active loop is composed by the output capacitor C_o and the LED. The current waveform during turn off is found through (3.1).

$$i_o(t)_{off} = I_{o\,nom}\, e^{-t/\tau_o} \tag{3.1}$$

Where τ_o is defined as described through (3.2).

$$\tau_o = r_d\, C_o \tag{3.2}$$

Considering $t = t_{fall}$ where current falls to an arbitrary factor k_f of the output average current ($i_o(t_{fall}) = k_f\, I_{o\,nom}$), the time delay can be found through

$$t_{fall} = \tau_o\, ln(k_f^{-1}), \tag{3.3}$$

Where k_f can be defined by the designer accordingly to what is considered off state. For instance, a $k_f = 0.1$ means that fall-time is defined as when the output current reaches 10% of the nominal value $I_{o\,nom}$.

3.1.2 Turn-on/Power-up behavior

Equivalently, the turn on dynamics will occur during stage 1, where the analyzed current path contains the switched capacitor C_s and the inductor in parallel to the output loop. The initial output voltage for this loop must also be considered as the minimum capacitor voltage, i.e., the LED threshold voltage V_t. The description of the current behavior during this time interval in given through

$$i_o(t)_{on} = \frac{V_{in} - V_t}{r_d + \dfrac{Z_o\,(\tau_o^2\,\omega_o^2 + 1)}{sin(\omega_o\,t) + \tau_o\,\omega_o(e^{-t/\tau_o} - cos(\omega_o\,t))}} \tag{3.4}$$

where Z_o is defined as $Z_o = \sqrt{L/C_s}$.

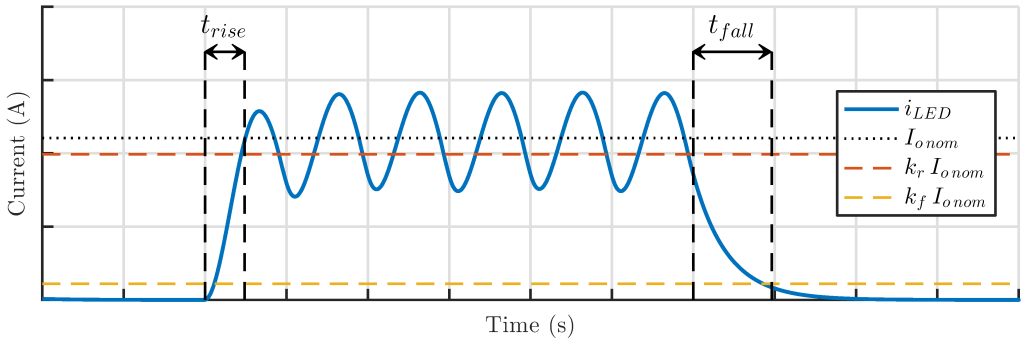
Once isolating the time t factor in Eq. 3.4 is not feasible, this transcendental equation must be solved numerically in order to find the required time $t = t_{rise}$ for the output current to reach an arbitrary k_r factor of the average output current. Thus, the rising time can be found by solving

$$i_o(t_{rise})_{on} = k_r \, I_{o\,nom}. \tag{3.5}$$

Once again, t_{rise} is defined by the designer through the k_r factor that represents which percentage of the nominal current output value is required for the converter to be considered under on state: for instance, a factor $k_r = 0.9$ defines t_{rise} as the time required for the converter to reach 90% of it nominal value.

The theoretical turn-on and turn-off LED waveforms are displayed in Figure 49, where the definitions of k_r and k_f can be graphically described.

Figure 49 – LED turn-on and turn-off times.



Source: Author (2020).

3.2 RSC BUCK CONVERTER DESIGN EXAMPLE AND ROUTINE

In order to demonstrate the capabilities of the RSC buck converter to be designed in light of the VLC requirements, this section will present a step-by-step design process for a $10\,W$ LED converter fed by a $48\,V$ input voltage. Other significant data are highlighted in Table 9.

Table 9 – Source and load values.

LED Lamp		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_o	$10\,W$
Nominal Output Voltage	$V_{o\,nom}$	$20.32\,V$
Input Voltage	V_{in}	$48\,V$

Source: Author (2020).

3.2.1 Data Transmission and Power Requirements

The average value of the inductor current, presented in (3.6), can be calculated by means of its waveforms shown in previous section. This result can be used together with the definition of the average output power $P_o = V_o\, I_o$ to yield (3.7). This equation relates the equivalence between output power, switched capacitor's capacitance C_s and switching frequency.

$$I_L = C_s\, f_s\, \frac{V_{in}}{G} \tag{3.6}$$

$$P_o = C_s\, f_s\, V_{in}^2 \tag{3.7}$$

Since the output power is predetermined by load and capacitance values must follow commercial availability, the frequency is used as the main independent design variable. Once a finite integer number of high-frequency pulses are allowed in data period, the transmission rate f_d is a multiple of the switching frequency f_s. Thus, as can be seen, the process of choosing data transmission rate is tied to the load power and the design must be made iterative, rather than in closed form. This first part of the design process can be divided as follows.

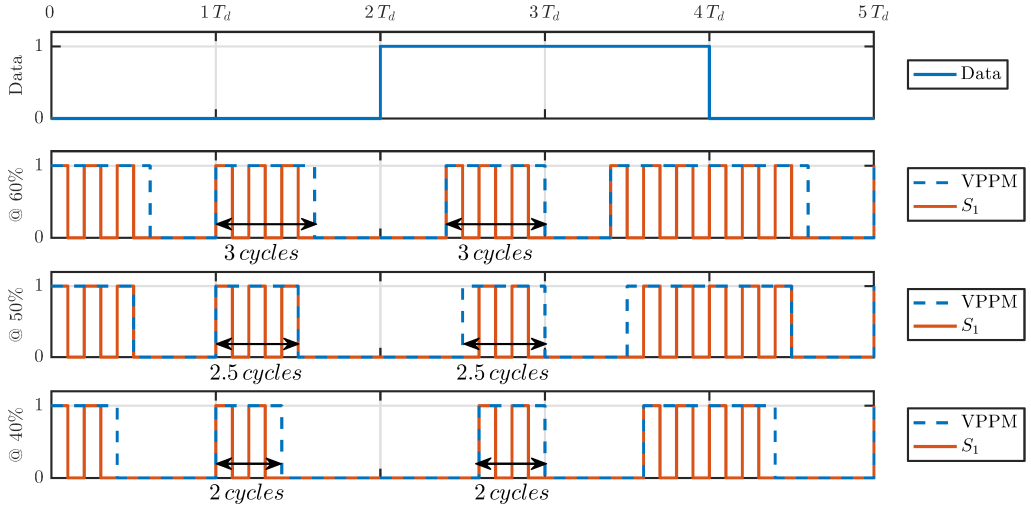
3.2.2 Step 1 - VLC Dimming Resolution vs. Transmission Rate trade-off

The ratio between data frequency and converter switching frequency gives an integer value that represents the amount of high-frequency pulses fitting in a single data period. This factor represents the inverse of the dimming resolution ($\Delta_{dim} = f_d/f_s$) achieved by the transmitter while still preserving DCM.

A dimming resolution of up to 20 % was chosen, making it possible to transmit data at a rate of 1/5 of the switching frequency. With switching frequency reaching up to $500\,kHz$, a transmission rate of $100kbps$ is expected. However, it is also possible to improve dimming resolution (i.e., reduce its value) with a data transmission rate trade-off, such that transmissions of $50kpbs$ are possible for intermediate brightness levels intervals of 10 %.

Figure 50 displays a VPPM modulation example for the 20 % dimming resolution. As can be seen, both 60 % and 40 % brightness levels work as expected, where at 50 % a bit asymmetry can be seen. At these half resolutions, dimming can be achieved by 'transmitting' a signal with equal numbers of '0's and '1's, but realistic data transmission cannot be performed due to the possibility of flicker. Additionally, an integer number of switching cycles inside a data period is required for the proper operation of the circuit, once neither charge or discharge of the energy-storing elements can be stopped by the active switches within one switching cycle.

Figure 50 – Data modulation examples for a bitstream of [00110] for three different brightness levels and respective switching signals for switch S_1.



Source: Author (2020).

3.2.3 Step 2 - Power Corrections

In order to ensure data transmission at the LED's nominal power, a power correction is required for the converter design such that nominal LED conditions are achieved for minimum dimming. These corrections are shown in (3.8) assuming the LED's nominal power must be processed for the converter operating at 90% of its maximum power.

$$\begin{cases} I_o = \frac{0.5\,A}{0.9} & \rightarrow I_o = 0.556\,A \\ V_o = V_t + r_d\,I_o & \rightarrow V_o = 20.662\,V \\ P_{max} = I_o\,V_o & \rightarrow P_{max} = 11.476\,W \\ G = \frac{V_o}{V_{in}} & \rightarrow G = 0.43 \end{cases} \tag{3.8}$$

3.2.4 Step 3 - Switched Capacitor Selection

With switching frequency set as $f_s = 500\,kHz$ and output power set at $P_{max} = 11.476\,W$, (3.7) can be used in order to find the required capacitance of the switched capacitor C_s through (3.9).

$$C_s = \frac{P_{max}}{f_s\,V_{in}^2} = \frac{11.476\,W}{500\,kHz\,(48\,V)^2} \rightarrow C_s = 9.964nF \tag{3.9}$$

An arrangement of three $3.3\,nF$ parallel-connected capacitors is then chosen in order to properly divide the circulating current and reduce possible heating of the switched capacitor C_s. It must be remarked that when no commercial value of capacitance is found, switching frequency cannot be changed without altering the data rate transmission, and these three initial steps must be simultaneously fine-tuned. Having found a relatively

acceptable capacitance value through commercial capacitor arrangements, the design can be proceeded.

3.2.5 Step 4 - Output Capacitor Selection

The selection of the output capacitor C_o will directly affect the fall-time of the VPPM modulation, which should be observed according to (3.1). The worst-case scenario occurs while sending the two subsequent high bits '1's during minimum dimming, where a larger fall-time of the first bit could cause the erroneous detection of the second bit as a zero. During minimum dimming, a delay of one switching period is expected between the ending of stage 6 of the first bit and the beginning of stage 1 for the second. Therefore, it is reasonable to expect a detector that samples around the data period edge at a distance of half a switching cycle, which would be an appropriate delay time for the converter to turn off. Additionally, by having the fall-time to be a fraction of the worst-case distance between two pulses assures complete discharge of the output capacitor C_o down to the LED threshold voltage before the next pulse rise, as expected in the analysis section. With that assumption, the output capacitor C_o can be chosen by selecting the capacitance value that causes the current to reach a factor k_f of its nominal value at the required time. This capacitance is described as

$$C_o = \frac{1}{2\, f_s\, r_d}\, \frac{1}{ln(k_f^{-1})}. \tag{3.10}$$

However, the output capacitance C_o will also directly affect the output voltage and current high-frequency ripples, such that blindly selecting a capacitor for a given fall-time without considering these effects can be detrimental to the LED's photometrical performance. In order to calculate the output voltage ripple, it is required an integration of the output capacitor current waveform in order to estimate charge accumulation at the output capacitor C_o according to (3.11).

$$Q_o = \int_{t_a}^{t_1} \left[i_{L\,stage1}(t) - I_L \right] dt + \int_{t_1}^{t_b} \left[i_{L\,stage2}(t) - I_L \right] dt \tag{3.11}$$

Where t_a and t_b are the crossing points where the output capacitor current waveform touches zero, given by (3.12).

$$\begin{cases} t_a = \dfrac{1}{\omega_o}\, asin\left[\dfrac{f_s}{\omega_o} \dfrac{1}{G\,(G-1)} \right] \\ t_b = \dfrac{1}{\omega_o}\, acos\left(\dfrac{G}{G-1} \right) - \dfrac{f_s}{\omega_o^2\, G} + \dfrac{\sqrt{1-2\,G}}{\omega_o\, G} \end{cases} \tag{3.12}$$

As can be seen, a value for resonant frequency ω_o is required for these calculations, which cannot be determined once the inductor was not selected at that point. However, it will be desired to select an inductance value such that the converter operates near

the DCM limits in order to reduce the maximum current peak value. Therefore, a fair estimation is to use the limit resonant frequency value given in (2.44).

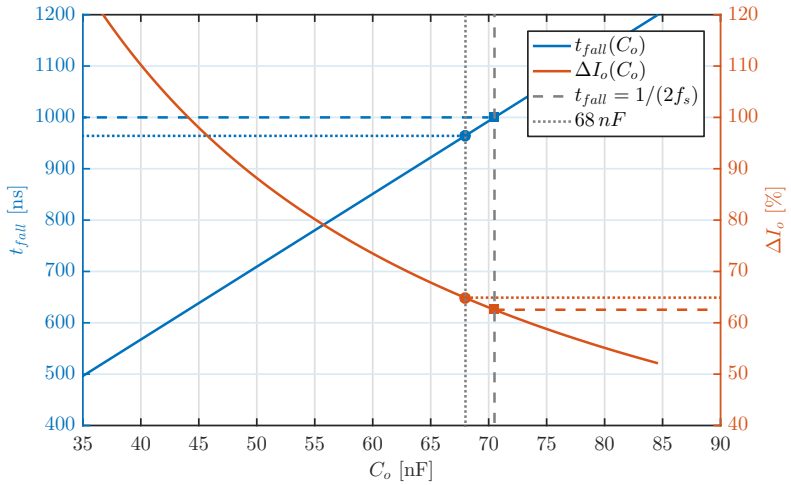
Once the output capacitor C_o charge has been calculated, the LED current ripple can be given by (3.13).

$$\Delta I_o = \frac{Q_o}{r_d\, C_o} \tag{3.13}$$

The relation between output capacitor C_o, current ripple ΔI_o and fall-time are graphically shown in Figure 51. The time delay is calculated considering the time that the voltage reaches $k_f = 0.1$ times its nominal value. As can be seen, smaller values of capacitance lead to shorter fall-times, at the cost of increased current ripple. Using the parameter of t_{fall} as half the switching period and choosing the next commercially available capacitor ($C_o = 68\,nF$) lead to a current ripple of $\Delta I_o = 361mA$ with a fall-time of $t_{fall} = 964\,ns$.

Choosing the next commercially available capacitor assures that the output current ripple is at its minimum, allowing the converter to operate according to the assumption made in the analysis section of nearly-constant output voltage. For instance, with the current variation found, the output voltage variation can be calculated through $\Delta V_o = \Delta I_o\, r_d$, which yields around $2.18\,V$ or a $11\,\%$ variation relative to the nominal voltage. Furthermore, it can be seen that the choice of maximum possible capacitance also increases the robustness of the system by stopping the output current ripple to be too significant to the point of crossing the light flux threshold that would indicate an erroneous pulse absence at the receptor. Otherwise, it would be required of the receptor to filter out short valley pulses.

Figure 51 – Output capacitor C_o influence in t_{fall} and ΔI_o.



Source: Author (2020).

It is important to remember that although the output current ripple seems to be

excessive (around 65 % of the nominal current), the light modulation standard for this order of frequency is rather broad (IEEE STANDARDS, 2015). For instance, a light modulation of 100 % is allowed by around $1.2\,kHz$, enabling the PBT modulations with embedded dimming for higher frequencies. For instance, in this example VPPM is achieved at $f_d = 100\,kHz$ and $f_d = 50\,kHz$, far above the limit. Around the switching frequency of $f_s = 500\,kHz$, not only the limit would be higher, but also the light modulation would be smaller, meaning that for the output capacitor C_o itself, a design focused on response time is adequate.

3.2.6 Step 5 - Inductor Selection

The inductance selection must be trifold: it must consider the inductor effects on the rising time, on the inductor current ripple and must be limited to a maximum value in order to assure DCM operation.

Once again, these relations can be displayed graphically. In order to describe the effect of the inductance at the rising time, the calculation provided in (3.4) must be solved numerically for t_{rise} such that $i_o(t_{rise}) = k_r\, I_o$. This relation shows that the rising time is affected by every single reactive element in the circuit. However, once both capacitors are more closely related to different variables, it is desired to considered them constants, while inductance value can be chosen in order to tune rise time.

In the meantime, the relation between inductance and peak inductor current can be found at time instant t where current value in (2.11) reaches maximum value. This calculation can be described by

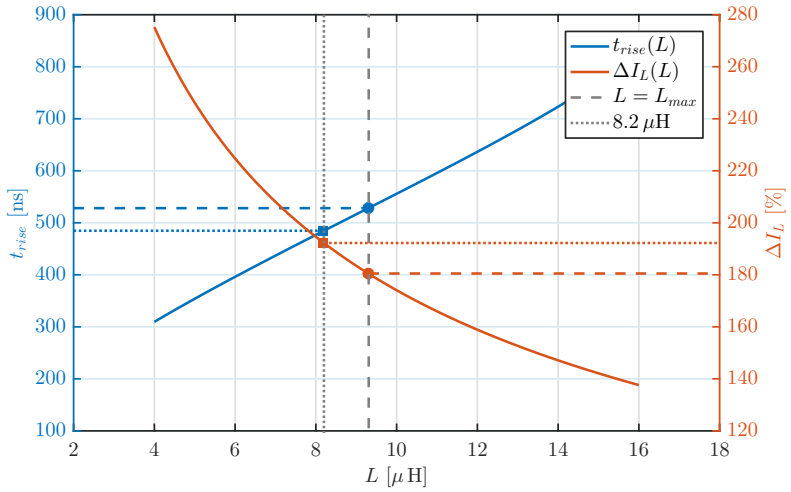
$$\Delta I_L = \frac{\sqrt{L\,C_s}}{L}\,(V_{in} - V_t). \tag{3.14}$$

Finally, the maximum limit of inductance is described according to the definition of ω_0 and (2.44), resulting in

$$L_{max} = \frac{1}{\omega_0^2\,C_s} \rightarrow L_{max} = 9.31\,\mu H. \tag{3.15}$$

The comparison between the three relations are displayed in Figure 52, where the rise time is calculated as the delay it takes the current to reach $k_r = 0.9$ times the nominal current. As can be seen, the calculation of rise time fails for smaller ranges, but is still valid for a significant range. Nevertheless, it can be seen that just by the DCM limitation, the choice of the inductor already produces a rise time significantly smaller than fall-times and should not produce any sampling problem even in worst case scenario. Finally, the inductor of choice is $L = 8.2\mu\,H$, the next commercially available inductor smaller than the DCM limit (3.15). The rise time expected is $t_{rise} = 484\,ns$ whereas the inductor peak current is $\Delta I_L = 0.968\,A$.

Figure 52 – Inductor influence in t_{rise} and ΔI_L.



Source: Author (2020).

3.3 SIMULATED VALIDATION

The results of the design process are summarized in Table 10. A simulation is used to validate the design process according to the expected values of current and switching times.

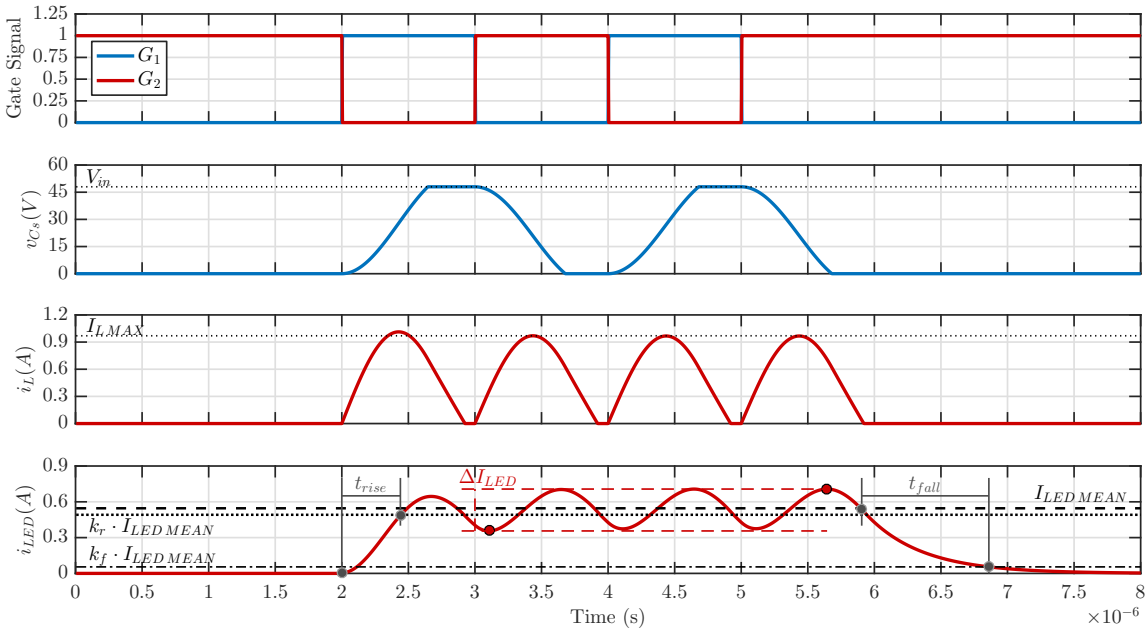
Table 10 – RSC buck converter design.

Source and Load		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Output Current	I_s	$0.552\,A$
Output Power	P_o	$11.405\,W$
Switching Frequency	f_s	$500\,kHz$

Source: Author (2020).

The simulation result is plotted in Figure 53. The average LED current was numerically calculated between a integer amount of of cycles discounting the first, as to guarantee steady state. The value found was $I_{o\,nom} = 0.5457\,A$. Using the arbitrary $k_f = 0.1$ and $k_r = 0.9$ factors it was calculates the thresholds of the switching times, enabling measurement of t_{fall} and t_{rise} respectively.

Figure 53 – Simulation plotted results for design validation.



Source: Author (2020).

The relevant values for the design process are summed in Table 11. As can be seen, the design resulted in desired operation of the converter, with the calculations yielding accurate results.

Table 11 – Simulated validation of RSC buck converter design.

Switching times:		**Simulated**	**Expected**
Rise Time	t_r	$440.0\,ns$	$484.3\,ns$
Fall Time	t_f	$955.0\,ns$	$964.5\,ns$
Current Variations:		**Simulated**	**Expected**
Inductor Peak Current	ΔI_L	$0.970\,A$	$0.968\,A$
LED Current Ripple	ΔI_{led}	$0.351\,A$	$0.361\,A$

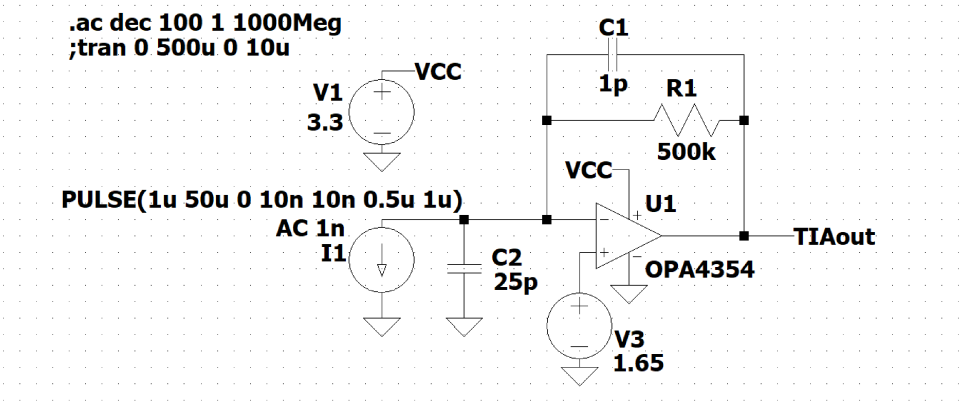
Source: Author (2020).

3.3.1 Receiver

The receiver is composed by a BPW34 photodiode and dual operational amplifier OPA2354 which implements a transimpedance amplifier (TIA) and a non-inverting hystersis comparator. The TIA will convert the photocurrent into a voltage signal, adding an offset V_{off} controlled by a potentiometer. This offset exists in order to regulate the voltage signal in order to compensate for ambient light, allowing a positioning of the analog output at an appropriate level for the comparator to respond sensibly. A total capacitance of $1\,pF$ between the output and the inverting input of the TIA was used for bandwidth limitation.

In order to validate the TIA as a low-pass filter, a LTspice XVII simulation was performed. The simulated circuit can be seen in Figure 54, built with the OPAx354 SPICE model provided by manufacturer. The photo-diode is modelled as a pulsed current source with a 50 μA current peak, in accordance to the BPW34 photodiode datasheet.

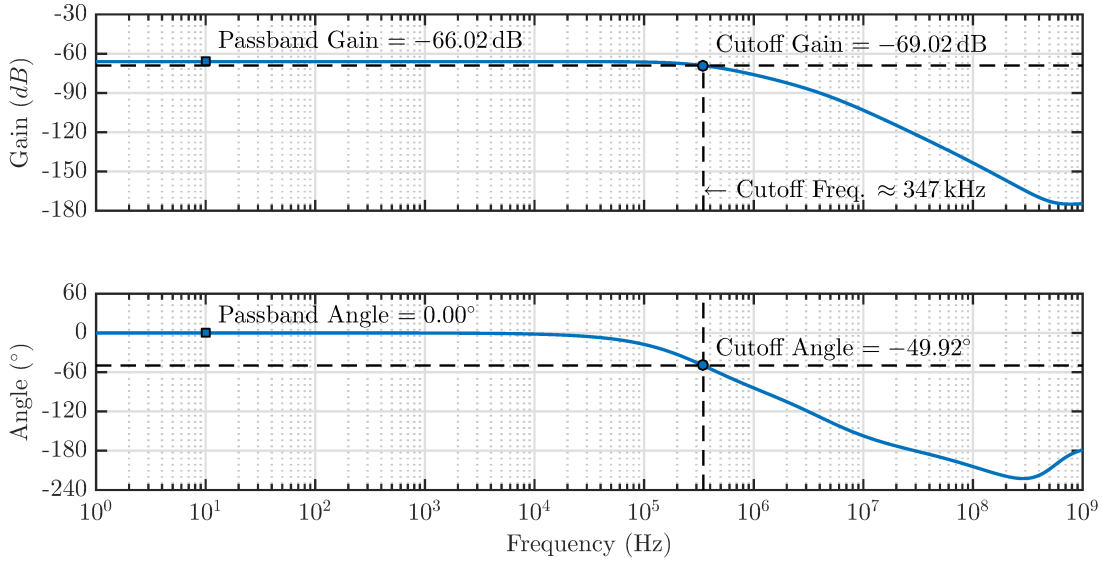
Figure 54 – LTspice circuit for the TIA simulation.



Source: Author (2020).

The LTspice simulation allows for the small-signal ac analysis of the circuit, resulting in the bode plot of at the *TIAout* node as shown in Figure 55. The results show a cutoff frequency of a proximately 350 kHz.

Figure 55 – LTspice simulation for the ac analysis at the *TIAout* node.



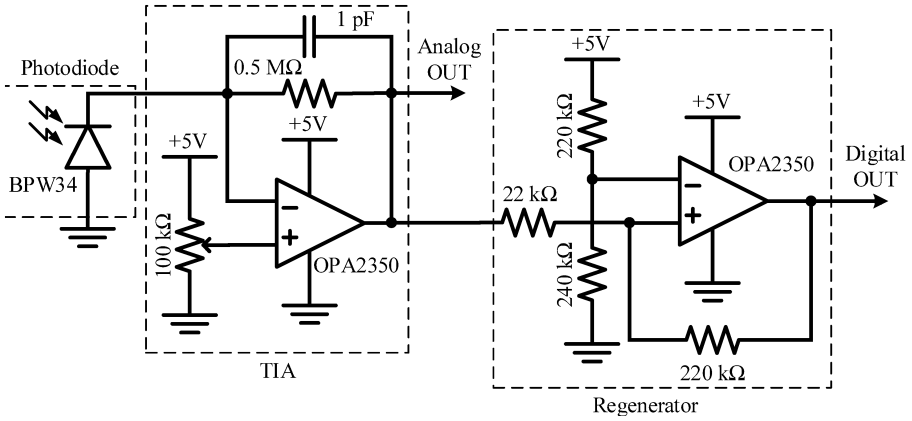
Source: Author (2020).

Thus, the TIA serves three purposes: to convert current values from the photodiode to an amplified voltage value, to filter high-frequency noise and to counteract possible ambient light through the potentiometer, adjusting the bias level of the comparator. This adjusts the received signal to be properly inserted at a hysteresis comparator. This comparator presents a constant-value threshold, such that the output for this circuit is

high whenever the input is above the threshold and low whenever the input is below the threshold. To perform as such, the comparator is assembled as an amplifier with positive feedback, which characterizes a regenerator.

As a result, the VLC receiver presents an intermediate analog output, which is proportional to the received light, and a final digital output that describes the received light in states of 'on' and 'off' depending on the instantaneous amplitude. The simplified schematics is shown in Figure 56.

Figure 56 – VLC receiver schematics.



Source: Author (2020).

3.4 CODES

A TIVA C Series TM4C123G was used in order to synthesize the required PWM signals for the transmitter, as well as controlling the instants where such signal were enabled according to the transmitted data. The microcontroller receives the transmitted data through packages of 512 bytes by its UART, connected to a MATLAB function. The code at the microcontroller could operate in two different modes: continuously looping the transmitted signal or through a single-shot transmission. The first mode is useful for efficiency testing, where data must be transmitted continuously for a sufficiently high timespan that allows the LED to reach steady-state burst mode. On the other hand, the one-shot transmission is used to evaluate bit error rate (BER), where a limited amount of bits is required. The complete code programmed at the TIVA microcontroller is shown at Appendix B. Since it is rather large to be inserted during this text, exerts of it will be shown instead in order to allow a further explaining of its workings.

For the evaluation of the BER, the output of the receiver was observed by an oscilloscope measuring a window sufficiently high to detect an entire package transmitted. A MATLAB code was developed to decode the modulated output, thus allowing for the data to be compared.

This section details the codes used for the modulation and for the demodulation of the data.

3.4.1 Transmitter

The RSC converter must operate in constant frequency and duty ratio, such that the output power (and thus brightness level) can be limited solely by the data modulation. However, the transmission rate can be changed through a multiplying factor ''M', that effectively controls the number of high-frequency switching cycles are comprised in a single data period. A MATLAB code was written in order to alter this data transmission rate in real time through the UART. The code is an adaptation of a previously existing code available at the laboratory, and thus, additionally contains an unused feature of duty-ratio variation as well. This code is shown in Listing 3.1.

Listing 3.1 – MATLAB code for transfer rate variation through UART.

```
function serial_dim_VPPM(M,d)
% Initiates serial communication
s = serial('COM12', 'BaudRate', 115200);
fopen(s)
% Hold-and-wait code:
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plots random image
scrsz = get(0,'ScreenSize');
f = figure('Position', [.25*scrsz(1) .25*scrsz(2) .25*scrsz(3) .25*scrsz(4)]);
polar(2*pi*rand(5,500),rand(5,500));
% Waits confirmatory key press:
disp('Pressione SPACE para enviar, SW1 para resetar');
waitforbuttonpress
close(f);
workspace
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Stores M and duty into x variable
x = ['M = ',num2str(M),', d = ',num2str(d),'%'];
% Translate x into single string:
x = sprintf('M%03dD%03d',M,d*10);
% Send x string to serial:
fprintf(s,x);
% Stop serial communication
disp('------------------------ Fim');
stopasync(s); close(s); delete(s); clear s;
```

Similarly, a MATLAB function was developed in order to transmit data packages to the microcontroller, as explicit in Listing 3.2. This function loads a preexisting data vector previously-saved into a *'.mat'* file, concatenating it with symbols to be interpreted by the TIVA code.

Listing 3.2 – MATLAB code for transfering data to TIVA through UART.

```
function DATA_SEND(TRANSFER_TIVA_PORT,TRANSFER_FILE_DATA,ONESHOT);
% Initiates serial communication
s = serial(TRANSFER_TIVA_PORT, 'BaudRate', 115200);
fopen(s)
% Load Data from file
data = load(TRANSFER_FILE_DATA);
DATA = sprintf(num2str(data.transf'));
if ONESHOT == 1
   % Upper case 'S' leads to a hard-stop: one-shot transmission
   DATA = ['T' DATA 'S']
else
   % Lower case 's' leads to a soft-stop: looped transmission
   DATA = ['T' DATA 's']
end
for it=1:max(size(DATA));
   fprintf(s,DATA(it)); % Send 'DATA' string to serial
end
% Stop serial communication
disp('------------------------- Fim');
stopasync(s); close(s); delete(s); clear s;
```

As can be seen, the philosophy of this communication is to use a single UART channel to send different types of information, symbolizing the nature of each data by a letter that will allow for the TIVA code to translate it. For instance, letters 'M' and 'D' shown in Listing 3.1 indicates for the microcontroller that the information received are related to the frequency multiplying factor and duty ratio respectively. In Listing 3.2, the 'T' symbol indicates that data to be received is the transmission data. Additionally, the upper case 'S' and lower case 's' symbols indicate whether the microcontroller should transmit this information a single time or continuously looped. An additional MATLAB function was developed in order to send a single 'Z' symbol to the microcontroller, indicating that it must clear its transmission data vector by replacing every cell with a zero.

The excerpt of the TIVA code that receives the UART data from MATLAB can be seen on Appendix B between lines 347 and 451. The interrupt handler *UART0IntHandler* detects when the computer is transmitting data to the microcontroller. The first character is saved in an auxiliary variable that goes through a sorting *switch/case* logic that deals with each data accordingly, allowing a single UART channel to be used for several functions. Among them, the data transmitted is received through the UART as a string starting with a character 'T' and ending with either characters 'S' or 's', symbolizing respectively the begging end end of the package. This data string to be transmitted is then stored in a variable called $DATA\_VPPM$.

After this data is received, the main section of the code, responsible for the data

modulation, is set to start. The flag $STOP\_FLAG$ is set to zero, allowing the code to run. At the same time, the interrupts for the PWM and the TIMER modules are enabled. The whole modulation logic of the code is performed by these two interrupts, while the infinite loop remains blank. As the desired switching frequency rises, the computational time spent at each interrupt is increasingly more relevant, and as such, the goal is for the Interrupt logics to spend the least amount of computational effort as possible.

The TIMER module is set to reset after the equivalent of one transfer period, with one interrupt at the end of each cycle. The higher-frequency PWM module is set to a frequency M times higher, with its interrupt at the end of each cycle. At first, the code initiated with nominal transfer rate ($f_d = 100\,kbps$, i.e., $M = 5$) and lowest available dimming. This values can be seen in lines 60 and 61 on Listing B.1 at Appendix B. The resulted logic is based on counting the integer number of high-frequency switching cycles that occur at a given transfer period.

When sending bit '0', the total of high-frequency PWM pulses transmitted at the beginning of the transmission period is the total number of cycles times the VLC dimming, rounding up. On the other hand, the code should round down the number of high-frequency PWM pulses it should send at the end of the data transfer period when sending the bit '1'. This calculation can be seen on lines 121 and 122 of Listing B.1. The same calculation is performed whenever there is a change in M of VLC Dimming, as shown in lines 438 and 439 of Listing B.1.

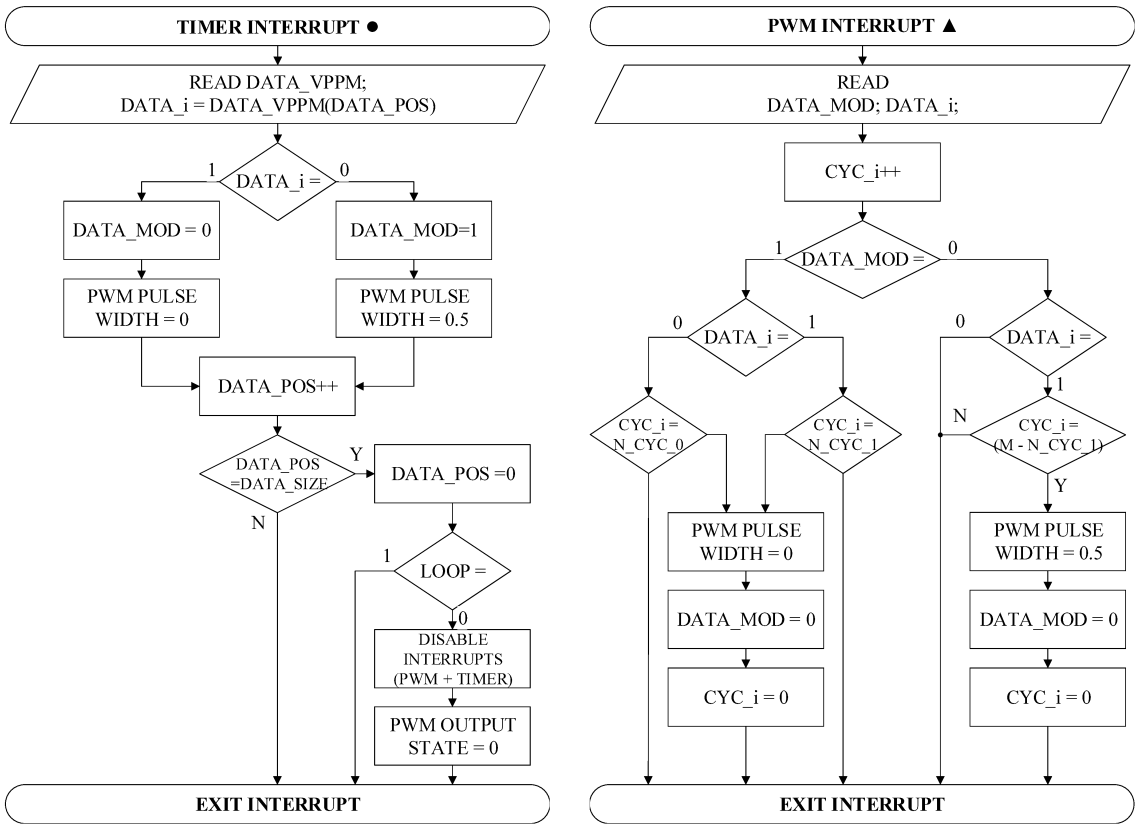
Data will start being transmitted after the UART detects that information string has been received, storing it at the $DATA\_VPPM$ vector. The TIMER interrupt is responsible for starting a new bit transfer, by detecting the next-available data ($DATA\_i = DATA\_VPPM(DATA\_POS)$) and starting the modulation properly: if the next bit to be transfered is zero, the VPPM modulation starts in high state ($DATA\_MOD = 1$) and the PWMs are active. On the other hand, if the next bit to be transfered is one, the modulation starts in low state ($DATA\_MOD = 0$) the PWMs are deactivated. Note however that even in low state, the PWM interrupt must continue counting the cycles, and thus, deactivation is not performed by disabling the PWM module. Instead, deactivation is performed simply by setting the high-frequency PWM duty ratio to zero. This effectively deactivates the PWM while allowing its interrupt function to continue working.

As the TIMER Interrupt Handler is responsible for starting the modulation for each data transfer period, the PWM Interrupt Handler is responsible for changing its state by counting the amount of integer high-frequency cycles must occur before $DATA\_MOD$ is changed. At the end of each PWM cycle, the interrupt counter increments in one, and by reaching the number of cycles it must stay at the initial state, it changes accordingly.

The TIMER Interrupt Handler can be read on lines 228 to 267 at Listing B.1, where the PWM Interrupt Handler can be read on lines 269 to 308 of Listing B.1. Likewise,

the codes are graphically described by Figures 57a and 57b respectively.

Figure 57 – Logic workflow for the (a) TIMER Interrupt and (b) PWM Interrupt implemented at the TIVA microcontroller for VPPM modulation.



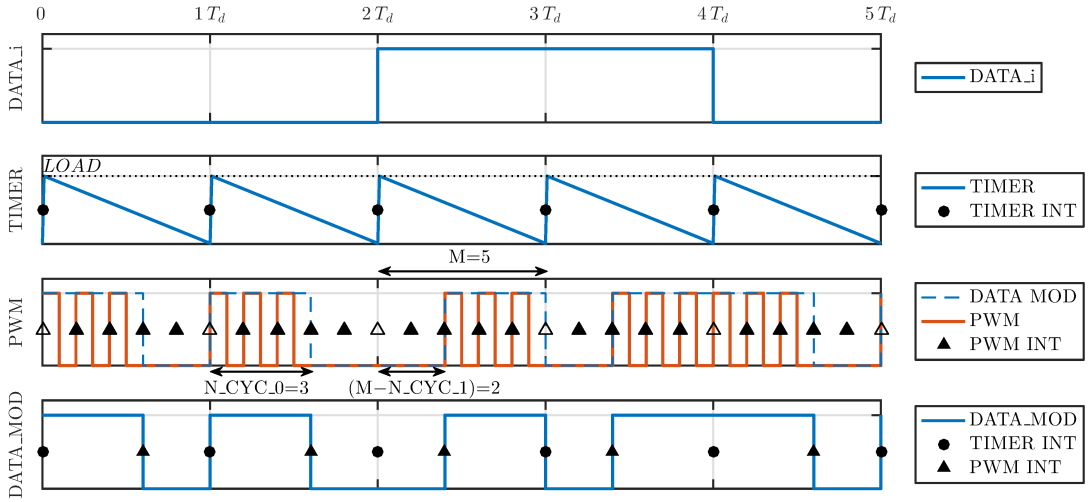
Source: Author (2020).

An example of the working interrupt logic can be seen on Figure 58, where transmission rate is 5 times the switching frequency ($M = 5$), meaning that 5 high-frequency PWM cycles occur in a given transmission period. The TIMER module is programmed with a LOAD value such that its period is the transmission rate period, and an interrupt occurs at every TIMEOUT event, as symbolized by the bullet (•) symbol. Meanwhile, the PWM module is set to a frequency 5 times higher, with its interrupt (▲) occurring at the end of each cycle. At 60% dimming, the high state in each transmission cycle presents $5 * 0.6 = 3$ cycles. It is clearly shown, therefore, that the DATA_MOD signal is initialized during the TIMER interrupt (•), having its value changed during a specific PWM interrupt (▲) after an appropriate number of cycles.

A noteworthy point is that the TIMER interrupt always occurs, relatively speaking, at the same instant as a PWM interrupt. As the TIMER interrupt effectively resets the PWM signal and its cycle counter, this PWM interrupt (△) is not counted and could almost be suppressed from representation, once they do not affect the work flow of the code. However, these specific PWM interrupts (△) have an important effect exclusively when transmitting the '1' bit because they force the PWM to stop after the required

number of cycles. This feature was shown to be crucial during experimentation because when the converter were to wait for the TIMER interrupt, a small delay in it would cause the code to supply an additional PWM pulse. Albeit narrower due to the sudden interruption by the TIMER interrupt, it was often sufficient to supply charge to the switched capacitor, prolonging the ON period and affecting VLC dimming and data transmission. This interrupt, therefore, remains uncounted as desired but must be taken into account nonetheless as a hard-stop when transmitting the '1' bit.

Figure 58 – Modulating logic for transmitting the [00110] bitstream for VLC dimming of 60%.



Source: Author (2020).

3.4.2 Receiver

The data reception was realized with the receptor circuit through its digital output being measured with an oscilloscope. Due to processing limitations of the TIVA, an offline demodulation was chosen, where the data collected through the oscilloscope was treated by a MATLAB code in order to interpret the information transmitted. The code is divided in Listings 3.3, 3.4 and 3.5 for clarity. The first section, shown in Listing 3.3 treats with the initial data load, that reads the transmitted data stores in a '.mat' file as well as the oscilloscope acquisition in '.csv'. The data frequency and VLC dimming of the measurement in question must be added manually for demodulation purposes. Additionally, an auxiliary variable 'desloc' was shown to be useful for manual adjustments in data treatment.

Additionally, important variables must be initiated before the actual demodulation. The received data 'rec_data' goes through a regeneration process to clear possible analog noise, turning into an truly binary data stream. The 'clock' signal and 'cnt' counter are also initiated, alongside the variable 'CNT_SAMPLE' that detects the position inside the data period for proper sampling according to the VLC dimming and transfer rate.

Listing 3.3 – Demodulation code: data loading and variable initializing.

```
1  %Demodulador offline
2  close all;clear all;clc;
3  %% Data loaing
4  load_data = 1; %1 for loading new data, 0 for using pre-loaded data (faster)
5  deloc=1;       % Manual adjustment
6  tek='0107';    % Oscillocope file number
7  VLC_dim=0.4;   % VLC Dimming used experiment
8  fsig = 100e3;  % Signal frequency (100kbps or 50 kbps)
9  path = pwd;    % path main oscilloscope files:
10 % loads data:
11 if load_data
12     path_sent = [path '\Transf_Data_rand.mat'];
13     path_rec = [path '\dados2\tek', tek, 'ALL.csv'];
14     load(path_sent);
15     data_sent = transf;       % .mat data sent to TIVA through UART
16     M = csvread(path_rec,21,0); t=M(:,1);
17     rec_data = M(:,2);        % oscilloscope reading from receiver output
18     save('data_to_process.mat','t', 'data_sent','rec_data');
19 else
20     load('data_to_process.mat');
21 end
22 %% Pre-processing of data entry
23 rec_data = rec_data > 1.65;          % Regenaration threshold for received data
24 ts = t(2)-t(1);                      % Oscilloscope sampling period calculation
25 clock = zeros(size(t,1),1);          % Initializing clock variable
26 fclk = fsig;                         % VPPM signal / sampling frequency
27 D = VLC_dim;                         % Data duty ratio
28 CNT_SAMPLE = round((((1-D)/2)/fclk)/ts);% Sampling position in data period
29 CNT = CNT_SAMPLE+1;                  % Initializing count above threshold
30 count = zeros(size(t));              % Storing cnt values for plotting
31 NumEdgesInit = 4;                    % Number of edges before enabling clock
32 rising_edge = 0;                     % Number of rising edges on singal
33 rec = zeros(1,NumEdgesInit+deloc);   % Vetor with demodulated data
34 tdetc = zeros(1,NumEdgesInit+deloc); % Vetor with instants of demodulated data
```

In order to initiate the clock, a stream of zeros must be received, allowing for the calculation of the data transfer rate that is used to create a clock of the same frequency. The amount of expected zeros is described by the 'NumEdgesInit' variable. The demodulation loop highlighted in Listing 3.4 analyses the oscilloscope data chronologically counting the rising edges and storing the time instant where the clock is initiated in line 44. The clock in initiated in line 49.

Once the clock is initiated, its own rising edges are detected in line 54, used to reset the counter 'ÇNT'. Once this variable increases at every loop (line 65), it represents essentially a delay between rising edge and sampling instant. Once this variable reaches de expected delay (calculated in line 28), the sampling can occur.

Listing 3.4 – Demodulation code: main sampling loop.

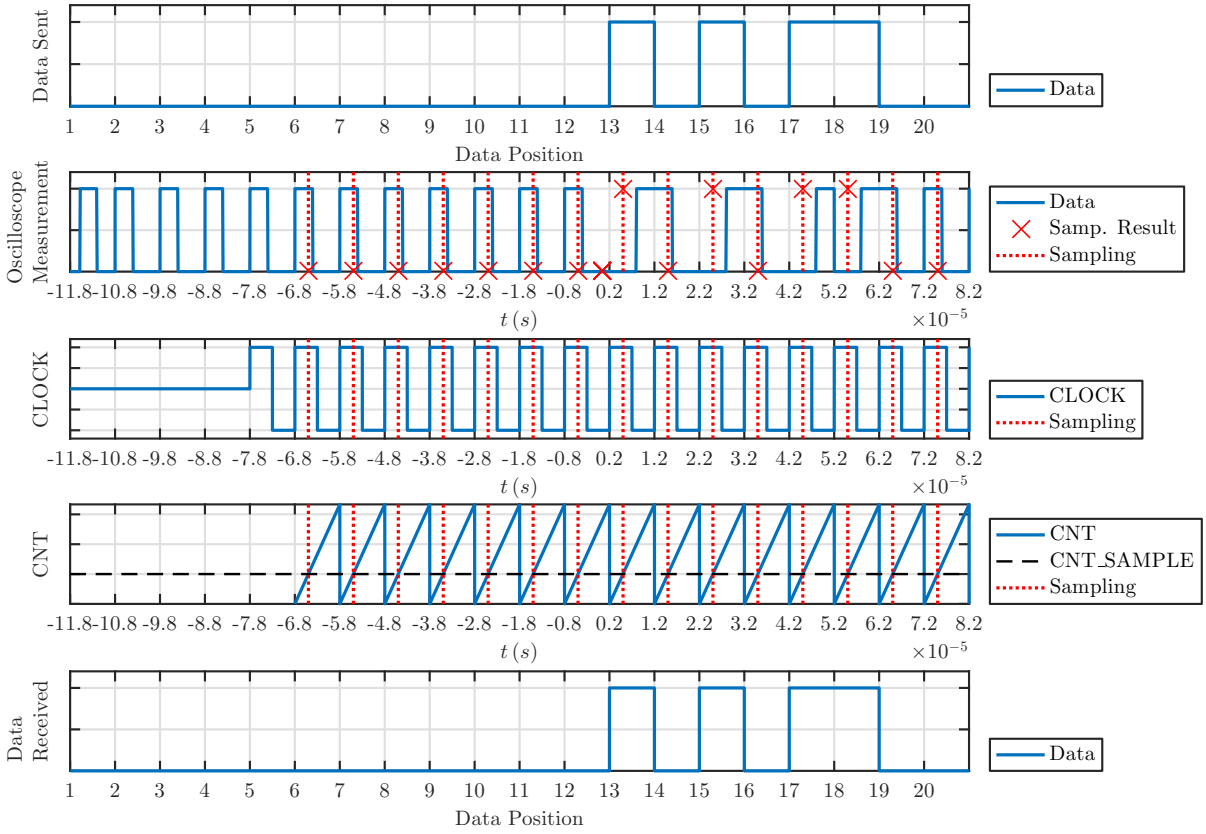
```
35 %% Demodulation Loop
36 for i=2:size(t,1)-1
37     %Detecting rising edges in signal
38     if(rec_data(i+1)==1&&rec_data(i)==0)
39         rising_edge = rising_edge+1;
40         tr = t(i);     %storing the time instant where rising edge is detected
41         if (rising_edge==2)
42             first_edge = tr;
43         elseif(rising_edge==NumEdgesInit+1)
44             ti = t(i); % instant where clock is initiated
45         end
46     end
47     % Waits 'NumEgesInit' rising edges before initating clock
48     if(rising_edge>NumEdgesInit)
49         clock(i) = 1*sign(sin(2*pi*fclk*(t(i)-ti))); %calculates clock
50     else
51         clock(i) = 0;
52     end
53     % Detects rising edges of clock singal
54     if(clock(i)==1&&clock(i-1)==-1)
55         CNT = 0;   % resets counter
56     end
57     % Sampling procedure
58     if(CNT==CNT_SAMPLE)   % Waits for approprate sampling instant
59         rec(length(rec)+1) = ~rec_data(i); % demodulates signal
60         tdetc(length(tdetc)+1) = t(i);   % sampling instant
61         if(rec(end)==0 && rec(end-1)==0 && rec(end-2)==0 && rec(end-3)==0)
62             ti = tr;   % resets clock after 4 consecutives zeros
63         end
64     end
65     CNT = CNT+1; count(i)=CNT;
66 end
```

The sampling logic, initiated in line 58, is straightforward: once the sampling always occurs by detecting the initial value of the signal in each transfer period, it only requires a value inversion of the sampled value. For the VPPM modulation, when the pulse is positioned at the beginning of the data transfer period, the sampled value is high, where the bit transmitted is '0'. Likewise, when the pulse is positioned at the end of the data transfer period it meant he transmitted bit is '1' but the sampled data is low. Therefore, an inversion of the sampled value correctly represents the transmitted bit.

The work flow of the code is exemplified in Figure 59. The transmitted data is shown, being initiated with a high number of zeros and followed by a string pseudo-randomly generated data. The digital output of the receiver is collected by an oscilloscope, displayed below. As can be seen, the pulse is properly positioned at the beginning of a

transfer period when transmitting ‘0’ and at the end of a transfer period when transmitting ‘1’. The sampling instant is shown, and the sampling result can be seen as an inversion of the data read at the sampling instant.

Figure 59 – Demodulation code work flow example.



Source: Author (2020).

The clock signal is also noted, with the correct frequency calculated and being properly initiated after ‘NumEdgesInit=4’ data cycles. The counter, initiated beyond its threshold value ‘CNT_SAMPLE’ in line 28, only enters the sample procedure initiated in line 57 after is reset in the first rising edge of the clock. Thus, a number of ‘NumEdgesInit+1=5’ bits have been lost before sampling. This data is predicted while initiating the sampled vector in lines 33 and 34, and can be seen as a Sample Result outside a sampling instant at $t = 0$ at the second row of the plot. After the counter is reset, a sampling instant is flagged whenever the ‘CNT’ variable reaches its threshold. The final result of the demodulation can be seeing the last row in Figure 59, containing the ‘NumEdgesInit+1=5’ bits ‘0’ missed by the sampling process, but predicted, followed by the sampled values.

Finally, Listing 3.5 prints the result, automatically detecting the BER and the error amount and positions.

Listing 3.5 – Demodulation code: printing results.

```
67 %% Prints result
68 fprintf('RESULT: BER\r\nBER = %.2f %%
       \r\n',100*sum(xor(data_sent,rec(1:length(data_sent))))/length(data_sent));
69 error_positions = find(xor(data_sent,rec(1:length(data_sent))));
70 if(~isempty(error_positions))
71     fprintf('First error at position : %d \r',error_positions(1));
72     fprintf('Total number of errors : %d \r\n',length(error_positions));
73 else
74     fprintf('There were no errors in transmission!\r\n');
75 end
```

3.5 PARTIAL CONCLUSIONS

This chapter aimed into describing a proposed VLC system operating with a RSC buck converter and VPPM modulation. Following the circuit description shown in Section 2.1, the element selection was proposed based on the influence of the then simplified output loop. With the proposed element selection, the turn-on and -off times of the circuit were accounted, presenting acceptable value in order to justify the exclusion of the auxiliary VLC output switch.

With the selected components, a prototype was built. Using GaN-FETs as active switches and Schottky diodes, a prototype operating in $500\,kHz$ was achieved, allowing up to $100\,kbps$ transfer rates and a density of $1.43\,kW/dm^3$. The PWM was generated through a TIVA C Series TM4C123G microcontroller, also responsible for modulating such PWM signal for data transfer in VPPM mode. The codes responsible for UART communication and data modulation were detailed in this chapter, alongise the code used for offline demodulation.

It should be noted that VPPM modulation was chosen due to its simplicity in data transmission, since this modulation does not require a compensation symbol. However, an unforeseen challenge was presented in the detection and demodulation of such signal, whose sampling must occur at very specific instants of the data transfer period. A simpler modulation whose sampling can be tied with the actual rising edge of the signal would be preferred.

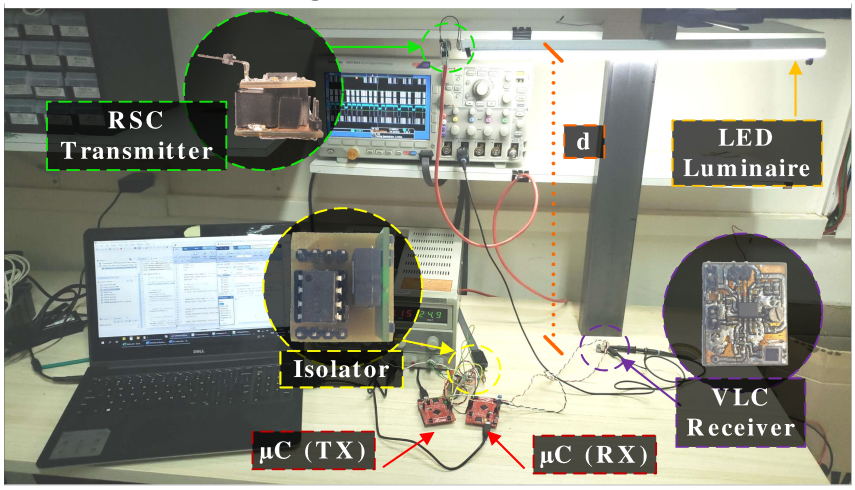
4 EXPERIMENTAL RESULTS

In order to validate the proposed design an experiment was developed. This section discusses this setup alongside the achieved results.

4.1 EXPERIMENTAL SETUP

The experiment was set up with the luminaire at a distance d of $1\,m$ above the receiver. A picture of the set up can be seen in Figure 60. The power converter was located immediately at the back of the luminaire, being connected to the signal isolation stage by a $3\,m$ long Cat 5 cable with 4 twisted pairs, with known inductance of $525\,nH/m$. The $5\,V$ and PWM signal wires were each braided with a wire grounded in both ends. The last remaining pair was used for the $48\,V$ required for the power stage supply.

Figure 60 – Experimental setup for the VLC system with highlighted main boards.



Source: Author (2020).

In order to evaluate experimentally the operation of the converter, a prototype was built to drive a commercial tubular LED lamp comprised of 24 parallel arrays of 6 LEDs in series each. The individual LED chips are Nichia NESW146AT, as stated by the manufacturer. The results of the design process are summarized in Table 10, while the component values used for the realization of the converter is displayed on 12.

4.1.1 Transmitter

The transmitter is composed by the RSC buck converter and an optical isolator that decouples the high-power circuit to the microcontroller. The simplified schematics of the transmitter circuit is shown in Figure 61. The switched capacitor cell has been rearranged so that the GaN-FET driving circuitry can easily access the same ground node as the input

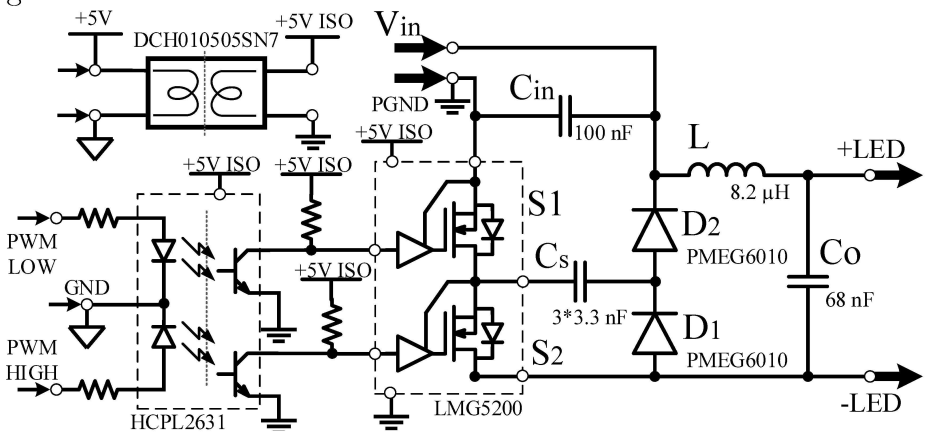
Table 12 – Component values for the converter realization.

Component		Value	Code	Packaging
Switched Capacitance	C_s	$3 \cdot 3.3\,nF$; $50\,V$	–	0603
Output Capacitance	C_o	$68\,nF$; $50\,V$	–	0603
Inductance	L	$8.2\,\mu H$; $7.3\,A$	SRR1210	$(12 \cdot 12 \cdot 10)\,mm$
Active Switch (GaN-FET)	$S_1; S_2$	$80\,V$; $10\,A$	$LMG5200$	9QFM
Diodes (Schottky)	$D_1; D_2$	$60\,V$; $1\,A$	$PMEG6010$	SOD123F

Note: The LMG5200 comprises both active switches in half-bridge configuration, as desired, including its respective driving circuits in a single packaging.
Source: Author (2020).

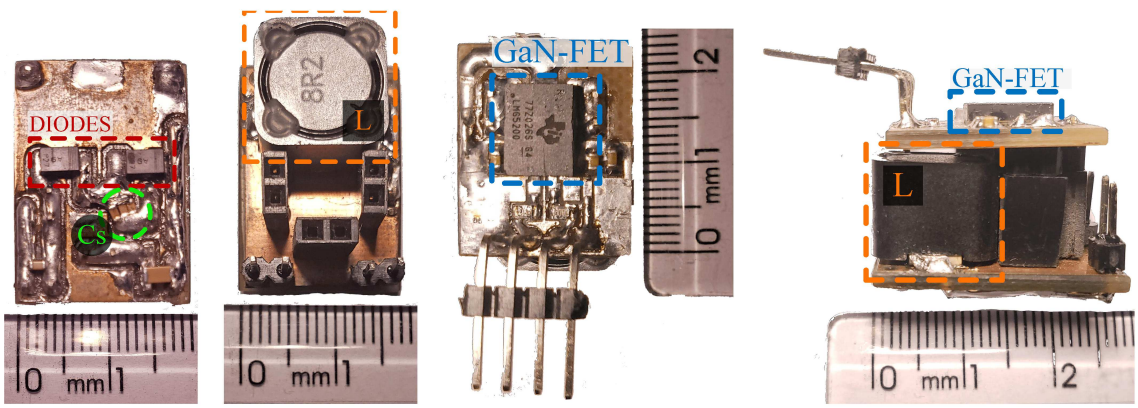
source. This repositioning is purely for practical purposes and present no effect to the operation of the circuit. The prototypes are shown in Figure 62. An appropriate inductor for high-frequency operation was chosen, as well as a switched capacitor with NP0/C0G dielectric. The transmitter circuit presents dimensions of $(23mm \cdot 16mm \cdot 19mm)$, and power density of $1.43\,kW/dm^3$.

Figure 61 – VLC transmitter schematics based on RSC buck converter.



Source: Author (2020).

Figure 62 – Transmitter prototype: (a) bottom layer view and (b) top layer view of passive board, (c) GaN-FET board and (d) assembled transmitter.



(a) (b) (c) (d)

Source: Author (2020).

4.2 COMPONENTS WAVEFORMS

At first, the converter operation must be validated through experimental results by analyzing the components waveforms as it is expected by the theoretical analysis presented in Section 2.2.

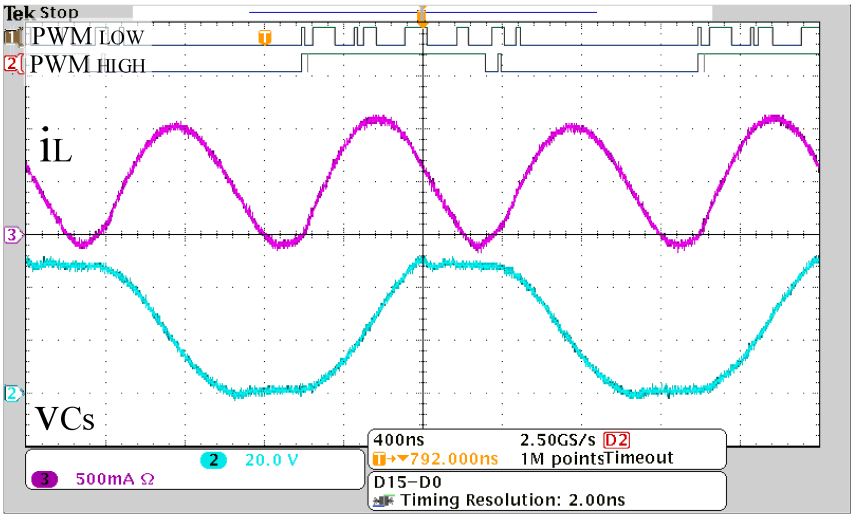
The figures presented in this section also contain the PWM signals measured at the output of the microcontroller for reference, named according to Figure 61. It is important to note that the isolating circuit presented inverts the signals. Therefore, while the PWM LOW signal controls the switch S_1, that means the switch S_1 will be conducting current whenever the PWM LOW signal is in LOW state, since it was measured at the input of the isolator and at the output of the microcontroller. Unfortunately, since the voltage measurements require a change in the reference probe, the PWM signals were often kept floating, with the exception of the measurement of the active switches which allowed for proper PWM measurement.

The waveform of the states v_{Cs} and i_L are shown in Figure 63. The voltage is shown to present minimum value of $0\,V$ and a maximum value of approximately $V_{in} = 48\,V$, as expected. When the PWM LOW signals siwthces to LOW state, the gate signal at the S_1 switch is HIGH due to the isolator's inverting characteristics. Thus, the capacitor starts its charge as expected while the inductor magnetizes and demagnetizes. Since the charging delay of the capacitor is not enough to demagnetize the inductor completely, the remaining energy is released with the charged capacitor. The switched capacitor C_s discharges when the PWM HIGH signal changes to LOW state, which allows the switch S_2 to conduct current, connecting the charged switched capacitor C_s to the output.

The measured waveforms show expected behavior for the states, thus validating the theoretical analysis. However, non-idealities of the components create small discrepancies, where the most evident is the negative values of current i_L. As analyzed theoretically, the diodes D_1 and D_2, reverse biased at this point, would oppose current at the inductor. However, once the GaN-FETs also present intrinsic diodes, there is a current path that allows circulation of negative current through the inductor.

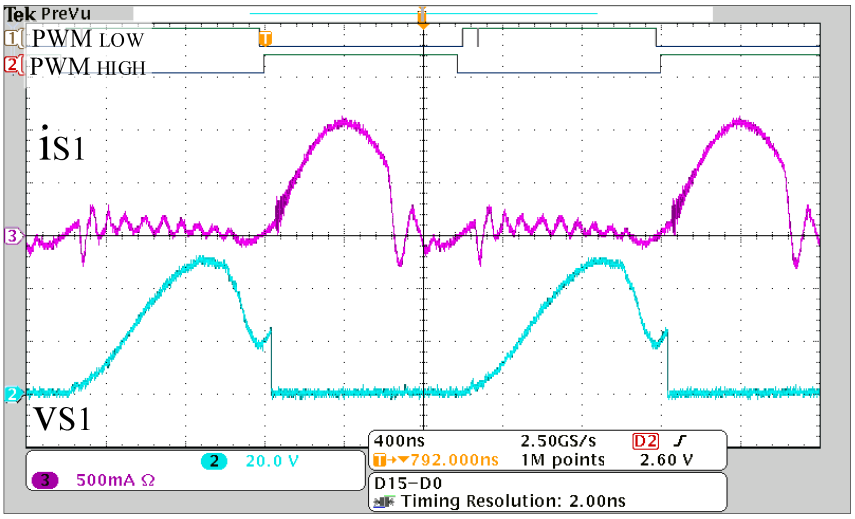
Likewise, Figure 64 shows the waveforms of both current and voltage at the active switch S_1, where it is possible to clearly identify the PWM signals. As it is shown, the S_1 switch conducts current when the PWM LOW signal is at LOW state (and thus the gating signal of S_1 is HIGH). At this instant, the current at the switch S_1 is the same as the Inductor current. This current is suddenly interrupted when the switched capacitor C_s reaches its maximum voltage. When the switch S_1 is in blocking stage its current is nearly null, presenting oscillations due to non-idealities of the component, where the voltage is allowed to increase.

Figure 63 – Waveforms of current at inductor L and voltage at switched capacitor C_s.



Legend: Analog channels: CH2 - Voltage v_{Cs}, CH3 - Current i_L. Digital channels: CHD1 - PWM LOW, CHD2 PWM HIGH.
Source: Author (2020).

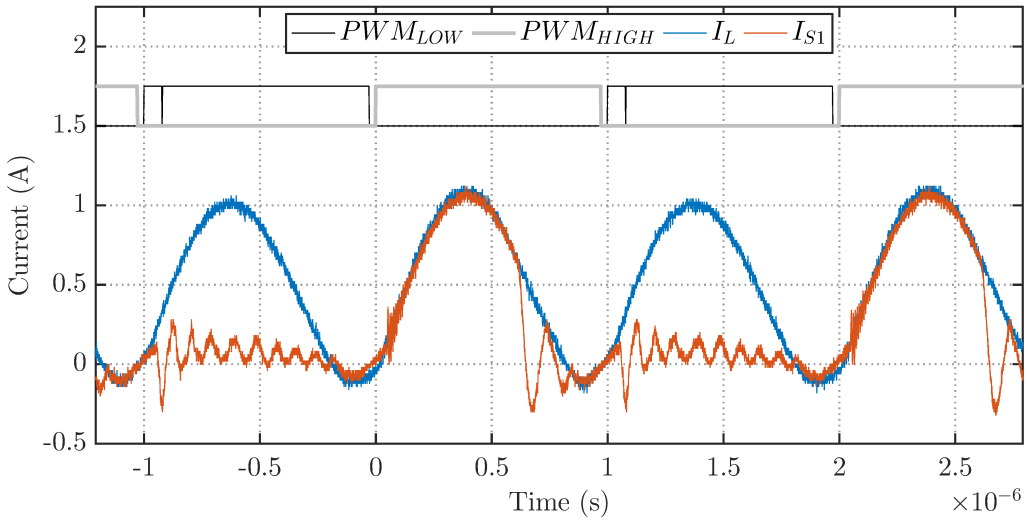
Figure 64 – Voltage and current waveforms at active switch S_1.



Legend: Analog channels: CH2 - Voltage v_{S1}, CH3 - Current i_{S1}. Digital channels: CHD1 - PWM LOW, CHD2 PWM HIGH.
Source: Author (2020).

Once the gating signal fails for the other measurements, aligning the oscilloscope trigger between measurements was not possible. However, plotting the data acquired and aligning the currents adequately allows for a clearer comparison between currents, where the negative values of the inductor current i_L can be attributed to the GaN-FETs intrinsic diode, as can be seen in Figure 65.

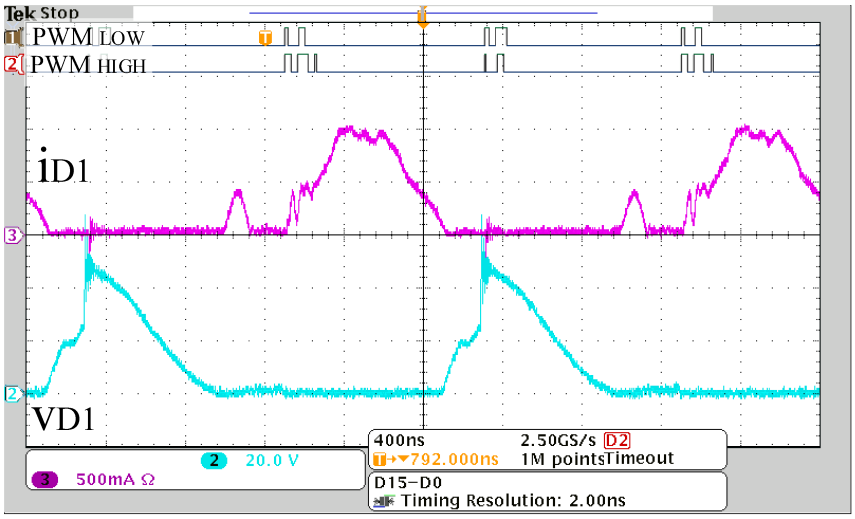
Figure 65 – Experimental current comparison between inductor L and active witch S_1.



Source: Author (2020).

Accordingly, the voltage and current across diode D_1 were also measured, as shown in Figure 66. The waveforms show adequately the difference between conduction and blocking modes, with current and voltages rising alternatively as expected. The current waveform was expected to show a sinusoidal half-cycle for the conducting period of the switch S_1 and a smaller peak related to the demagnetizing of the inductor at the end of the S_2 conduction period. This was shown to occur as nearly as expected albeit non-idealities of the components. Likewise, the voltage waveform was expected to present a steep increase with a constant value divided in two steps, proceeded with a slower decrease down to $0\,V$ once again. This was shown to occur, once again, with non-idealities, as it is expected of an experimental result.

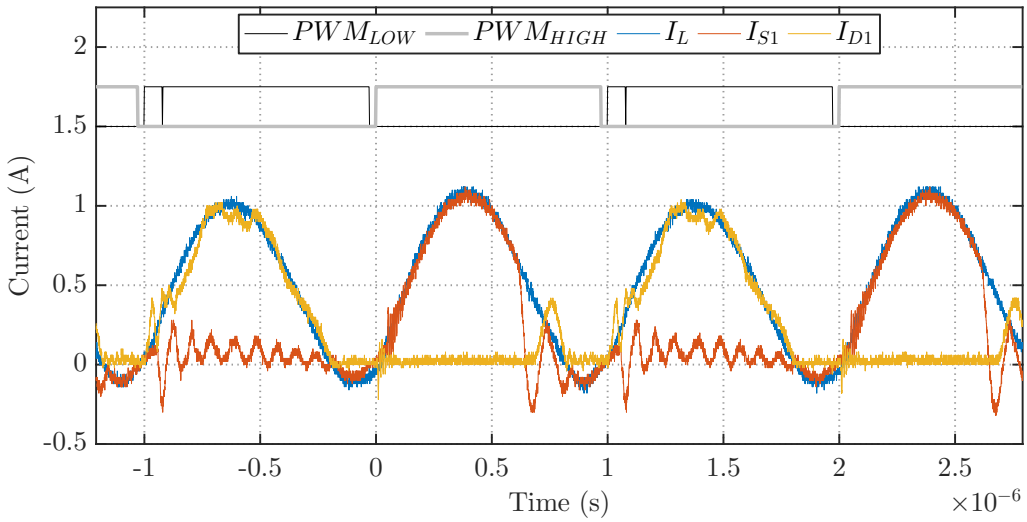
Figure 66 – Voltage and current waveforms at diode D_1.



Legend: Analog channels: CH2 - Voltage v_{D1}, CH3 - Current i_{D1}.
Digital channels: CHD1 - PWM LOW, CHD2 PWM HIGH.
Source: Author (2020).

When properly aligned, the current waveform at the D_1 diode can be more clearly compared to the inductor current I_L and the S_1 switch current I_{S1}. Figure 67 displays such comparison where one can see how the diode and the active switch operate alternatively in order to supply the inductor current.

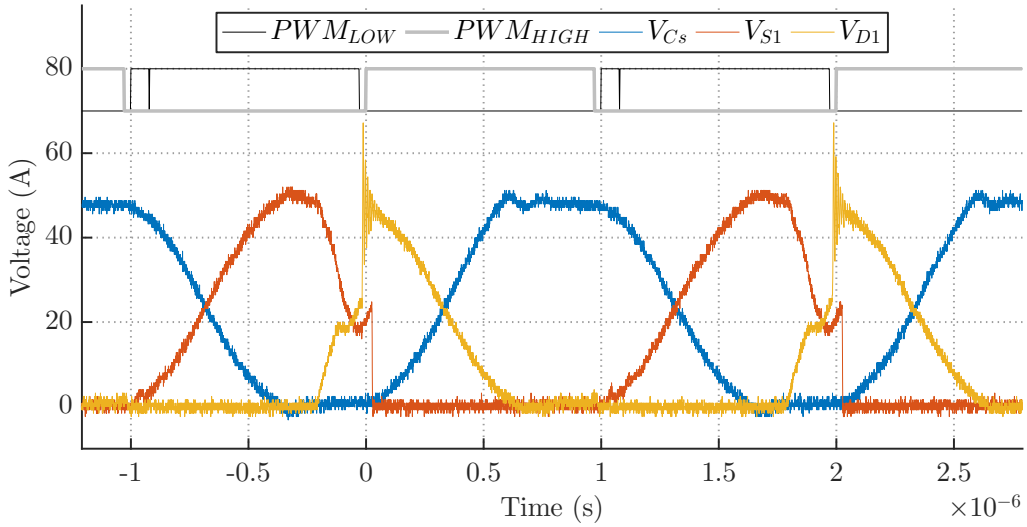
Figure 67 – Experimental current comparison between inductor L and active witch S_1.



Source: Author (2020).

The same can be done with the main voltages across the components, as shown in Figure 68.

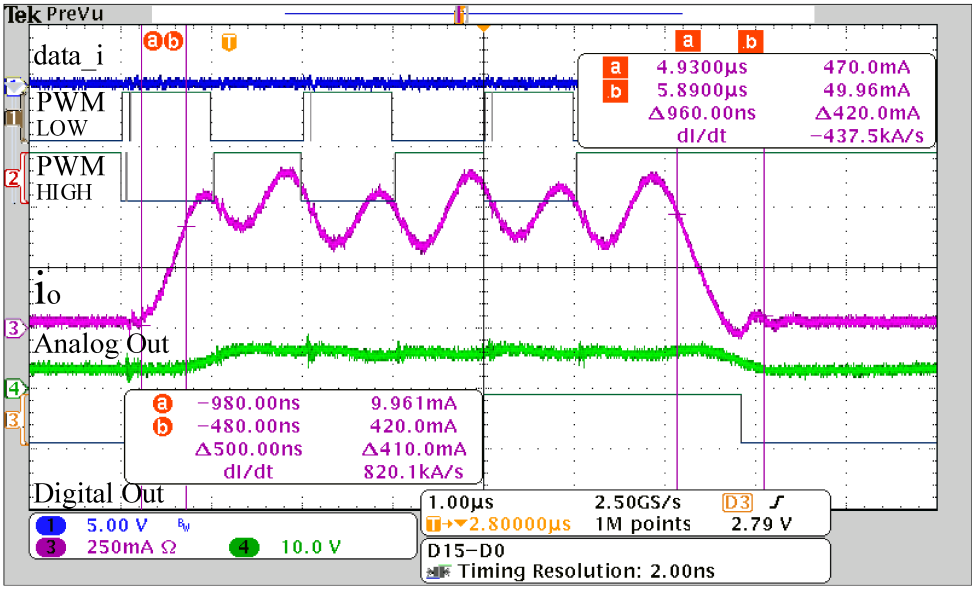
Figure 68 – Experimental voltage comparison between switched capacitor V_{Cs}, active switch S_1 and diode D_1.



Source: Author (2020).

Finally, the current at the LED load was measured while transmitting the bit '0' continuously, effectivelly allowing for the measurement of the t_{rise} and t_{fall} timespan. The result is shown in Figure 69, where the instantaneous transmitted data is shown alongside the PWM signals, the output current and both analog and digital outputs of the receiver.

Figure 69 – Waveforms at output and receiver.



Legend: Analog channels: CH1 - Data transmitted, CH3 - Current i_{out}, CH4 - Receiver Analog Output. Digital channels: CHD1 - PWM LOW, CHD2 PWM HIGH, CHD3 - Receiver Digital Output.
Source: Author (2020).

Table 13 displays a comparison between the expected values according to the proposed design procedure and the experimental results. As can be seen, the values of rise time and fall time are as expected, presenting errors of around 3.2% and 0.5% respectively between experimental and expected values. The current values presented higher errors, although still whitin the accepted. THe inductor peak current varied between expected and measured in around 13% while the LED current ripple presented an error of 16%. The difference in the output current ripple is beneficial, however, and in accordance with the calculation of the output capacitor C_o that limited maximum output ripple.

Table 13 – Experimental validation of RSC buck converter design.

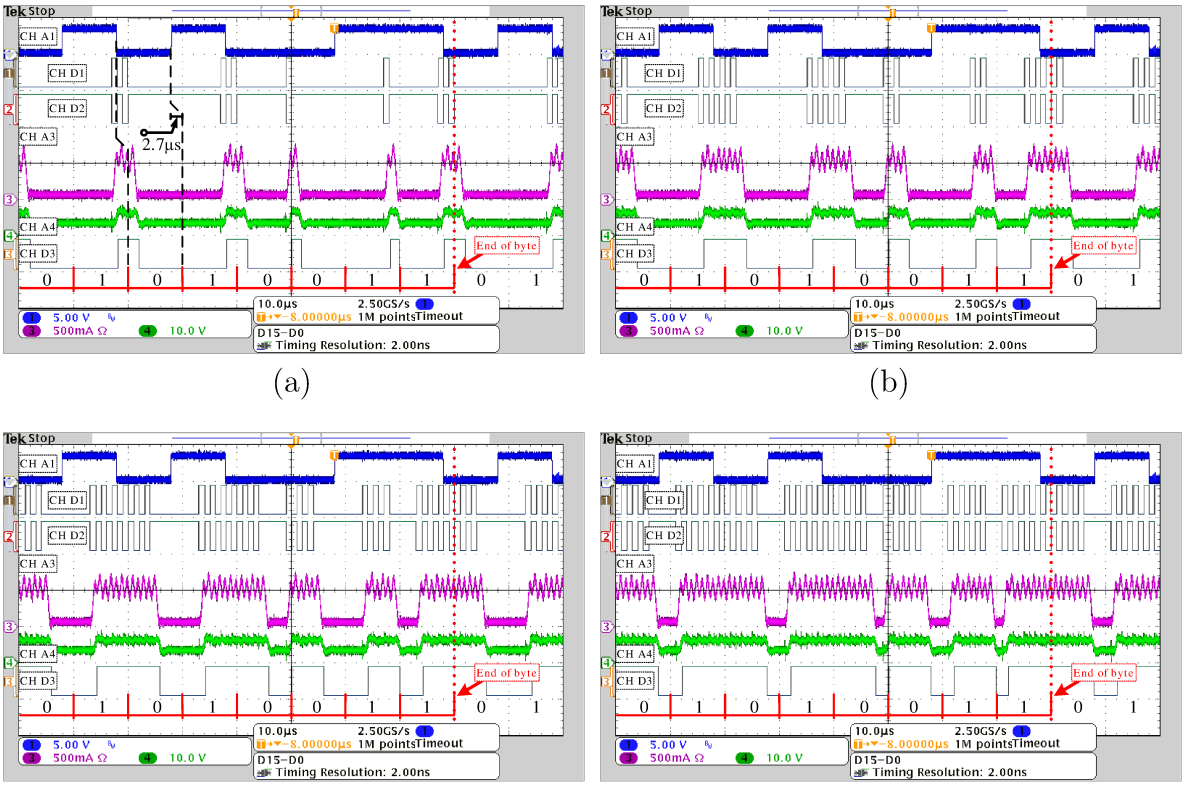
Switching times				
		Simulated	**Expected**	**Measured**
Rise Time	t_r	440.0 ns	484.3 ns	500.0 ns
Fall Time	t_f	955.0 ns	964.5 ns	960.0 ns
Current Variations				
		Simulated	**Expected**	**Measured**
Inductor Peak Current	ΔI_L	0.970 A	0.968 A	1.098 A
LED Current Ripple	ΔI_{led}	0.351 A	0.361 A	0.302 A

Source: Author (2020).

4.3 DATA TRANSFER

Te data transfer at 100 $kbps$ is then evaluated in Figure 70 for the appropriate allowed light levels. A bitstream of [01010011] is sent repetitively. This bitstream was chosen to allow simple visual demonstration of every possible bit transition ($0-1$, $1-0$, $0-0$ and $1-1$). One can note that for all cases, the coded bitstream is available at the receiver-side, showing that the proposed converter is able to transmit the desired data. A latency can be perceived, however, due to delays on both transmitter and receiver circuits, totaling a delay between input and output of around 2.7 μs.

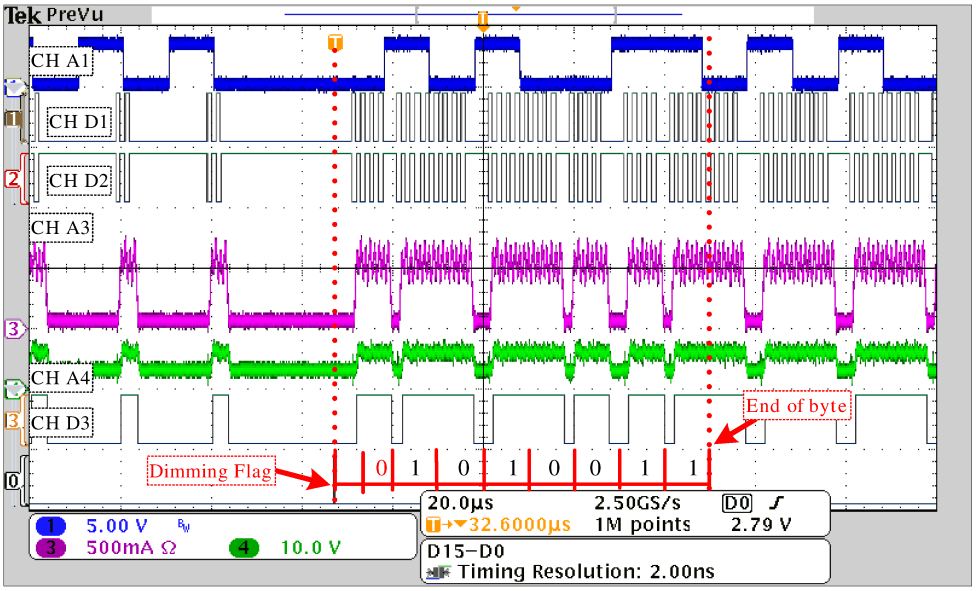
Figure 70 – Data transmission of bit [01010011] at light levels of (a) 20%, (b) 40%, (c) 60% and (d) 80%.



Legend: Analog channels: CH A1 (5 V/div) - DATA, CH A3 (500 mA/div) - Output Current, CH A4 (10 V/div) - Analog output of VLC receiver. Digital channels: CH D1 - PWM at switch S_1, CH D2 - PWM at switch S_2, CH D3 - Digital output at VLC receiver. Horizontal scale: 10 $\mu s/div$.
Source: Author (2020).

Both transmitter and receiver operate according to expected, with the system appropriately aligning the light pulse at the beginning of the data period for 0 bit and at the end of the data period for the 1 bit. Finally, the system under duty cycle variation is highlighted in Figure 71.

Figure 71 – Data transmission of bit [01010011] for a dimming step, from 20% to 80% light level.



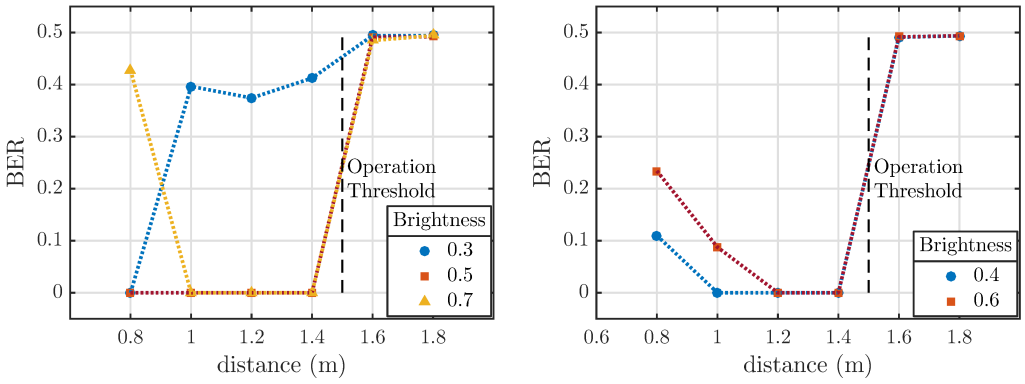
Legend: Analog channels: CH A1 (5 V/div) - DATA, CH A3 (500 mA/div) - Output Current, CH A4 (10 V/div) - Analog output of VLC receiver. Digital channels: CH D1 - PWM at switch S_1, CH D2 = PWM at switch S_2, CH D3 - Digital output at VLC receiver. Horizontal scale: $20\,\mu s/div$.
Source: Author (2020).

4.4 BER

The simple decoding system described in section 3.4.2 was implemented in order to validate the transmitter operation over a transmission of 512 pseudo-randomly-generated bits. The same vector of pseudo-random values was transmitted over different distances and brightness levels allowing for the bit error rate (BER) calculation by dividing the number of bit errors by the total number of transferred bits.

As can be seen in Figure 72, the operation of the system is validated over a distance range of around $1\,m$ for average brightness levels. The system operates well (bit error null) at $0.8\,m$ as long as the brightness is sufficiently low. The range of transmission of the system under test is limited at around $1.5\,m$. It is important to highlight that the limitations are caused by the receiver circuit, that maintains constant reference at the regenerator and therefore is only optimal at a certain distance (at lower distances, the TIA saturates due to constant gain and offset at higher brightness levels; at higher distances, the signal strength is too low to change the regenerator's state due to constant comparator reference). Albeit more sophisticated receiver circuits and demodulation algorithms could assist the performance of the system, such alternatives are out of the scope of this work and were not pursued for now.

Figure 72 – BER estimation over different distances and brightness levels for (a) 50 *kbps* transmission rate and (b) 100 *kbps* transmission rate.



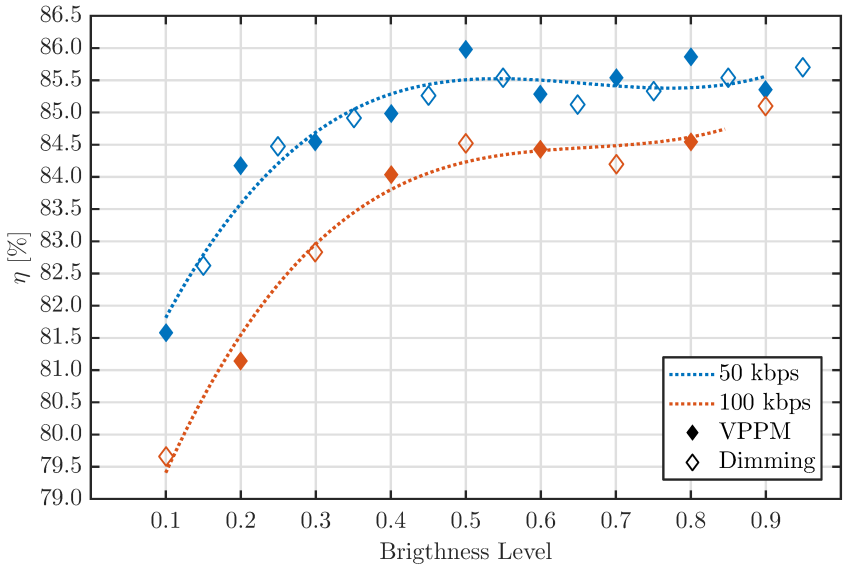
(a) (b)

Source: Author (2020).

4.5 EFFICIENCY ANALYSIS

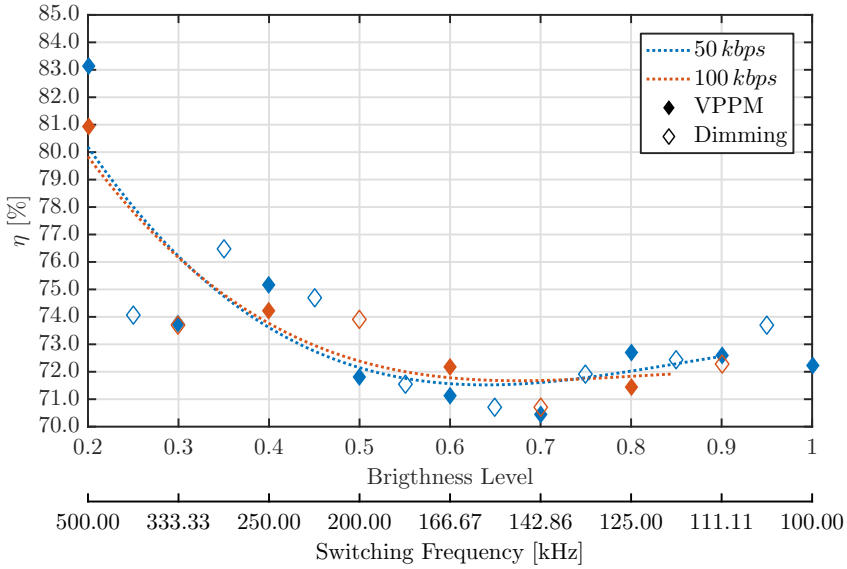
In order to analyze the converter's efficiency, power measurements were performed at both input and output with a digital power meter for different lighting levels while switching frequency is kept constant at $f_s = 0.5\,MHz$. The results are presented in Figure 73. On the other hand, efficiency can be also analyzed through the condition of constant output power while adjusting both light level and switching frequency accordingly, as shown in Figure 74. Data was collected for both transmission rates within the dimming possibilities of the 50 *kbps* rate, even though data transmission and dimming is limited to fixed steps as shown in Figure 50.

Figure 73 – Efficiency analysis of the power stage for given brightness levels (constant switching frequency f_s).



Source: Author (2020).

Figure 74 – Efficiency analysis of the power stage for given switching frequencies (constant output power P_o).



Source: Author (2020).

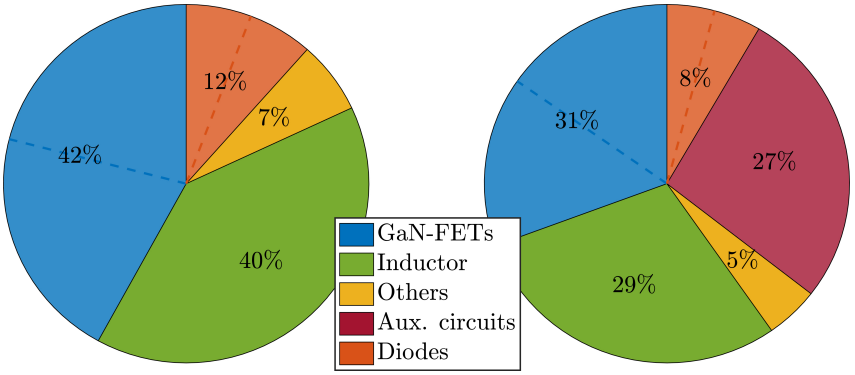
As shown in Figure 73, the efficiency of the converter is higher at low transmission rates. Since in both cases the same amount of switching cycles occur per second, this difference is attributed not to switching losses, but to the spacing between modulation cycles. For 50 *kbps* scenario, pulses are grouped together rather than spaced, meaning that the output capacitor C_o is charged less often and the LED is kept biased for more time. This effect is increased at lower brightness levels, where at the lowest possible, singular pulses at 50 *kpbs* are still grouped together at '1'-'0' crossings, but bit asymmetry at 100 *kbps* stops this grouping altogether by having singular pulses only at a certain bit. This effect can also be perceived at lower brightness levels at the constant power plot in Figure 74, although such differences are overshadowed likely due to inductor's core losses, expected to rise as frequency decreases.

Converter losses are less significant for higher power as the converter reaches efficiencies of up to 85.41% for transmission rates of 100 *kbps* and up to 85.7% for transmission rates of 50 *kbps*. The efficiency levels obtained for the RSC buck converter match efficiency levels found in literature for the same power level. For instance, (CASTELLANOS *et al.*, 2017) uses a similar structure on a CMOS LED driver for up to 700 mA, reaching 83.1% efficiency in nominal operation. In (RENTMEISTER; STAUTH, 2017), a power delivery of 10 W can be achieved by a $2V : 5A$ setup or by a $8V : 1.25A$ setup, with respective efficiencies of around 85% and 80.0%. Furthermore, the relation between efficiency and switching frequency was shown to be almost constant at around 77.5% for lower frequencies, but once again surpassing the 80% mark for nominal switching frequency.

In order to investigate power loss, a power breakdown for the three major components has been performed by measuring both current and voltage at a finite and integer

num of cycles for each component. Figure 75 displays the relative consumption of the GaN-FETs, diodes and inductor. The measurement was performed with burst mode disabled. The losses at the individual components were estimated using the waveforms of the oscilloscope after probe calibration involving deskew, gain and offset correction. Then, the auxiliary $5\,V$ circuit (containing isolation and driving of the GaN module) had its quiescent current measured through a multimeter, allowing loss estimation. The auxiliary circuit was shown to present a fairly significant consumption for the overall load power in this case (10 W) of around $0.52\,W$, representing 5% of the nominal power given that the output power is very low. With this figure, the efficiency considering the auxiliary driving/isolation circuitry drops from 85.41% to 81.78% for rates of $100\,kbps$ and from 85.7% to 82.04% for transmission rates of $50\,kbps$ when comparing purely with the power stage of the transmitter.

Figure 75 – Power loss breakdown for the main components of the RSC converter while (a) considering purely the power converter and (b) adding the power of the auxiliary circuit.



Source: Author (2020).

It can be noted that the inductor alone is the main loss-causing element, dissipating nearly the same amount of energy as the two GaN-FETs combined. The use of high-frequency cores as well as an improved PCB layout with reduced current loops may improve the converter's efficiency.

4.6 PARTIAL CONCLUSIONS

In this chapter the results of the experimental tests are displayed and discussed. At first, the components waveforms were measured, allowing verification with the theoretical and simulated expectations. The currents were measured using flexible wires as jumpers, allowing passage at the current probe. The voltages were measured with simple voltage probes, using the auxiliary spring in order to reduce current loops.

With the validated waveforms and confirmation of expected operation, the data transfer was confirmed by transferring a fixed bitstream continuously. Four different levels of dimming were testes, as well as a dimming step. The measurements were performed using an oscilloscope, with transmitter and receiver being mutually observed. The converter and receiver were shown to operate as expected, proving that data transfer with the RSC buck converter is possible.

The following test validated the efficiency of the data transmitter through BER evaluation. The data acquisition showed that the data reception and demodulation is possible with the code described in Chapter 3. Challenges of this test were also presented in the experimental setup, that required a black plastic to cover the experiment barriers to reduce light reflection and interference. Additionally, the low power of the LED load presented limitations on maximum distance of the receiver, that could reach up to around $1.5\,m$.

The efficiency measurement was shown to be challenging as well, with the input and output power varying significantly specially for lower output power settings (maximum dimming). Regardless, an estimation of the efficiency was possible with varying output power and switching frequency. Additionally, the efficiency breakdown was performed for the components, indicating potential of efficiency improvement at the inductor.

5 CONCLUSION

In previous decades, LED technology has presented a consistent market penetration by exceeding previous technologies in luminous efficacy and lifespan, resulting in desirable financial viability. But beyond lighting purposes, the LEDs controllability and fast dynamic response have been inspiring new applications for light. Among these new applications lies the Visible Light Communication field, comprised by the technique of using light at the visible spectrum for communication purposes.

The increase of the converter slew rate has becoming a requirement for emerging VLC systems as an alternative to the low efficiency auxiliary switch currently applied to traditional slow-response converters. The exclusion of this auxiliary switch, however, introduces load dynamics that must be considered in the converter design.

This work proposes a new switched-capacitor cell as replacement for the previous switching cell such that, while applied to traditional dc-dc converter topologies, results in resonant switched-capacitor (RSC) converters with soft-switching semiconductors. The theoretical waveforms of the RSC forms of the main dc-dc lower-order converters were analysed in Chapter 2, with the addition of the RSC Flyback converter.

Chapter 3 presented the design of a resonant switched capacitor buck-type converter in which burst-mode was used to allow VPPM transmission in VLC applications. A design methodology was proposed for VLC-oriented converters considering output dynamics. Finally, a prototype was built capable of both data transmission and power processing of $10\,W$ as described in Chapter 4. The compact prototype, with dimensions of $(23mm \cdot 16mm \cdot 19mm)$, presented power density of $1.43\,kW/dm^3$. A VLC receptor was also built in order to evaluate data recognition.

The system has proven VLC applicability with appropriate burst operation as VPPM transmitter. A simple receiver was able to correctly recognize bits for several brightness levels. For the distance range where the receiver presented adequate operation, the obtained BER was null for the number of bits transmitted. This value is in accordance with literature BER values for VPPM, which can reach between 10^{-4} and 10^{-6} for VLC transmitters employing a series switch (ZHAO; XU; TRESCASES, 2014) (SALMENTO *et al.*, 2019). More precise BER values can be obtained with larger bitstreams, however hardware limitations prevented the pursue of such tests.

Finally, a transmission rate of $100\,kbps$ was achieved over a distance of $1\,m$ with an overall efficiency of $85.4\,\%$.

By presenting an appropriate operation with significant data transfer rate, it is believed that a proof of concept was achieved, displaying the validity of such circuit for a cutting-edge application that is VLC. However, being an early and introductory study on the matter, a comparison with other dual-purpose converters established in literature

would not be fair, once they operate at varying transfer rates and power levels, with several also performing grid connectivity with PFC. Nonetheless, the simplicity of the circuit, evident by its high power density powered by its small inductance due to the switched resonant loop displays promise for the RSC converter family.

As a result, more in-depth studies are suggested. Possible branches of study would naturally present in the experimental testing of the other RSC converters presented in this work, as well as in the increase of switching frequency, limited in this work by the microcontroller available. The author believe that not only a higher transmission rate could be achieved, but also the very efficiency could be positively affected due to the decrease of inductor core losses. Finally, PFC capability must be investigated, as grid connectivity would be a significant step for the popularity of such circuit.

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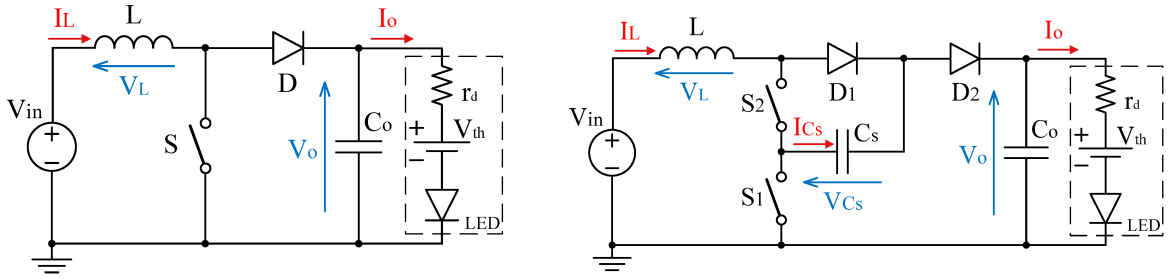
APPENDIX A – Mathematical analysis of the remaining converters

An in-depth mathematical analysis is developed in this appendix for the remaining converters similarly to the buck analysis shown in Section 2.2.

A.1 RSC BOOST ANALYSIS

The classic boost converter is shown on Figure 76 alongside the RSC boost converter. The six distinct stages are highlighted in Figure 77.

Figure 76 – Classic boost converter (a) and RSC boost converter (b).



(a) (b)

Source: Author (2020).

A.1.1 Switched capacitor analysis

The maximum and minimum voltages at the switched capacitor C_s are found through the voltage loop involving such capacitor and the reverse biased diode in stages 1 and 4.

For the stage 1 shown in Figure 78a, the blocking diode is D_2, and the analyzed loop comprises $[S_1 - C_s - D_2 - V_o]$. Thus, the voltage at the blocking diode is

$$v_{D2}(t) = V_o - v_{Cs}(t). \tag{A.1}$$

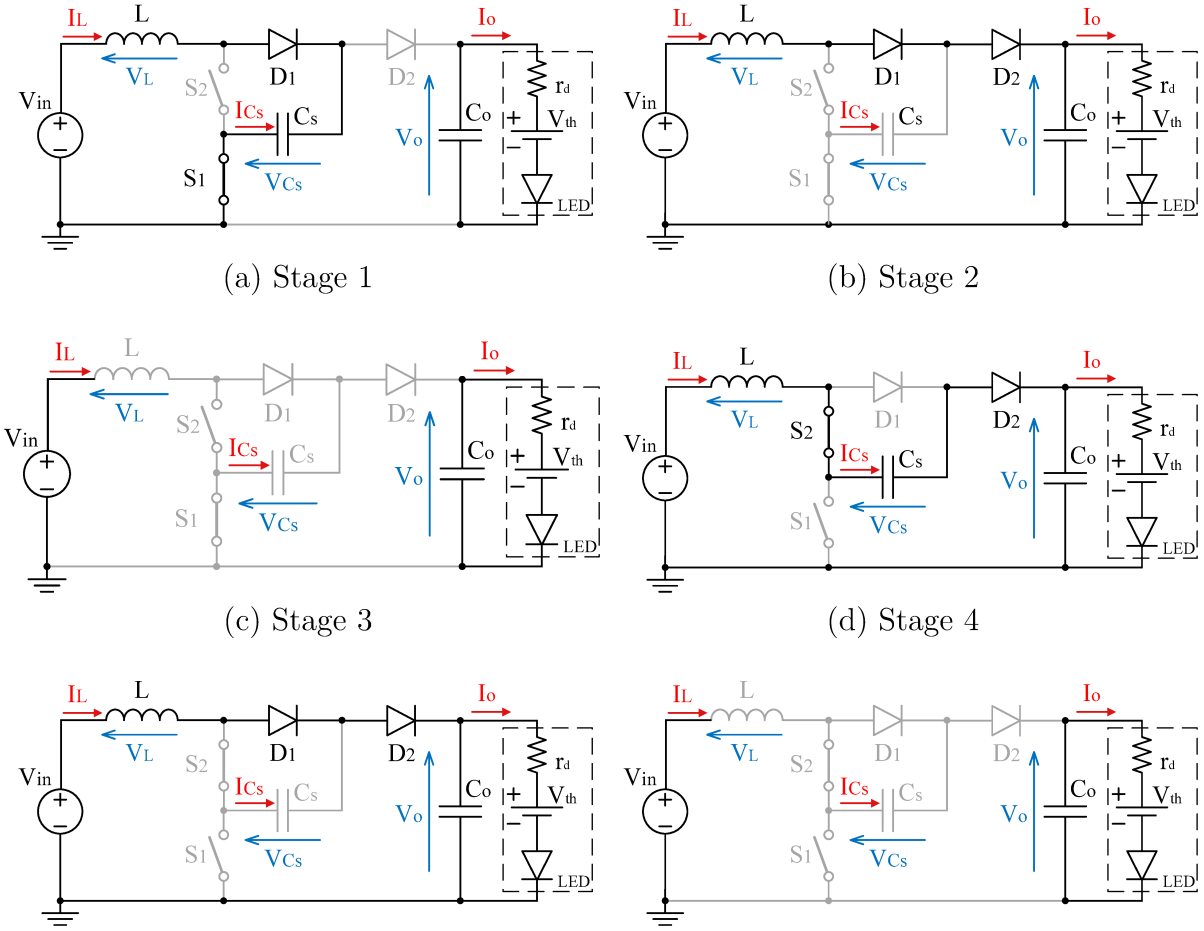
Therefore, when the voltage at the switched capacitor reaches $V_{Cs} = V_o$, blocking diode D_2 becomes forward-biased, thus stopping further voltage increase. In stage 4 described in Figure 78d, the blocking diode is D_1, with a blocking voltage described by

$$v_{D1}(t) = v_{Cs}(t). \tag{A.2}$$

Thus, by reaching null voltage during discharge the switched capacitor allows current conduction at diode D_1. In summation, maximum and minimum voltages at the switched capacitor C_s are

$$V_{Cs\,max} = V_o \; ; \; V_{Cs\,min} = 0. \tag{A.3}$$

Figure 77 – Stages of operation of the RSC boost converter.



(a) Stage 1

(b) Stage 2

(c) Stage 3

(d) Stage 4

(e) Stage 5

(f) Stage 6

Source: Author (2020).

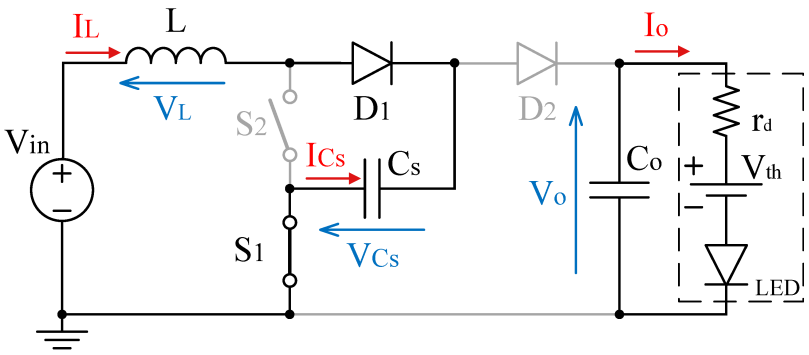
The operational analysis can now be described given the initial stages of the V_{Cs} state.

A.1.2 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor through the closed path displayed in Figure 78. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = 0 \\ i_L(t_0) = 0 \end{cases} \tag{A.4}$$

Figure 78 – Boost RSC: stage 1.



Source: Author (2020).

The semiconductor conditions for the boost converter in stage 1 are described in Table 14.

Table 14 – Semiconductor Conditions for RSC boost: stage 1.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = i_L(t)$
S_2	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described in (A.5) and (2.7).

Time Domain		Frequency Domain	
$V_{in} = v_{Cs}(t) + L\,\frac{d}{dt} i_L(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + s\,L\,I_L(s)$	(A.5)
$C_s\,\frac{d}{dt} v_{Cs}(t) = i_L$	$\xrightarrow{\mathcal{L}}$	$s\,C_s\,V_{Cs}(s) = I_L(s)$	(A.6)

Substituting the $I_L(s)$ equivalence given in (A.6) at (A.5) and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_{in}}{s}\,\frac{1}{C_s\,L\,s^2 + 1} = \frac{V_{in}}{s}\,\frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.7}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in}\,(1 - \cos(t\,\omega_0)). \tag{A.8}$$

On the other hand, isolating the inductor current from the equations (A.5) and (A.6) yields

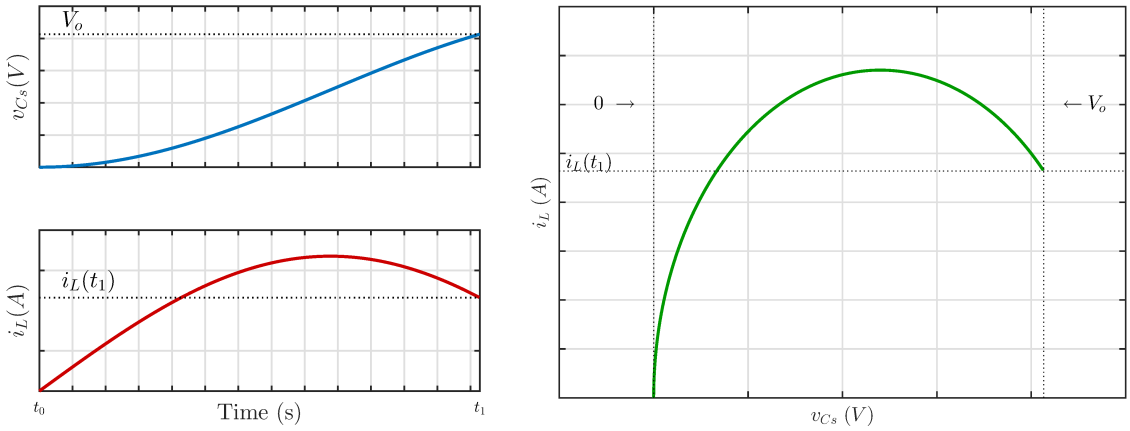
$$I_L(s) = C_s\, V_{in}\, \frac{1}{C_s\, L\, s^2 + 1} = C_s\, V_{in}\, \frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.9}$$

and finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\, \omega_0\, V_{in}\, \sin(t\, \omega_0). \tag{A.10}$$

The resulted waveforms described are shown in Figure 79.

Figure 79 – Boost RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



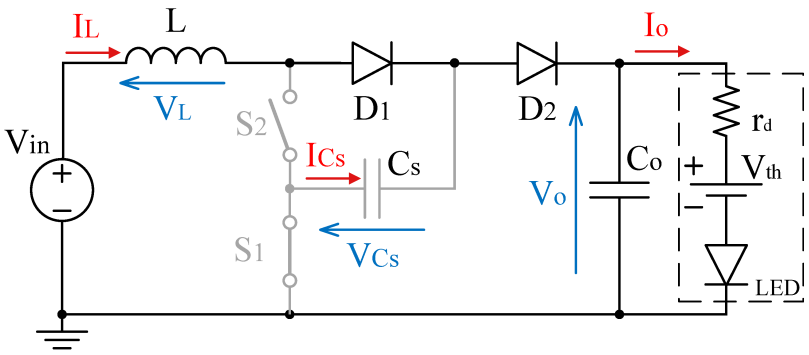
(a) (b)

Source: Author (2020).

When the capacitor reaches sufficient voltage to bias directly the diode D_2, the remaining energy on the inductor forces a current through the passive semiconductors as shown in Figure 80. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_o \\ i_L(t_1) = I_{L\,(t1)} \end{cases} \tag{A.11}$$

Figure 80 – Boost RSC: stage 2.



Source: Author (2020).

Table 15 highlights the semiconductor conditions for such state.

Table 15 – Semiconductor Conditions for RSC boost: stage 2.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described in as

Time Domain		**Frequency Domain**	
$V_{in} = L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L\,(s\,I_L(s) - I_{L(t1)}) + \frac{V_o}{s}.$	(A.12)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max}. \tag{A.13}$$

The inductor behavior can be solved by isolating $I_L(s)$ from (A.12), which yields

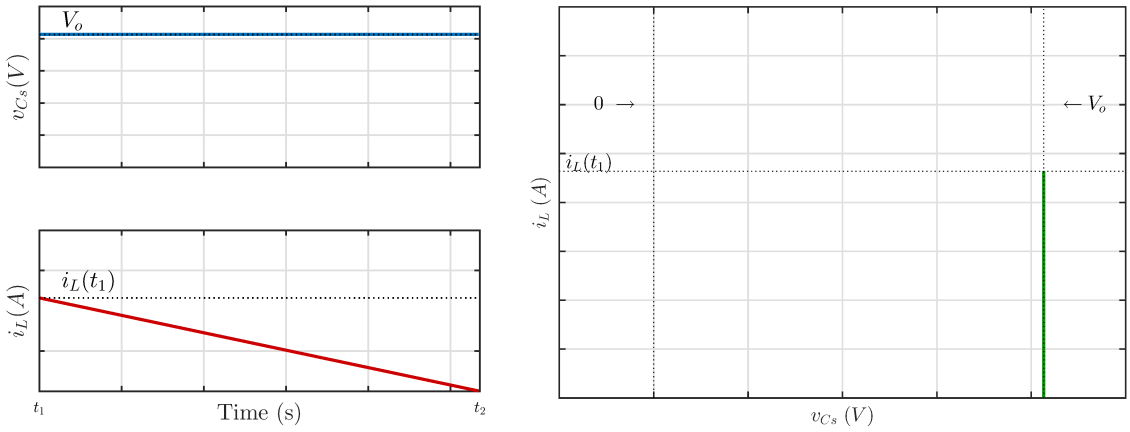
$$I_L(s) = \frac{I_{L(t1)}}{s} + \frac{V_{in} - V_o}{L\,s^2}. \tag{A.14}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_L(t) = I_{L(t1)} + \frac{V_{in} - V_o}{L}\,t. \tag{A.15}$$

The resulted waveforms described are shown in Figure 81.

Figure 81 – Boost RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



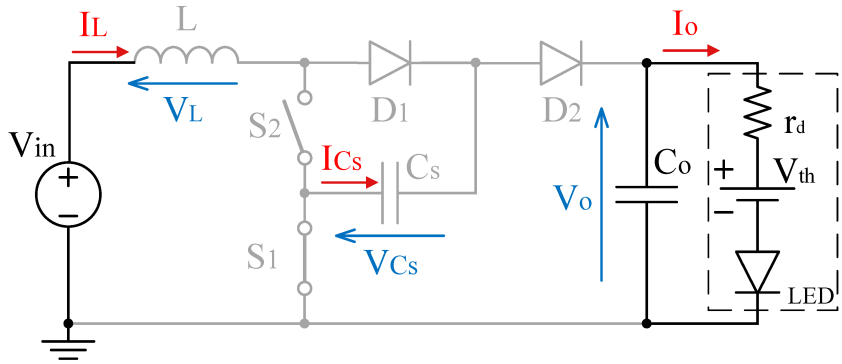
(a) (b)

Source: Author (2020).

This stage is characterized by the complete depletion of energy on the inductor and consequential annulment of current through the components, as shown in Figure 82. Given the required DCM operation, this study considers that the current on the inductors does reach zero while still on the first half of the switching period. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_o \\ i_L(t_2) = 0 \end{cases} \tag{A.16}$$

Figure 82 – Boost RSC: stage 3.



Source: Author (2020).

Through loop and node equations, the conditions for the semicondutors in given stage are described in Table 16.

Table 16 – Semiconductor Conditions for RSC boost: stage 3.

	State	Voltages	Currents
S1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S2	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D1	Blocking	$v_{D1} = v_{Cs}(t) - V_{in}$	$i_{D1} = 0$
D2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor current are constant as

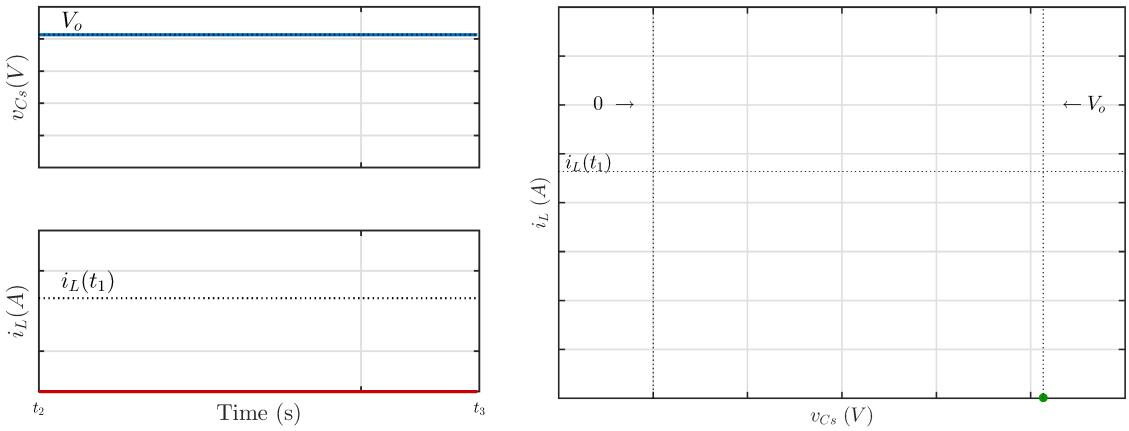
$$v_{Cs}(t) = V_{Cs\,max} = V_o \tag{A.17}$$

and

$$i_L(t) = 0. \tag{A.18}$$

The resulted waveforms described are shown in Figure 83.

Figure 83 – Boost RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



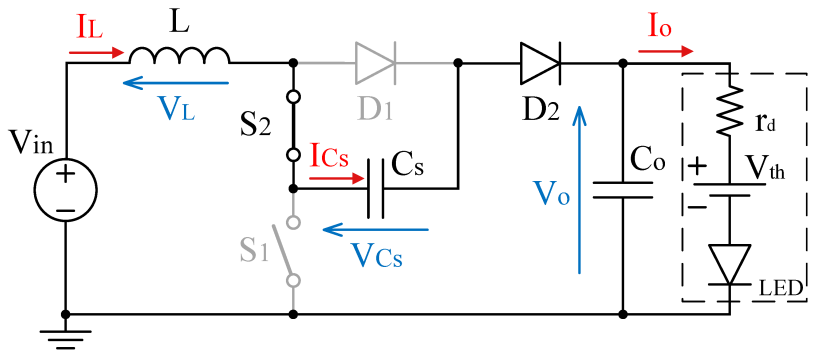
(a) (b)

Source: Author (2020).

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1, accordingly to Figure 84. The switched capacitor is once again added to the active part of the circuit allowing its storage energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_o \\ i_L(t_3) = 0 \end{cases} \tag{A.19}$$

Figure 84 – Boost RSC: stage 4.



Source: Author (2020).

Semiconductor values of current and voltage at stage 4 are describes in Table 17.

Table 17 – Semiconductor Conditions for RSC boost: stage 4.

	State	Voltages	Currents
S1	Blocking	$v_{S1} = V_o - v_{Cs}(t)$	$i_{S1} = 0$
S2	Conducting	$v_{S2} = 0$	$i_{S2} = i_L(t)$
D1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The node and loop equations for this stage are described by (A.20) and (A.21).

Time Domain		Frequency Domain	
$V_{in} = L\,\frac{d}{dt}i_L(t) + v_{Cs}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = s\,L\,I_L(s) + V_{Cs}(s) + \frac{Vo}{s}$	(A.20)
$C_s\,\frac{d}{dt}v_{Cs}(t) = -i_L$	$\xrightarrow{\mathcal{L}}$	$C_s\,(s\,V_{Cs}(s) - V_{Cs\,max}) = -I_L(s)$	(A.21)

Using both equations and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_o - V_{in}}{s}\,\frac{1}{C_s\,L\,s^2+1} + V_{Cs\,max}\,\frac{C_s\,L\,s}{C_s\,L\,s^2+1} = \frac{V_o - V_{in}}{s}\,\frac{\omega_0^2}{s^2+\omega_0^2} + V_o\,\frac{s}{s^2+\omega_0^2}. \tag{A.22}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_o - V_{in}\,(1 - \cos(t\,\omega_0)). \tag{A.23}$$

On the other hand, isolating the inductor current from the equations (A.20) and (A.21) yields

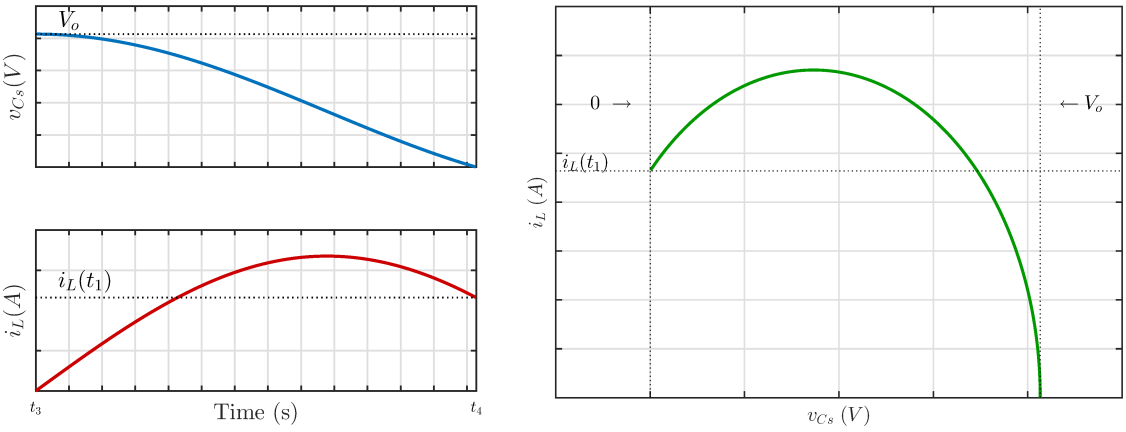
$$I_L(s) = C_s\,V_{in}\,\frac{1}{C_s\,L\,s^2+1} = C_s\,V_{in}\,\frac{\omega_0^2}{s^2+\omega_0^2}. \tag{A.24}$$

And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.25}$$

The resulted waveforms described are shown in Figure 85.

Figure 85 – Boost RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



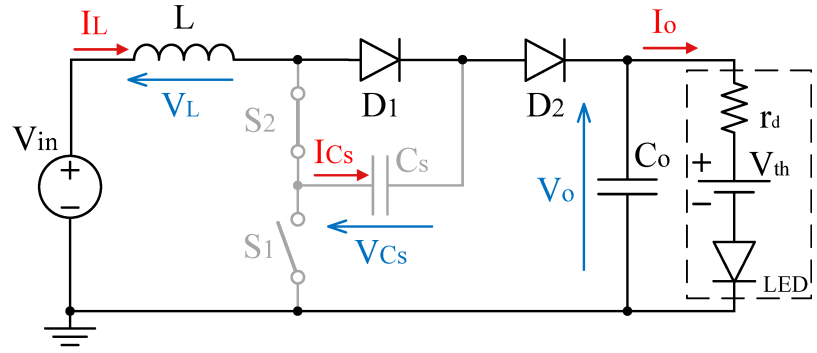
(a) (b)

Source: Author (2020).

With the complete discharge of the switched capacitor its voltage is maintained in zero, allowing the diode D_1 to be forward biased. Once again, remnant energy on the inductor forces a current flow into both diodes. The initial conditions to this stage are described by

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = 0 \\ i_L(t_4) = I_{L\,(t4)} \end{cases} \tag{A.26}$$

Figure 86 – Boost RSC: stage 5.



Source: Author (2020).

For stage 5, the condition of each semiconductor are highlighted in Table 18.

Table 18 – Semiconductor Conditions for RSC boost: stage 5.

	State	Voltages	Currents
$\mathbf{S_1}$	Blocking	$v_{S1} = V_o$	$i_{S1} = 0$
$\mathbf{S_2}$	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
$\mathbf{D_2}$	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described by (A.27).

Time Domain		Frequency Domain	
$V_{in} = L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L\,(s\,I_L(s) - I_{L(t4)}) + \frac{V_o}{s}$	(A.27)

With the capacitor completely discharged, its voltage remains zero

$$v_{Cs}(t) = V_{Cs\,min} = 0. \tag{A.28}$$

The inductor behavior can be solved by isolating $I_L(s)$ from (A.27), which yields

$$I_L(s) = \frac{I_{L(t4)}}{s} + \frac{V_{in} - V_o}{L\,s^2}. \tag{A.29}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

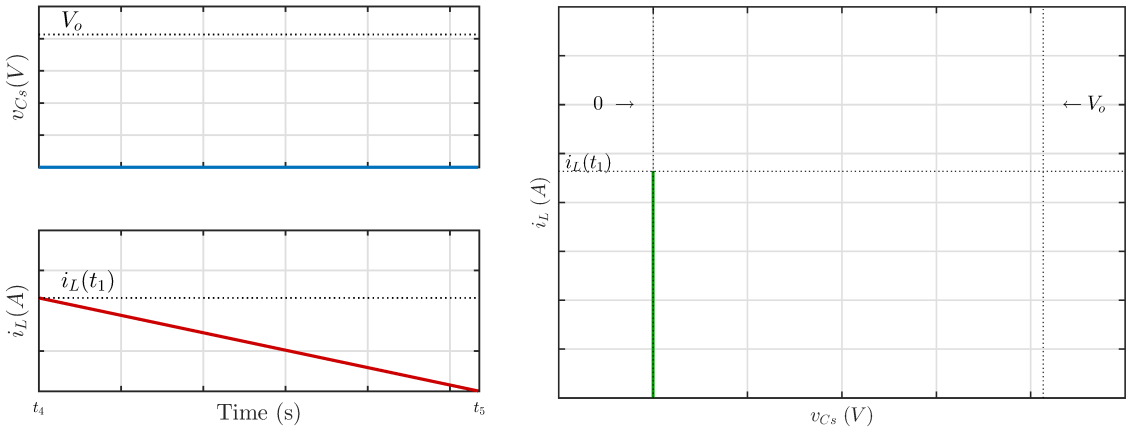
$$i_L(t) = I_{L(t4)} + \frac{V_{in} - V_o}{L}\,t. \tag{A.30}$$

The resulted waveforms described are shown in Figure 87.

Finally, with the end of the energy at the inductors, its current reaches zero before the ending of the switching cycle as shown in Figure 88. The time delay between these two events characterizes the stage 6, which presents as initial condition the following

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = 0 \\ i_L(t_5) = 0 \end{cases} \tag{A.31}$$

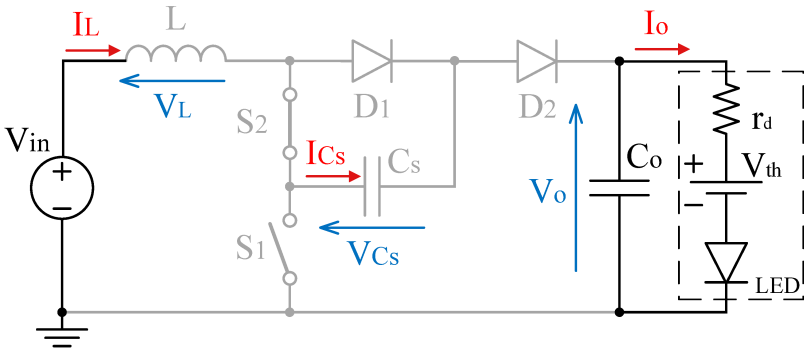
Figure 87 – Boost RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

Figure 88 – Boost RSC: stage 6.



Source: Author (2020).

Once again, the state of each semiconductor can be found and are described in Table 19.

Table 19 – Semiconductor Conditions for RSC boost: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = -v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - V_{in} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

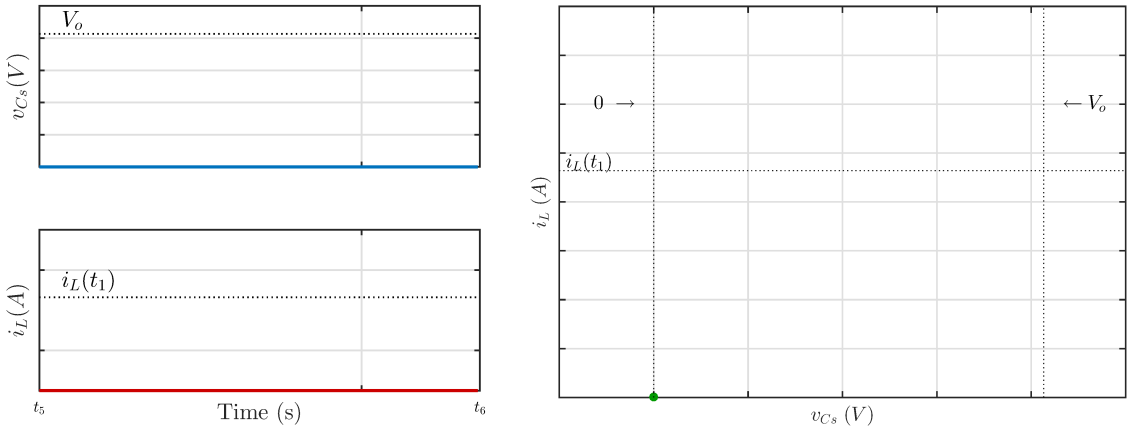
During stage 6 both capacitor voltage and inductor current are nell:

$$v_{Cs}(t) = V_{Cs\,min} = 0 \tag{A.32}$$

$$i_L(t) = 0 \tag{A.33}$$

The resulted waveforms described are shown in Figure 89.

Figure 89 – Boost RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.1.3 Time Analysis

In order to fully characterize the behavior of the converter, the time delay of each state must be determined.

A.1.3.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using the Eq (A.8) it is known that

$$v_{Cs}(t_1) = V_{in}\,(1 - \cos(\Delta t_1\,\omega_0)) = V_o. \tag{A.34}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$:

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{V_{in} - V_o}{V_{in}}\right) = \frac{1}{\omega_0}\,acos\,(1 - G)\,. \tag{A.35}$$

Applying the time duration for stage 1 into (A.10) it is possible to find the inductor current by the end of that stage which is required as one of the initial conditions for stage 2:

$$i_L(t_1) = C_s\,\omega_0\,V_{in}\,\sin(\Delta t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin\left(\frac{1}{\omega_0}\,acos(1 - G)\,\omega_0\right). \tag{A.36}$$

The result is given by (A.37):

$$I_{L\,t1} = C_s\,V_{in}\,\omega_0\,\sqrt{2G - G^2}. \tag{A.37}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $2G - G^2 > 0$, which results in a design requirement given in (A.38). Additionally, the boost converter topology inserts an inferior limitation to the static gain:

$$1 \leq G < 2. \tag{A.38}$$

A.1.3.2 Stages 2 and 5

The second stage is characterized by the discharge of the remnant energy on the inductors. From (A.15) and (A.37) it is known that

$$i_L(t_2) = I_{L(t1)} - \frac{V_{in} - V_o}{L}\,\Delta t_2 = C_s\,V_{in}\,\omega_0\,\sqrt{2G - G^2} + \frac{V_{in} - V_o}{L}\,\Delta t_2 = 0. \tag{A.39}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,(G-1)}\,\sqrt{2G - G^2}. \tag{A.40}$$

A.1.3.3 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}. \tag{A.41}$$

Which expands to

$$\frac{1}{\omega_0}\,acos\,(1-G) + \frac{1}{\omega_0\,(G-1)}\,\sqrt{2G - G^2} < \frac{1}{2\,f_s}. \tag{A.42}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\,f_s\,\left(acos\,(1-G) + \frac{1}{G-1}\,\sqrt{2G - G^2}\right). \tag{A.43}$$

A.1.4 Average Inductor Current

The average inductor current is found by integrating the current waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period

$$I_L = \frac{1}{T_s/2}\,\left(\int_{t_0}^{t_1} i_L(t)_1 dt + \int_{t_1}^{t_2} i_L(t)_2 dt\right). \tag{A.44}$$

By replacing the inductor current by its respective waveforms in each state yields

$$I_L = 2\,f_s\,\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{L(t1)} + \frac{V_{in} - V_o}{L}\,t\,dt\right). \tag{A.45}$$

Solving the equation above and making use of the relations given by (A.35), (A.37) and (A.40), the average output current can be simplified as (A.46):

$$I_L = C_s\,f_s\,V_{in}\,\frac{G^2}{G-1}. \tag{A.46}$$

A.1.5 Average Output Current

For the boost converter, the output current is the same as the current at diode D_2. Integrating its waveform over a period of time equal to the switching period yields the average output current:

$$I_o = \frac{1}{T_s}\left(\int_{t_0}^{t_1} i_{D2}(t)_1 dt + \int_{t_1}^{t_2} i_{D2}(t)_2 dt + \int_{t_2}^{t_3} i_{D2}(t)_3 dt + \int_{t_3}^{t_4} i_{D2}(t)_4 dt + \int_{t_4}^{t_5} i_{D2}(t)_5 dt + \int_{t_5}^{t_6} i_{D2}(t)_6 dt\right) \tag{A.47}$$

$$I_o = f_s \left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + 2\cdot\int_{t_1}^{t_2} I_{L(t1)} + \frac{V_{in}-V_o}{L}\,t\,dt\right). \tag{A.48}$$

Solving the equation above and making use of the relations given by (A.35), (A.37) and (A.40), the average output current can be simplified as (A.49):

$$I_o = C_s\,f_s\,V_{in}\,\frac{G}{G-1}. \tag{A.49}$$

A.1.6 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\,V_o = C_s\,f_s\,V_{in}\,V_o\,\frac{G}{G-1}. \tag{A.50}$$

Using the static gain definition stated as $V_o = G\,V_{in}$ the output power is given by

$$P_o = C_s\,f_s\,V_{in}^2\,\frac{G^2}{G-1}. \tag{A.51}$$

The capacitor must be sized accordingly to the output power, using the relation given by (A.52):

$$C_s = \frac{P_o}{f_s\,V_{in}^2\,G^2}\,(G-1). \tag{A.52}$$

A.1.7 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 20.

Table 20 – RSC boost simulation values fos (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

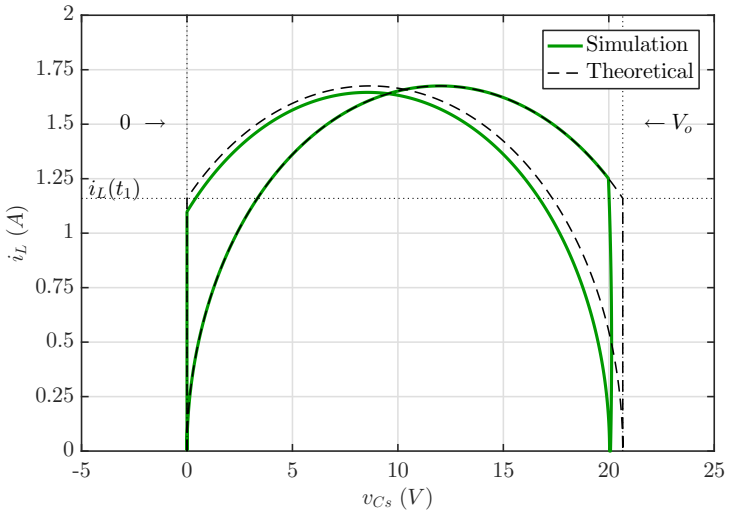
Source and Converter values		
Input Voltage	V_{in}	$12\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Output Capacitance	C_o	$470\,nF$
Switched Capacitance	C_s	$39\,nF$
Inductance	L	$2\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 90 yields a precise comparison between theoretical prediction and simulation result, highlighting specially the lower voltage of the charged switched capacitor.

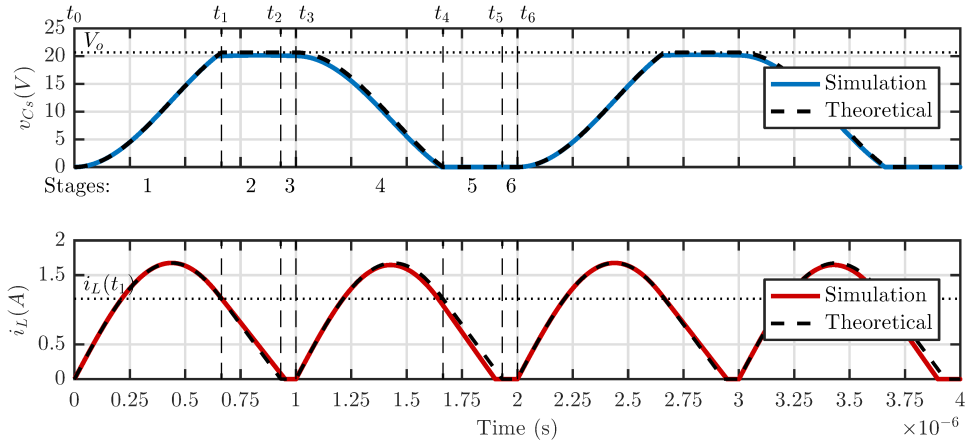
Figure 90 – State Plan for the RSC boost converter.



Source: Author (2020).

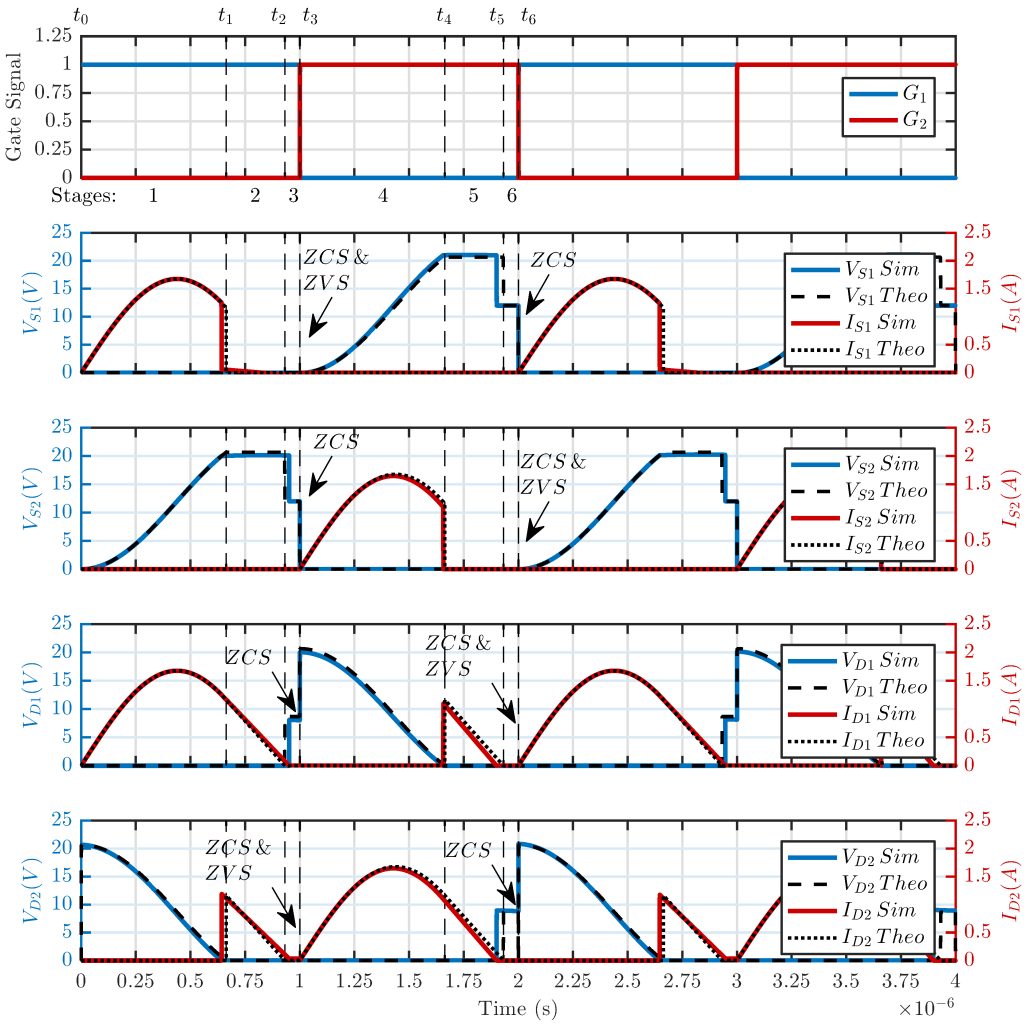
Thus, the waveform comparison of the RSC boost converter states for each stage in their respective timespans is shown in Figure 91. As seen, the maximum capacitor voltage caps slightly below the theoretical prediction due to the presence of the output loop, which also causes a faster demagnetizing of the inductor in stage 5. The small difference, however, highlights the consideration as a valid simplification of the circuit for its concise analysis. Finally, Figure 92 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 91 – Theoretical waveforms of the state variables for the RSC boost converter.



Source: Author (2020).

Figure 92 – Soft-switching on the semiconductors for the RSC boost converter.

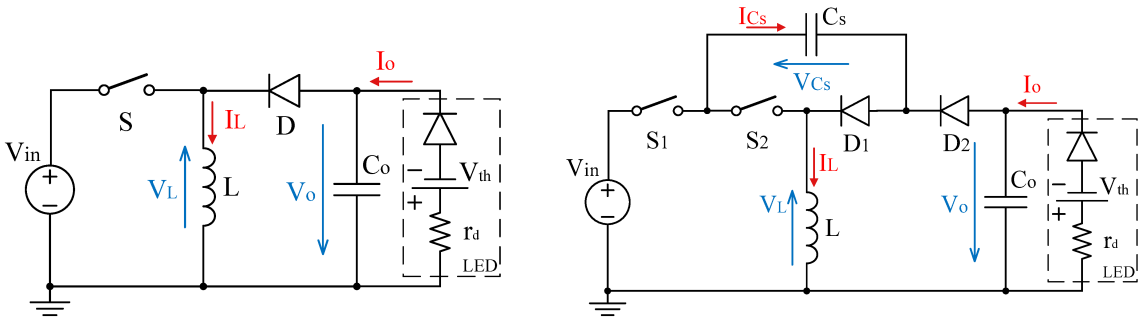


Source: Author (2020).

A.2 RSC BUCK-BOOST ANALYSIS

The classic buck-boost converter is shown on Figure 93 alongside the RSC buck-boost converter. The six distinct stages are highlighted in Figure 94.

Figure 93 – Classic buck-boost converter (a) and RSC buck-boost converter (b).



(a) (b)

Source: Author (2020).

A.2.1 Switched capacitor analysis

Once again, analyzing the voltage loops involving switched capacitor C_s and the reverse biased diode in stages 1 and 4 yields, respectively, the maximum and minimum voltage allowed across C_s.

In Figure 95a, the stage 1 is highlighted and it can be seen that the pertinent voltage loop to be analyzed comprises $[V_{in} - S_2 - C_s - D_2 - V_o]$. Thus, the voltage at the blocking diode D_2 is

$$v_{D2}(t) = V_{in} - v_{Cs}(t) + V_o. \tag{A.53}$$

The switched capacitor C_s is then stopped from further charging by the diode D_2 as soon as its voltage reaches $V_{Cs} = V_{in} + V_o$. On the other hand, its minimum voltage is determined by the stage 4 highlighted in Figure 95d. For this case, the appropriate loop is described by $[S_2 - V_{Cs} - D_1]$. Thus, voltage at the reverse biased diode D_1 is

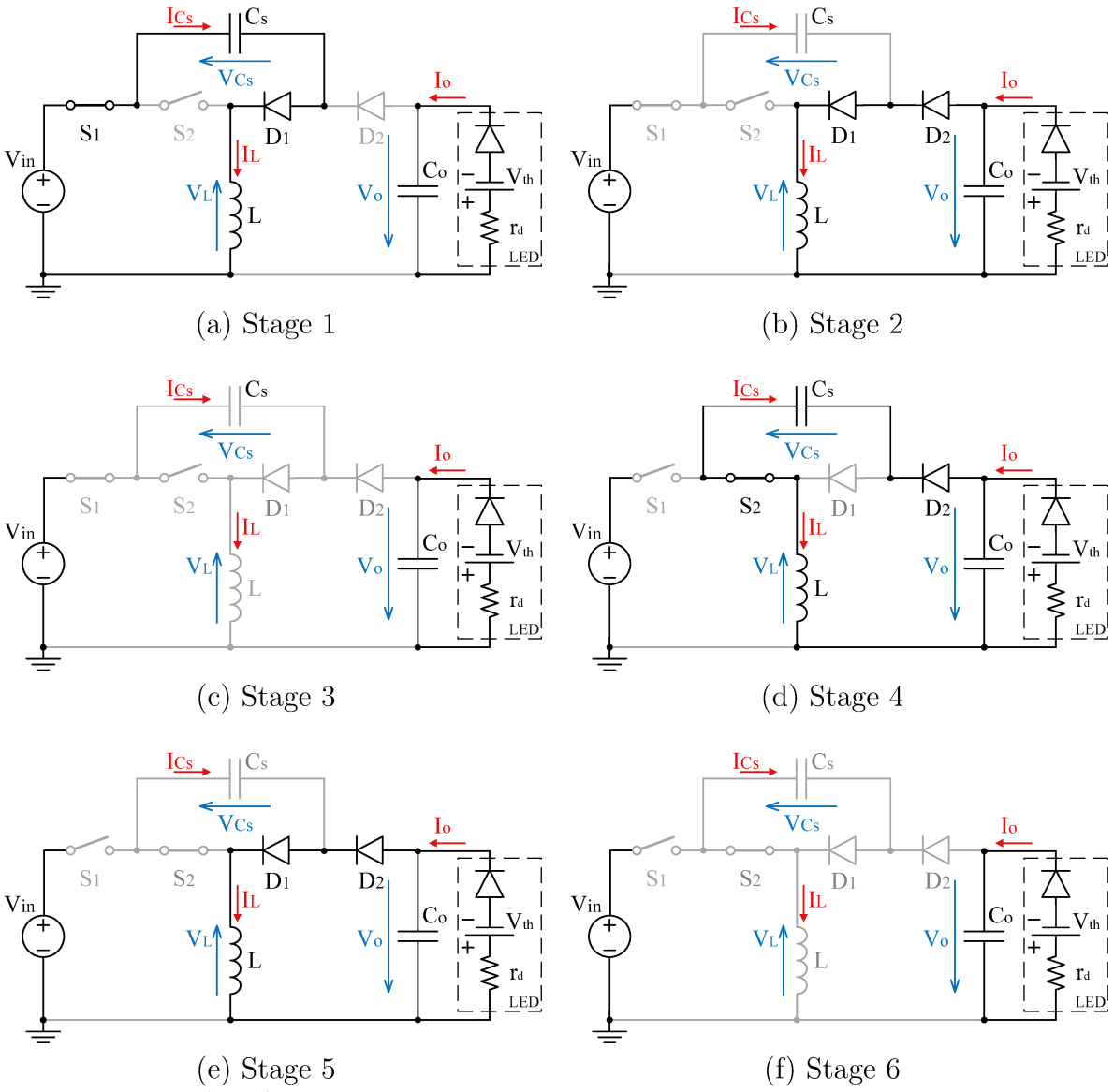
$$v_{D1}(t) = v_{Cs}(t). \tag{A.54}$$

When the switched capacitor C_s discharges to $V_{Cs} = 0$, the diode D_1 is allowed to conduct, stopping the C_s for further discharging. Therefore, minimum and maximum voltages at the switched capacitor C_s can be summarized by

$$V_{Cs\,max} = V_{in} + V_o \; ; \; V_{Cs\,min} = 0. \tag{A.55}$$

The operational analysis can now be described given the initial stages of the V_{Cs} state.

Figure 94 – Stages of operation of the RSC buck-boost converter.



(a) Stage 1

(b) Stage 2

(c) Stage 3

(d) Stage 4

(e) Stage 5

(f) Stage 6

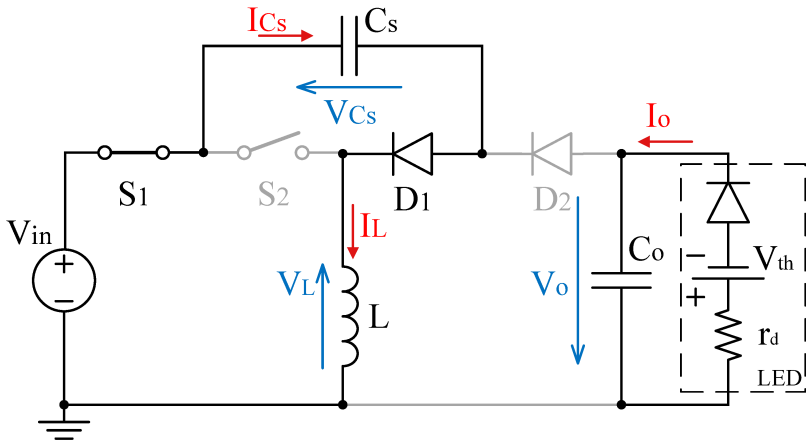
Source: Author (2020).

A.2.2 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor, as highlighted in Figure 95. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = 0 \\ i_L(t_0) = 0 \end{cases} \tag{A.56}$$

Figure 95 – Buck-Boost RSC: stage 1.



Source: Author (2020).

The semiconductor conditions for the first operational stage of the buck-boost converter are shown in Table 21.

Table 21 – Semiconductor Conditions for RSC buck-boost: stage 1.

	State	Voltages	Currents
$\mathbf{S_1}$	Conducting	$v_{S1} = 0$	$i_{S1} = i_L(t)$
$\mathbf{S_2}$	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
$\mathbf{D_2}$	Blocking	$v_{D2} = V_{in} + V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described through (A.57) and (A.58).

Time Domain		Frequency Domain	
$V_{in} = v_{Cs}(t) + L\,\frac{d}{dt} i_L(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + s\,L\,I_L(s)$	(A.57)
$C_s\,\frac{d}{dt} v_{Cs}(t) = i_L$	$\xrightarrow{\mathcal{L}}$	$s\,C_s\,V_{Cs}(s) = I_L(s)$	(A.58)

Substituting the $I_L(s)$ equivalence given in (A.58) at (A.57) and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_{in}}{s}\,\frac{1}{C_s\,L\,s^2 + 1} = \frac{V_{in}}{s}\,\frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.59}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in}\,(1 - \cos(t\,\omega_0)). \tag{A.60}$$

On the other hand, isolating the inductor current from the (A.58) and (A.57) yields

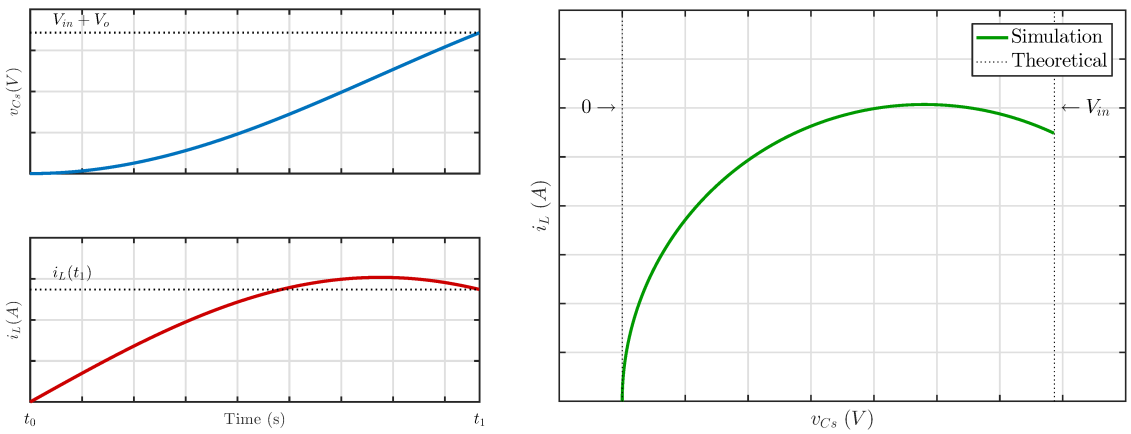
$$I_L(s) = C_s\, V_{in}\, \frac{1}{C_s\, L\, s^2 + 1} = C_s\, V_{in}\, \frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.61}$$

And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\, \omega_0\, V_{in}\, \sin(t\, \omega_0). \tag{A.62}$$

The resulted waveforms described are shown in Figure 96.

Figure 96 – Buck-Boost RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



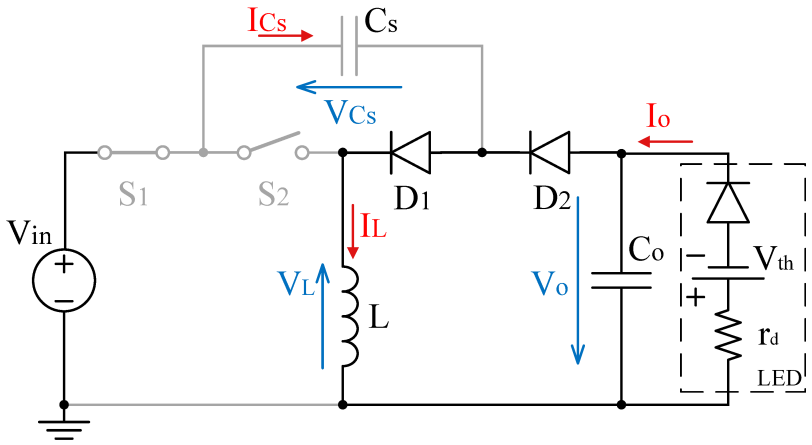
(a) (b)

Source: Author (2020).

When the capacitor reaches sufficient voltage to directly bias the diode D_2 the remaining energy on the inductor forces a current through the passive semiconductors, as shown in Figure 97. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_{in} + V_o \\ i_L(t_1) = I_{L\,(t1)} \end{cases} \tag{A.63}$$

Figure 97 – Buck-Boost RSC: stage 2.



Source: Author (2020).

Semiconductor conditions for stage 2 are found through node and loop equations, being highlighted in Table 22.

Table 22 – Semiconductor Conditions for RSC buck-boost: stage 2.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described by (A.64).

Time Domain		**Frequency Domain**	
$0 = L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$0 = L\,(s\,I_L(s) - I_{L(t1)}) + \frac{V_o}{s}$	(A.64)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max}. \tag{A.65}$$

The inductor behavior can be solved by isolating $I_L(s)$ from (A.64), which yields

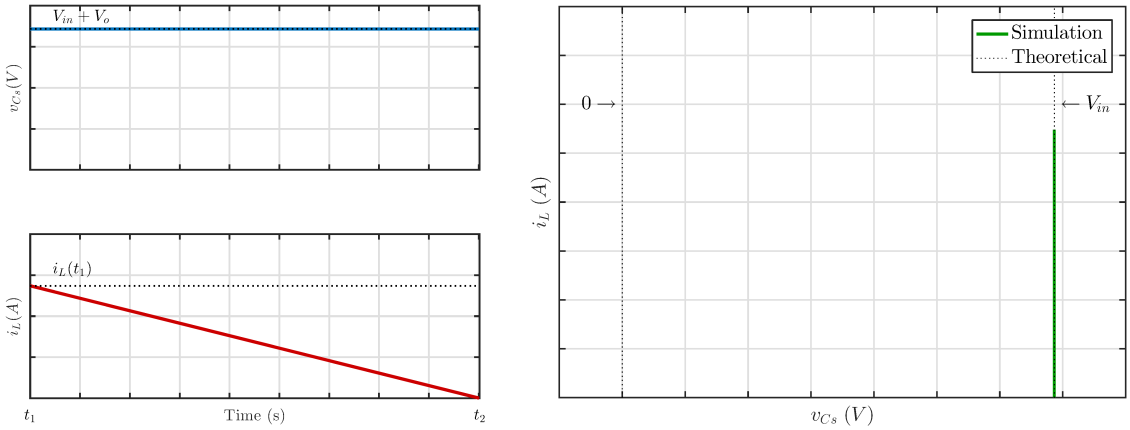
$$I_L(s) = \frac{I_{L(t1)}}{s} - \frac{V_o}{L\,s^2}. \tag{A.66}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_L(t) = I_{L(t1)} - \frac{V_o}{L}\,t. \tag{A.67}$$

The resulted waveforms described are shown in Figure 98.

Figure 98 – Buck-Boost RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



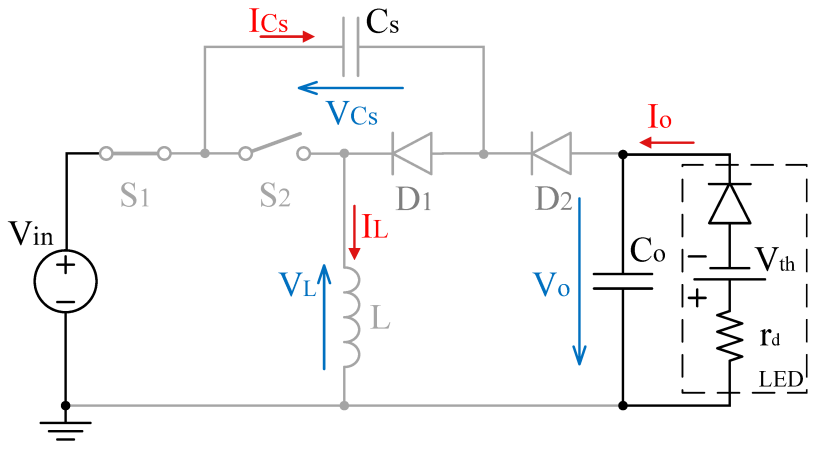
(a) (b)

Source: Author (2020).

This stage is characterized by the complete depletion of energy on the inductor, accordingly to Figure 99. Given the required DCM operation, this study considers that the current on the inductors does reach zero while still on the first half of the switching period. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_{in} + V_o \\ i_L(t_2) = 0 \end{cases} \tag{A.68}$$

Figure 99 – Buck-Boost RSC: stage 3.



Source: Author (2020).

Table 23 describes the semiconductor conditions for this stage/

Table 23 – Semiconductor Conditions for RSC buck-boost: stage 3.

	State	Voltages	Currents
S₁	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S₂	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D₁	Blocking	$v_{D1} = v_{Cs}(t) - V_{in}$	$i_{D1} = 0$
D₂	Blocking	$v_{D2} = V_{in} + V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

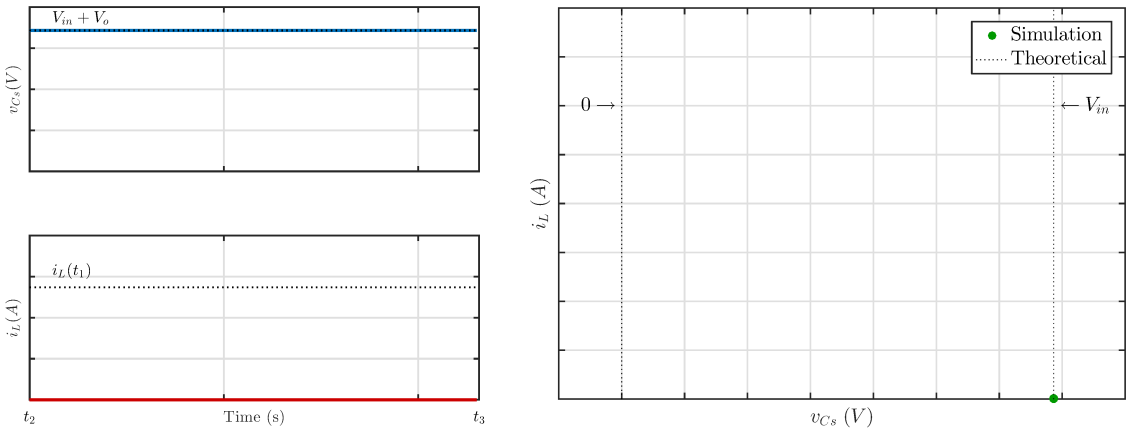
During stage 3 both capacitor voltage and inductor current are constant

$$v_{Cs}(t) = V_{Cs\,max} \tag{A.69}$$

$$i_L(t) = 0. \tag{A.70}$$

The resulted waveforms described are shown in Figure 100.

Figure 100 – Buck-Boost RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



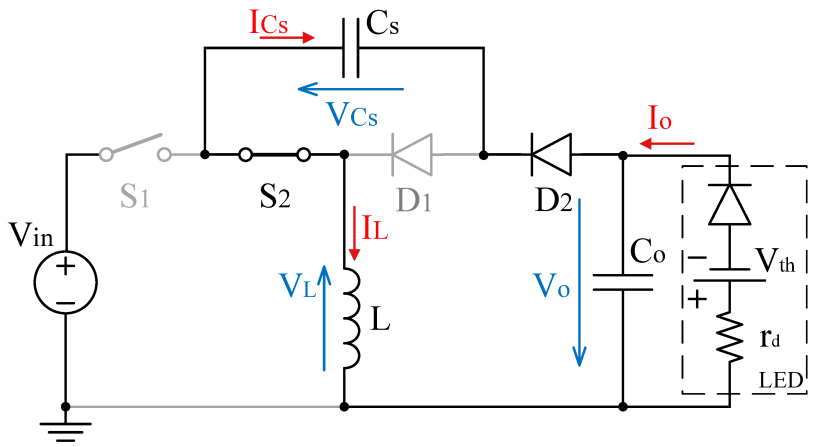
(a) (b)

Source: Author (2020).

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1. The switched capacitor is once again added to the active part of the circuit allowing its storage energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_{in} + V_o \\ i_L(t_3) = 0 \end{cases} \tag{A.71}$$

Figure 101 – Buck-Boost RSC: stage 4.



Source: Author (2020).

The behavior of the semiconductors at stage 4 are summarized in Table 24.

Table 24 – Semiconductor Conditions for RSC buck-boost: stage 4.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} + V_o - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = i_L(t)$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The node and loop equations for this stage are described by (A.72) and (A.73).

Time Domain		Frequency Domain	
$L\,\frac{d}{dt} i_L(t) = v_{Cs}(t) - V_o$	$\xrightarrow{\mathcal{L}}$	$s\,L\,I_L(s) = V_{Cs}(s) - \frac{V_o}{s}$	(A.72)
$C_s\,\frac{d}{dt} v_{Cs}(t) = -i_L$	$\xrightarrow{\mathcal{L}}$	$C_s\,(s\,V_{Cs}(s) - V_{Cs\,max}) = -I_L(s)$	(A.73)

Using both equations and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_o}{s}\,\frac{1}{C_s\,L\,s^2+1} + V_{Cs\,max}\,\frac{C_s\,L\,s}{C_s\,L\,s^2+1} = \frac{V_o}{s}\,\frac{\omega_0^2}{s^2+\omega_0^2} + (V_{in}+V_o)\,\frac{s}{s^2+\omega_0^2}. \quad \text{(A.74)}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_o + V_{in}\,\cos(t\,\omega_0). \quad \text{(A.75)}$$

On the other hand, isolating the inductor current from the (A.72) and (A.73) yields

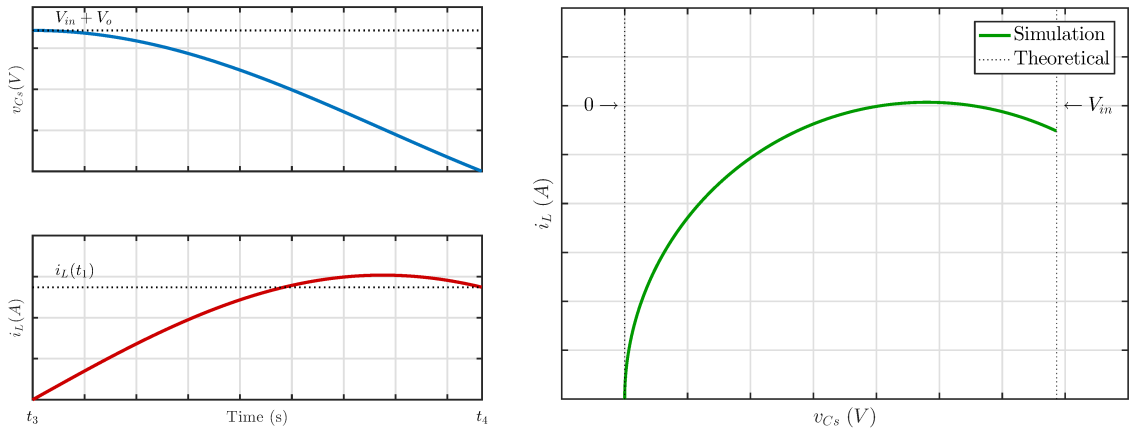
$$I_L(s) = C_s\, V_{in}\, \frac{1}{C_s\, L\, s^2 + 1} = C_s\, V_{in}\, \frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.76}$$

And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_L(t) = C_s\, \omega_0\, V_{in}\, \sin(t\, \omega_0). \tag{A.77}$$

The resulted waveforms described are shown in Figure 102.

Figure 102 – Buck-Boost RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



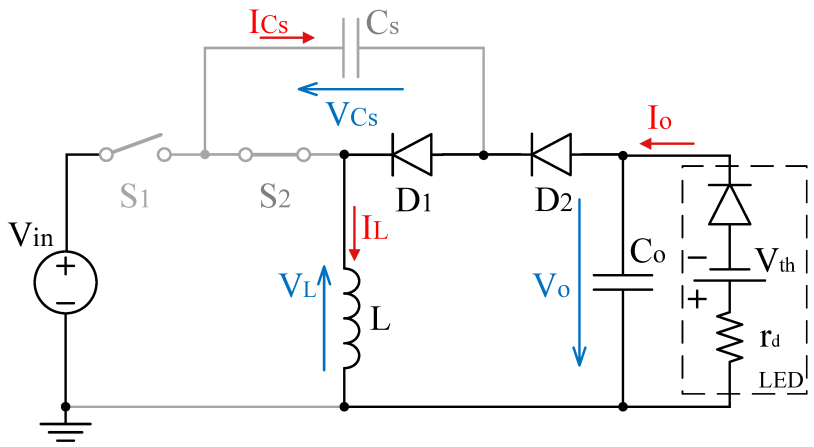
(a) (b)

Source: Author (2020).

With the complete discharge of the switched capacitor its voltage is maintained in zero, allowing the diode D_1 to be forward biased, as shown in Figure 103. Once again, remnant energy on the inductor forces a current flow into both diodes. The initial conditions to this stage are described by

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = 0 \\ i_L(t_4) = I_{L\,(t4)} \end{cases} \tag{A.78}$$

Figure 103 – Buck-Boost RSC: stage 5.



Source: Author (2020).

The descriptions of each semiconductor is shown in Table 25.

Table 25 – Semiconductor Conditions for RSC buck-boost: stage 5.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} + V_o - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_L(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_L(t)$

Source: Author (2020).

The loop equation for this stage is described as (A.79)

Time Domain		Frequency Domain	
$0 = L\,\frac{d}{dt} i_L(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$0 = L\,(s\,I_L(s) - I_{L(t4)}) + \frac{V_o}{s}$	(A.79)

With the capacitor completely discharged, its voltage remains zero

$$v_{Cs}(t) = V_{Cs\,min} = 0. \tag{A.80}$$

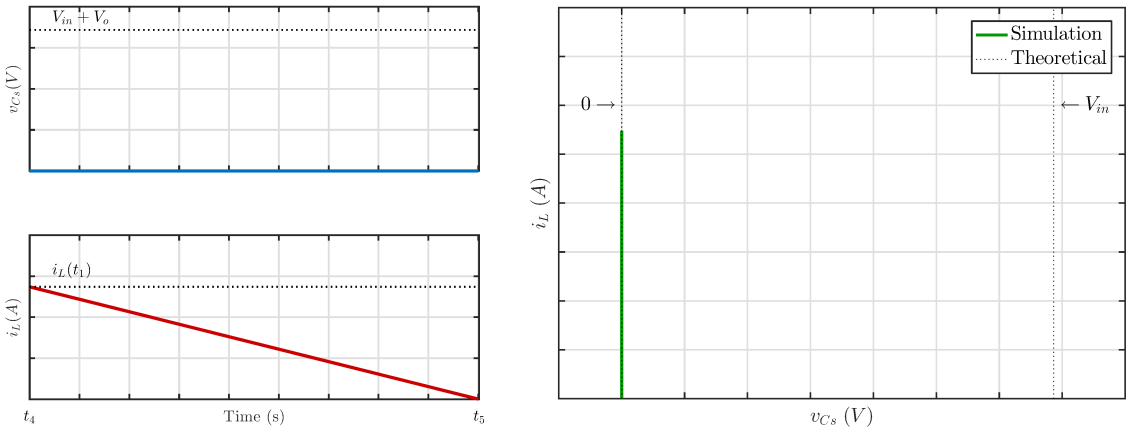
The inductor behavior can be solved by isolating $I_L(s)$ from (A.79), which yields

$$I_L(s) = \frac{I_{L(t4)}}{s} - \frac{V_o}{L\,s^2}. \tag{A.81}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_L(t) = I_{L(t4)} - \frac{V_o}{L}\,t. \tag{A.82}$$

Figure 104 – Buck-Boost RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

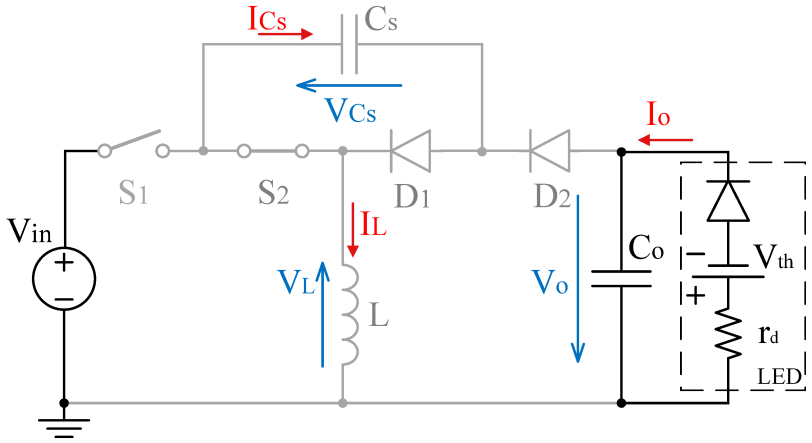
Source: Author (2020).

The resulted waveforms described are shown in Figure 104.

Finally, with the end of the energy at the inductors, its current reaches zero before the ending of the switching cycle, nulling the current through the components as shown in Figure 105. The time delay between these two events characterizes the stage 6, which presents as initial condition the following

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = 0 \\ i_L(t_5) = 0 \end{cases} \tag{A.83}$$

Figure 105 – Buck-Boost RSC: stage 6.



Source: Author (2020).

Through node and loop equations the descriptions of the semiconductors during stage 6 are found and displayed at Table 26.

Table 26 – Semiconductor Conditions for RSC buck-boost: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

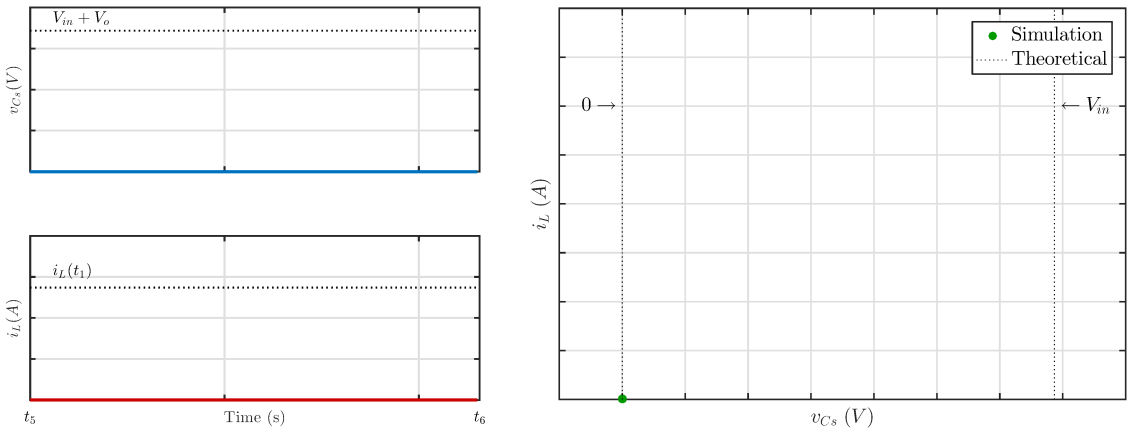
During stage 6 both capacitor voltage and inductor current are constant

$$v_{Cs}(t) = V_{Cs\,min} = 0 \tag{A.84}$$

$$i_L(t) = 0. \tag{A.85}$$

The resulted waveforms described are shown in Figure 106.

Figure 106 – Buck-Boost RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.2.3 Time Analysis

In order to fully characterize the behavior of the converter, the time of each state must be determined.

A.2.3.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using the Eq (A.60) it is known

that

$$v_{Cs}(t_1) = V_{in}\,(1 - \cos(t_1\,\omega_0)) = V_{in} + V_o. \tag{A.86}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$:

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{-V_o}{V_{in}}\right) = \frac{1}{\omega_0}\,acos\,(-G)\,. \tag{A.87}$$

Applying the time duration for stage 1 into (A.62) it is possible to find the inductor current by the end of such stage which is required as one of the initial conditions for stage 2:

$$i_L(t_1) = C_s\,\omega_0\,V_{in}\,\sin(\Delta t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin\left(\frac{1}{\omega_0}\,acos(-G)\,\omega_0\right). \tag{A.88}$$

The result is given by (A.89):

$$I_{L\,t1} = C_s\,V_{in}\,\omega_0\,\sqrt{1 - G^2}. \tag{A.89}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1 - G^2 > 0$, which results in a design requirement given in (A.90):

$$G < 1. \tag{A.90}$$

A.2.3.2 Stages 2 and 5

The second stage is characterized by the discharge of the remnant energy on the inductors. From (A.67) and (A.89) it is known that

$$i_L(t_2) = I_{L(t1)} - \frac{V_o}{L}\,\Delta t_2 = C_s\,V_{in}\,\omega_0\,\sqrt{1 - G^2} - \frac{V_o}{L}\,\Delta t_2 = 0. \tag{A.91}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,G}\,\sqrt{1 - G^2}. \tag{A.92}$$

A.2.3.3 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}. \tag{A.93}$$

Which expands to

$$\frac{1}{\omega_0}\,acos\,(-G) + \frac{1}{\omega_0\,G}\,\sqrt{1 - G^2} < \frac{1}{2\,f_s}. \tag{A.94}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\,f_s\,\left(acos\,(-G) + \frac{1}{G}\,\sqrt{1 - G^2}\right). \tag{A.95}$$

A.2.4 Average Inductor Current

The average inductor current is found by integrating the current waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period:

$$I_L = \frac{1}{T_s/2}\left(\int_{t_0}^{t_1} i_L(t)_1 dt + \int_{t_1}^{t_2} i_L(t)_2 dt\right), \tag{A.96}$$

that is,

$$I_L = 2\,f_s\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{L(t1)} - \frac{V_o}{L}\,t\,dt\right). \tag{A.97}$$

Solving the equation above and making use of the relations given by (A.87), (A.89) and (A.92), the average output current can be simplified as (A.98):

$$I_L = C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}. \tag{A.98}$$

A.2.5 Average Output Current

For the buck-boost converter, the output current is the same as the current at diode D_2. Integrating its waveform over a period of time equal to the switching period yields the average output current:

$$\begin{aligned} I_o = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{D2}(t)_1 dt + \int_{t_1}^{t_2} i_{D2}(t)_2 dt + \int_{t_2}^{t_3} i_{D2}(t)_3 dt \\ &+ \int_{t_3}^{t_4} i_{D2}(t)_4 dt + \int_{t_4}^{t_5} i_{D2}(t)_5 dt + \int_{t_5}^{t_6} i_{D2}(t)_6 dt\Bigg) \end{aligned} \tag{A.99}$$

$$I_o = f_s\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + 2\cdot\int_{t_1}^{t_2} I_{L(t1)} - \frac{V_o}{L}\,t\,dt\right). \tag{A.100}$$

Solving the equation above and making use of the relations given by (A.87), (A.89) and (A.92), the average output current can be simplified as (A.101):

$$I_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}. \tag{A.101}$$

A.2.6 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\,V_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}\,V_o. \tag{A.102}$$

Using the static gain definition stated as $V_o = G\,V_{in}$ the output power is given by

$$P_o = C_s\,f_s\,V_{in}^2\,(G+1). \tag{A.103}$$

The capacitor must be sized accordingly to the output power, using the relation given by (A.104):

$$C_s = \frac{P_o}{f_s\,V_{in}^2\,(G+1)}. \tag{A.104}$$

A.2.7 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 27.

Table 27 – RSC buck-boost simulation values for (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

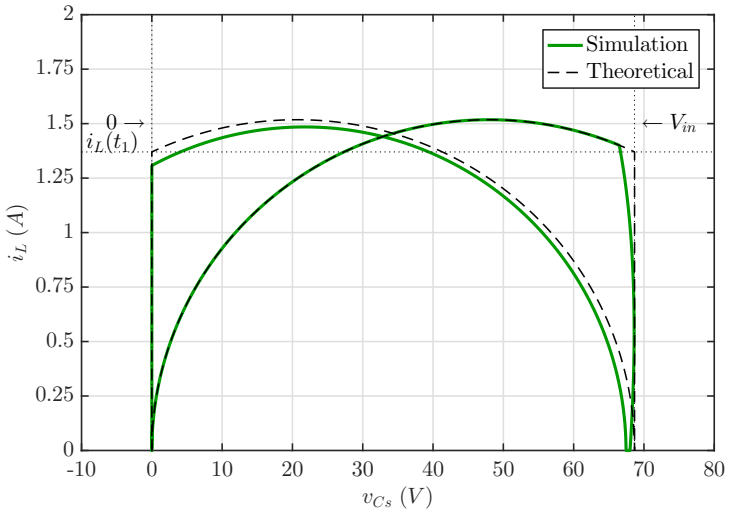
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$6.8\,nF$
Inductance	L	$6.8\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 107 yields a precise comparison between theoretical prediction and simulation result, highlighting specially the slightly lower current during the discharging stage 4.

Figure 107 – State Plan for the RSC buck-boost converter.

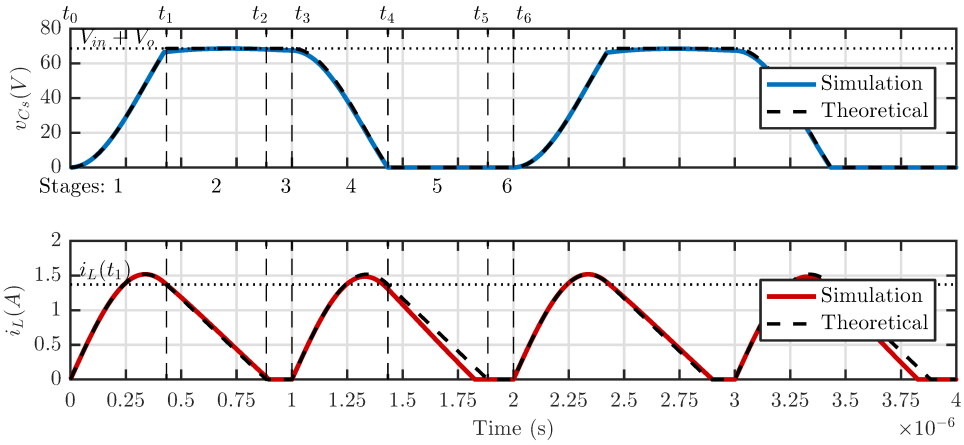


Source: Author (2020).

Thus, the waveform comparison of the RSC buck-boost converter states for each stage in their respective timespans is shown in Figure 108. In the time domain, only a small difference can be perceived in stage 5, where the demagnetizing of the inductor happens somewhat faster then theoretically predicted. Finally, Figure 109 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can

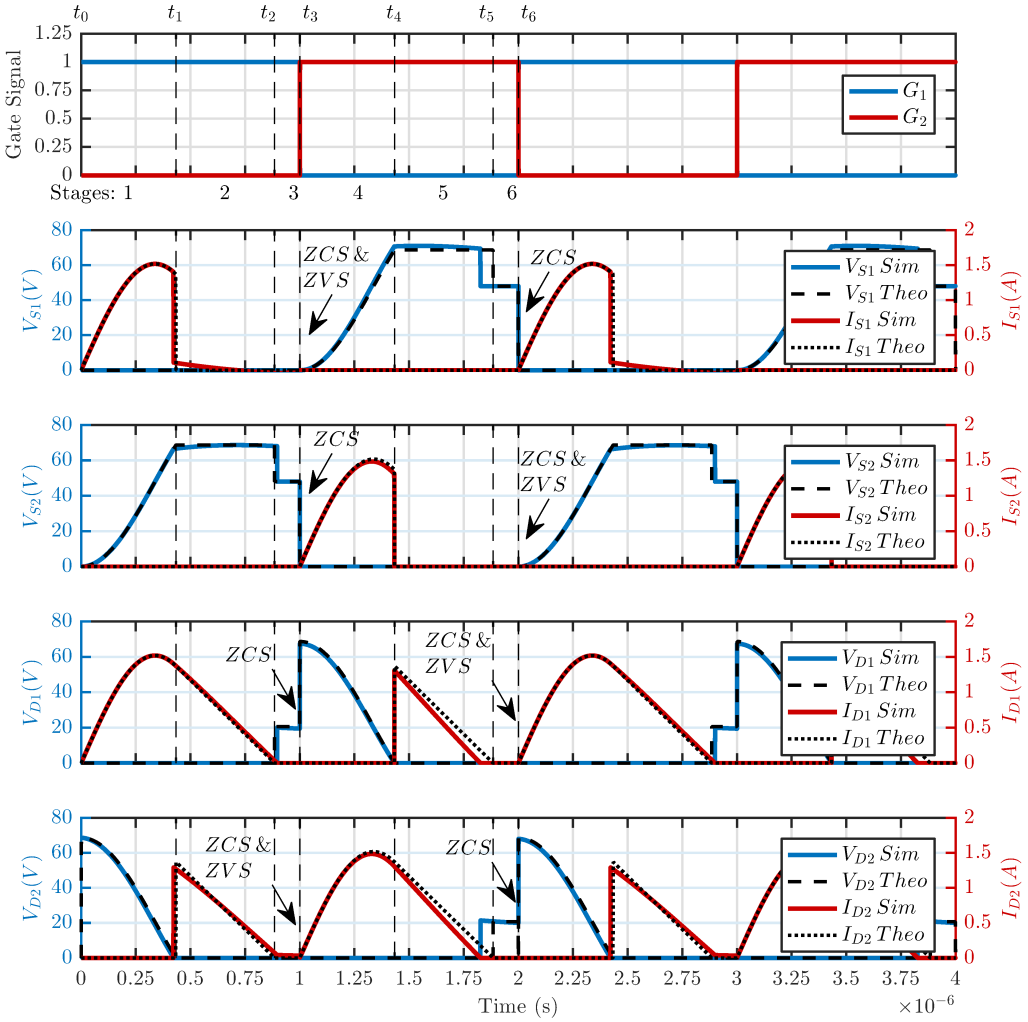
be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 108 – Theoretical waveforms of the state variables for the RSC buck-boost converter.



Source: Author (2020).

Figure 109 – Soft-switching on the semiconductors for the RSC buck-boost converter.



Source: Author (2020).

A.3 RSC FLYBACK ANALYSIS

The buck-boost topology presents a unique characteristic of interest regarding the magnetizing element: unlike the buck and boost topologies, where the inductor current is locked to either the output or input loops respectively, the buck-boost topology is such that the inductor current alternates between input and output loops depending on the switch state. This property allows that the input and output loops at the buck-boost converter to be physically separated by the use of two coupled inductors, creating a galvanic isolation.

This isolation serves many purposes and is greatly appreciated due to safety reasons: faults occurring at the load are stopped from causing damage in the input of the circuit, and high voltages from line input are blocked to be directly accessed at the output.

Additionally, the introduction of a transformer provides a new degree of flexibility for the circuit designer due to the turns ratio a of the transformer. This allows that the overall static gain G is a result of both duty cycle d and turns-ratio a, giving more freedom for the designer to choose optimal values of duty cycle.

This section will therefore expand on the RSC buck-boost topology presented before by adding a transformer as magnetizing element, thus developing an RSC flyback converter. It is important to highlight, however, that due to the inclusion of the switched capacitor C_s, this topology is not galvanic isolated as the classic flyback converter.

Variables used exclusively in this section are described in 28. With the intent to simplify the analysis, the transformer model will be based on an ideal transformer with an inductor in parallel with the primary coil representing its magnetizing inductance L_{mp}. Therefore, the resonant frequency will be declared as

$$\omega_0 = \sqrt{\frac{1}{L_{mp}\, C_r}}. \tag{A.105}$$

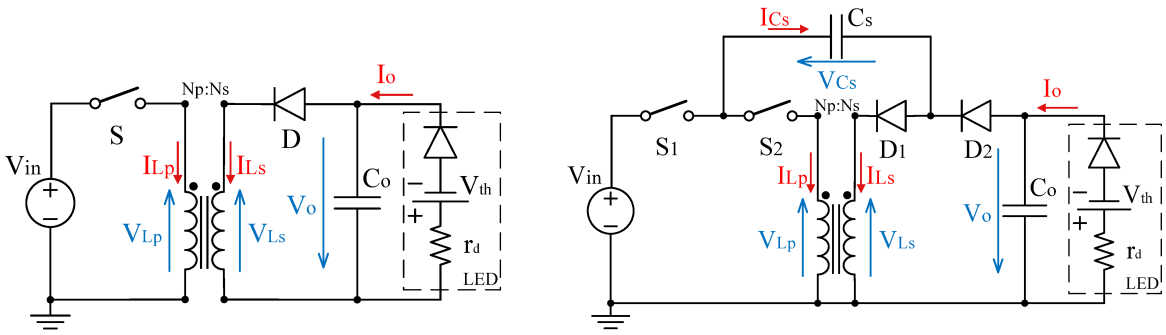
The classic flyback converter is shown on Figure 110 alongside the RSC flyback converter. The lack of galvanic isolation is made clear by the required physical connection between primary and secondary of the transformer that allows a closed current path on the switched capacitor C_s.

Table 28 – Variables pertinent to the RC flyback analysis.

Variable	Description	Equation
N_p	Number of turns at primary coil	$N_p = a\,N_s$
N_s	Number of turns at secondary coil	$N_s = (1/a)\,N_p$
a	turns-ratio	$a = N_p/N_s$
V_p	Current at primary coil	$I_{Lp} = (1/a)\,I_{Ls}$
I_{Ls}	Current at secondary coil	$I_{Ls} = a\,I_{Lp}$
V_{Lp}	Voltage at primary coil	$V_{Lp} = a\,V_{Ls}$
V_{Ls}	Voltage at secondary coil	$V_{Ls} = (1/a)\,V_{Lp}$
L_{mp}	Magnetizing inductance from the primary side	$L_{mp} = a^2\,L_{ms}$
L_{ms}	Magnetizing inductance from the secondary side	$L_{ms} = (1/a)^2\,L_{mp}$
I_{Lm}	Current at the magnetizing inductance L_{mp}	$I_{Lm} = I_{Lp} = (1/a)\,I_{Ls}$

Source: Author (2020).

Figure 110 – Classic flyback converter (a) and RSC flyback converter (b).



(a) (b)

Source: Author (2020).

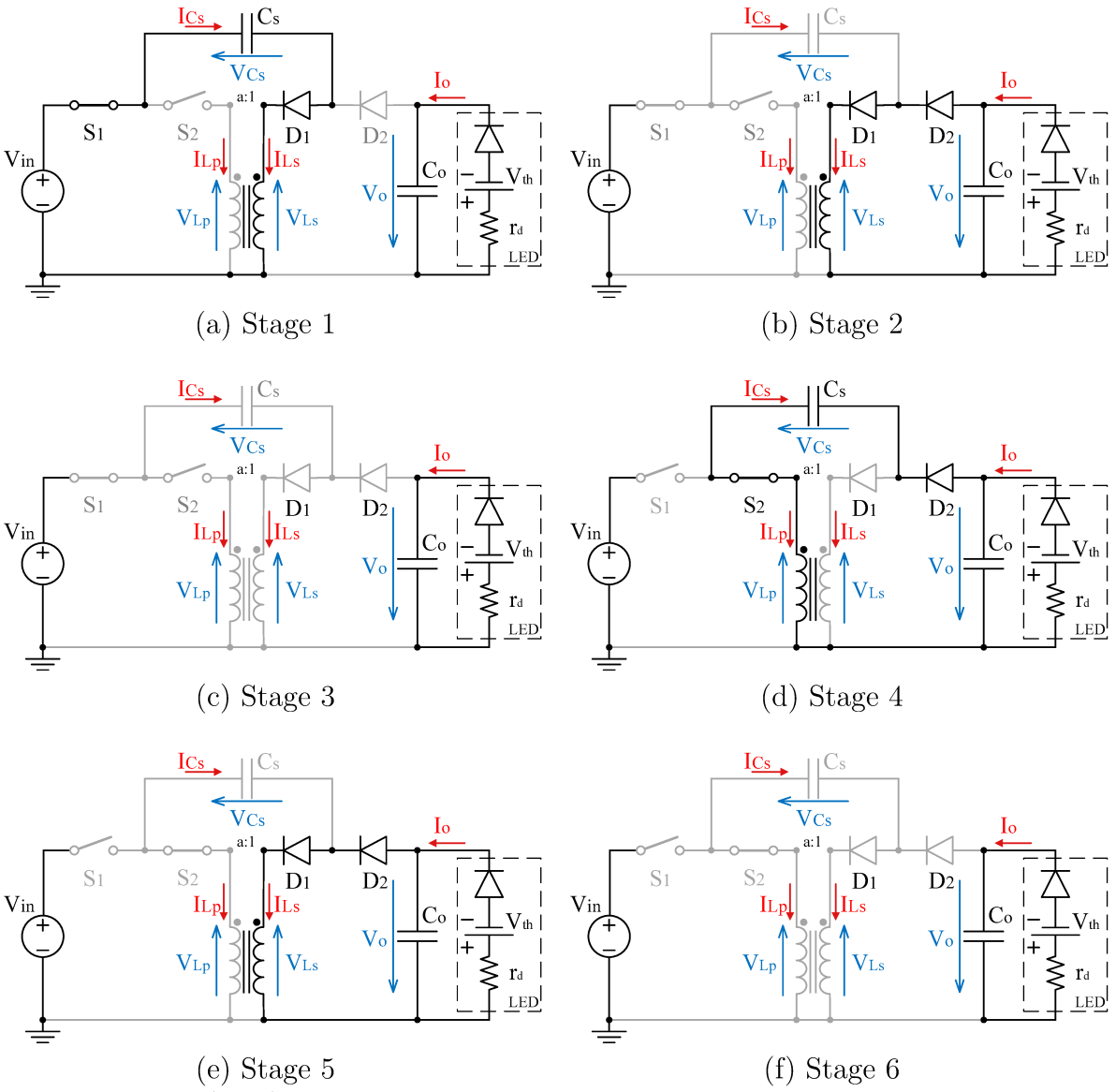
The six distinct stages are highlighted in Figure 111.

A.3.1 Switched capacitor analysis

The RSC flyback converter, as the previously described RSC converters, will also present a voltage-varying switched capacitor C_s, and its maximum and minimum values are important to determine as they are important for the initial states of the operational analysis. In stage 1, described in Figure 112a, the reverse biased diode is D_2. Therefore, the appropriate loop to analyze is composed by $[V_{in} - S_1 - C_s - D_2 - V_o]$. The voltage at the diode D_2 is described as

$$v_{D2}(t) = V_{in} - v_{Cs}(t) + V_o. \tag{A.106}$$

Figure 111 – Stages of operation of the RSC flyback converter.



(a) Stage 1 (b) Stage 2

(c) Stage 3 (d) Stage 4

(e) Stage 5 (f) Stage 6

Source: Author (2020).

Similarly, stage 4, displayed in Figure 112d, must be analyzed accordingly to the diode D_1. The only available voltage loop will include both sides of the transformer, and therefore, in order to properly simplify the equation, both voltage loops must be mathematically described: $[S_2 - C_s - V_{Lp} - D_1]$ and $[V_{Ls} - D_1 - V_o]$. Once the voltages at the transformer can be related linearly through the turns-ratio a, the voltage at the reverse biased diode D_1 can be simplified as

$$v_{D1}(t) = \frac{1}{a}\, v_{Cs}(t) - \frac{1}{a}(1-a)\, V_o. \tag{A.107}$$

Which means that diode D_1 is able to conduct when switched capacitor C_s discharges down to $V_{Cs} = (1-a)\, V_o$. Therefore, minimum and maximum voltages at the

switched capacitor C_s can be summarized by

$$V_{Cs\,max} = V_{in} + V_o \; ; \; V_{Cs\,min} = (1-a)\,V_o. \tag{A.108}$$

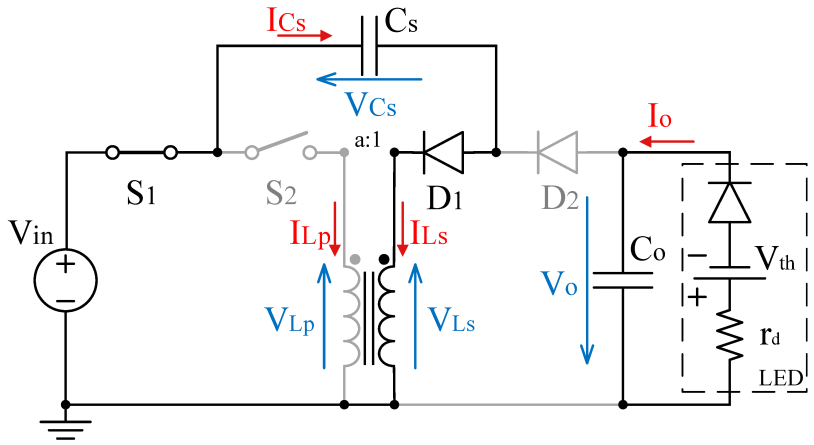
The operational analysis can now be described given the initial stages of the V_{Cs} state.

A.3.2 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor through the primary of the transformer as shown in Figure 112. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = V_o\,(1-a) \\ i_{Lm}(t_0) = 0. \end{cases} \tag{A.109}$$

Figure 112 – Flyback RSC: stage 1.



Source: Author (2020).

The loop and node equations for the given active circuit yields the voltage and current conditions at the semiconductors, described in Table 29.

Table 29 – Semiconductor Conditions for RSC flyback: stage 1.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = i_{Ls}(t)$
S_2	Blocking	$v_{S2} = (1-a)\,V_{in} + a\,v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{Ls}(t)$
D_2	Blocking	$v_{D2} = V_{in} + V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described by (A.110) and (A.111).

Time Domain		Frequency Domain	
$V_{in} = v_{Cs}(t) + L_{ms}\,\frac{d}{dt} i_{Ls}(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + s\,\frac{1}{a}\,L_{mp}\,I_{Lm}(s)$	(A.110)
$C_s\,\frac{d}{dt} v_{Cs}(t) = i_{Ls}$	$\xrightarrow{\mathcal{L}}$	$C_s(s\,V_{Cs}(s) - V_{Cs\,t0}) = a\,I_{Lm}(s)$	(A.111)

Substituting the $I_{Lm}(s)$ equivalence given in (A.110) at (A.111) and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_{in}}{s}\,\frac{a^2\,\omega_0^2}{s^2 + a^2\,\omega_0^2} + V_o\,(1-a)\,\frac{s}{s^2 + a^2\,\omega_0^2}. \tag{A.112}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in} + [(1-a)\,V_o - V_{in}]\cos(t\,a\,\omega_0). \tag{A.113}$$

On the other hand, isolating the inductor current from the (A.110) and (A.111) yields

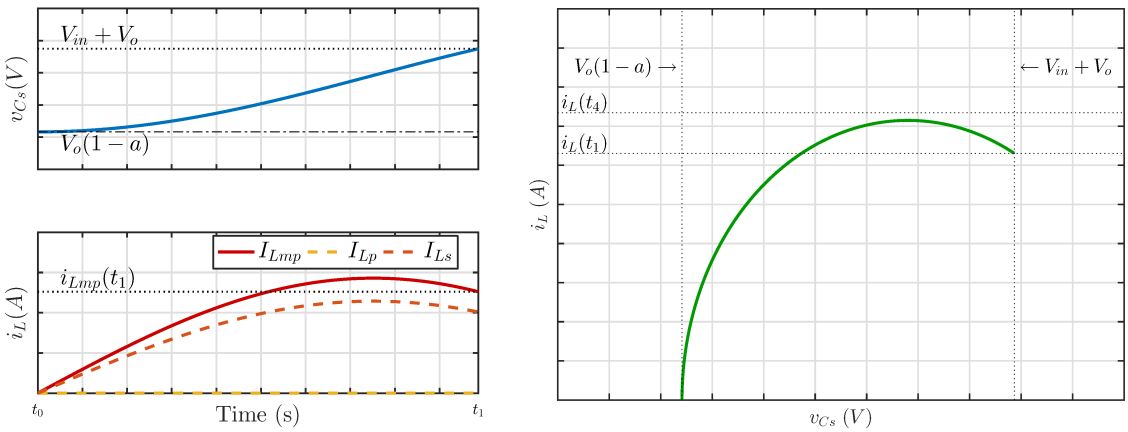
$$I_{Lm}(s) = C_s\,[V_{in} + V_o\,(a-1)]\,a\,\frac{\omega_0^2}{s^2 + a^2\,\omega_0^2}. \tag{A.114}$$

And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_{Lm}(t) = C_s\,\omega_0\,[V_{in} + V_o\,(a-1)]\,\sin(t\,a\,\omega_0). \tag{A.115}$$

The resulted waveforms described are shown in Figure 113.

Figure 113 – Flyback RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

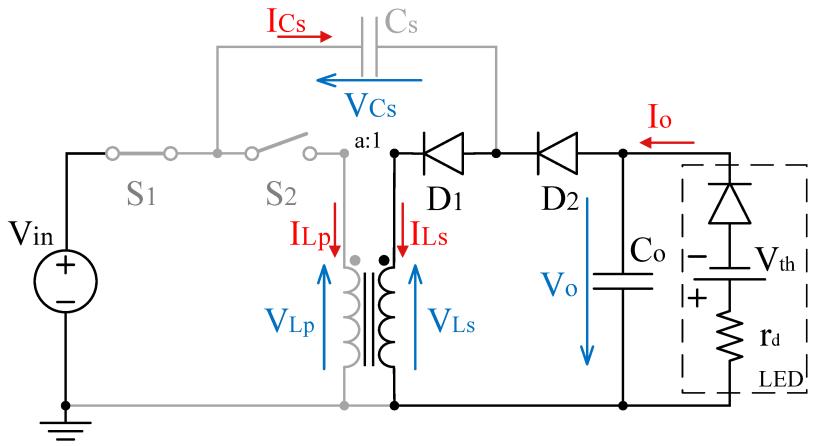
Source: Author (2020).

When the capacitor reaches sufficient voltage to forward bias the diode D_2 the remaining energy on the inductor forces a current through the passive semiconductors

as shown in Figure 114. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_{in} + V_o \\ i_{Lm}(t_1) = I_{Lm\,(t1)} \end{cases} \tag{A.116}$$

Figure 114 – Flyback RSC: stage 2.



Source: Author (2020).

Semiconductor conditions for this stage are summarized in Table 30.

Table 30 – Semiconductor Conditions for RSC flyback: stage 2.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = (1-a)\,V_{in} + a\,v_{Cs}(t)$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{Ls}(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{Ls}(t)$

Source: Author (2020).

The loop equation for this stage is described by (A.117).

Time Domain		Frequency Domain	
$0 = L_{ms}\,\frac{d}{dt} i_{Ls}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$0 = \frac{1}{a}\,L_{mp}\,(s\,I_{Lm}(s) - I_{Lm(t1)}) + \frac{V_o}{s}$	(A.117)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max} = V_{in} + V_o. \tag{A.118}$$

The inductor behavior can be solved by isolating $I_{Lm}(s)$ from (A.117), which yields

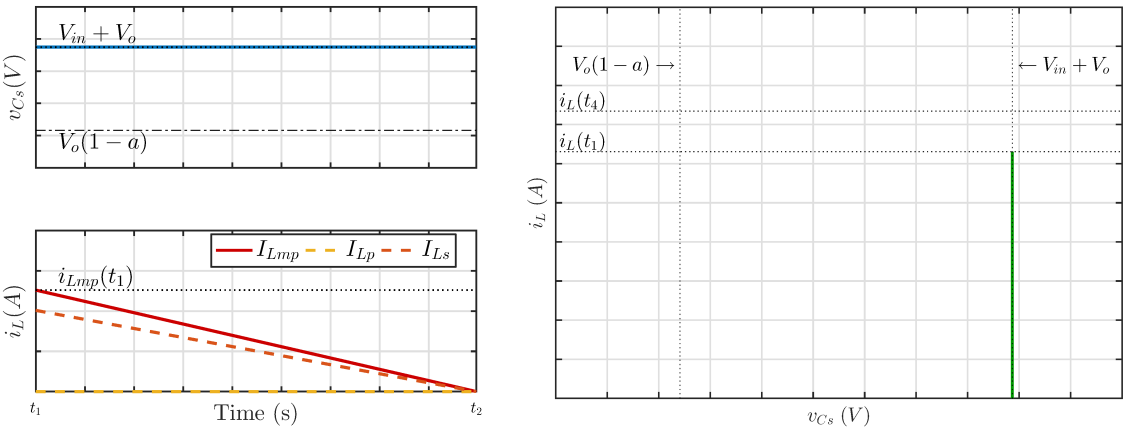
$$I_{Lm}(s) = \frac{I_{Lm(t1)}}{s} - a\,\frac{V_o}{L_{mp}\,s^2}. \tag{A.119}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{Lm}(t) = I_{Lm(t1)} - a\,\frac{V_o}{L_{mp}}\,t. \tag{A.120}$$

The resulted waveforms described are shown in Figure 115.

Figure 115 – Flyback RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



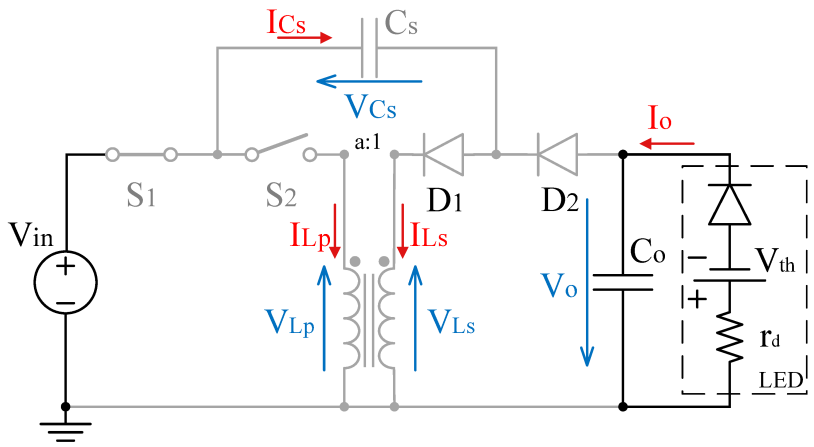
(a) (b)

Source: Author (2020).

This stage is characterized by the complete depletion of energy on the magnetizing element, resulting in the circuit describe d in Figure 116. Given the required DCM operation, this study considers that the current on the inductors does reach zero while still on the first half of the switching period. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_{in} + V_o \\ i_{Lm}(t_2) = 0 \end{cases} \tag{A.121}$$

Figure 116 – Flyback RSC: stage 3.



Source: Author (2020).

Table 31 displays the current and voltage conditions at the semiconductor for such stage.

Table 31 – Semiconductor Conditions for RSC flyback: stage 3.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t) - V_{in}$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_{in} + V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor current are constant.

$$v_{Cs}(t) = V_{Cs\,max} \tag{A.122}$$

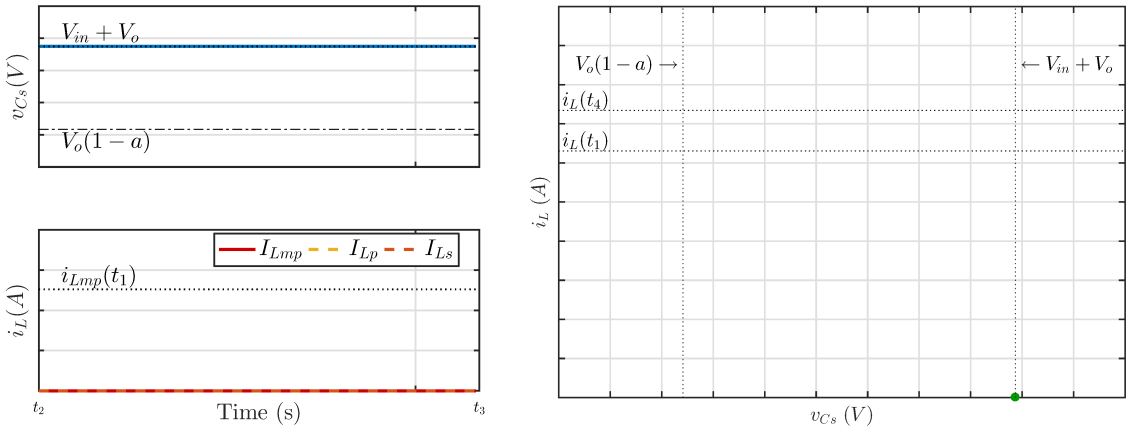
$$i_{Lm}(t) = 0. \tag{A.123}$$

The resulted waveforms described are shown in Figure 117.

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1, accordingly to Figure 118. The switched capacitor is once again added to the active part of the circuit allowing its storage energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_{in} + V_o \\ i_{Lm}(t_3) = 0 \end{cases} \tag{A.124}$$

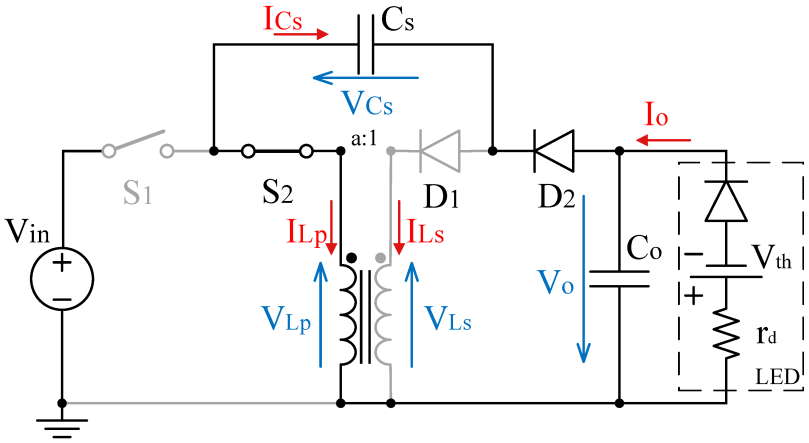
Figure 117 – Flyback RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

Figure 118 – Flyback RSC: stage 4.



Source: Author (2020).

The semiconductor condition for this stage are described in Table 32.

Table 32 – Semiconductor Conditions for RSC flyback: stage 4.

	State	Voltages	Currents
$\mathbf{S_1}$	Blocking	$v_{S1} = V_{in} + V_o - v_{Cs}(t)$	$i_{S1} = 0$
$\mathbf{S_2}$	Conducting	$v_{S2} = 0$	$i_{S2} = i_{Lp}(t)$
$\mathbf{D_1}$	Blocking	$v_{D1} = (1 - 1/a)\, V_o + (1/a)\, v_{Cs}(t)$	$i_{D1} = 0$
$\mathbf{D_2}$	Conducting	$v_{D2} = 0$	$i_{D2} = i_{Lp}(t)$

Source: Author (2020).

The node and loop equations for this stage are described through (A.125) and (A.126).

Time Domain		Frequency Domain	
$L_{mp}\,\frac{d}{dt}i_{Lp}(t) = v_{Cs}(t) - V_o$	$\xrightarrow{\mathcal{L}}$	$s\,L_{mp}\,I_{Lm}(s) = V_{Cs}(s) - \frac{V_o}{s}$	(A.125)
$C_s\,\frac{d}{dt}v_{Cs}(t) = -i_{Lp}$	$\xrightarrow{\mathcal{L}}$	$C_s\,(s\,V_{Cs}(s) - V_{Cs\,max}) = -I_{Lm}(s)$	(A.126)

Using both equations and isolating the capacitor voltage yields

$$V_{Cs}(s) = \frac{V_o}{s}\,\frac{1}{C_s\,L_{mp}\,s^2+1} + V_{Cs\,max}\,\frac{C_s\,L_{mp}\,s}{C_s\,L_{mp}\,s^2+1} = \frac{V_o}{s}\,\frac{\omega_0^2}{s^2+\omega_0^2} + (V_{in}+V_o)\,\frac{s}{s^2+\omega_0^2}. \tag{A.127}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_o + V_{in}\,\cos(t\,\omega_0). \tag{A.128}$$

On the other hand, isolating the inductor current from the (A.125) and (A.126) yields

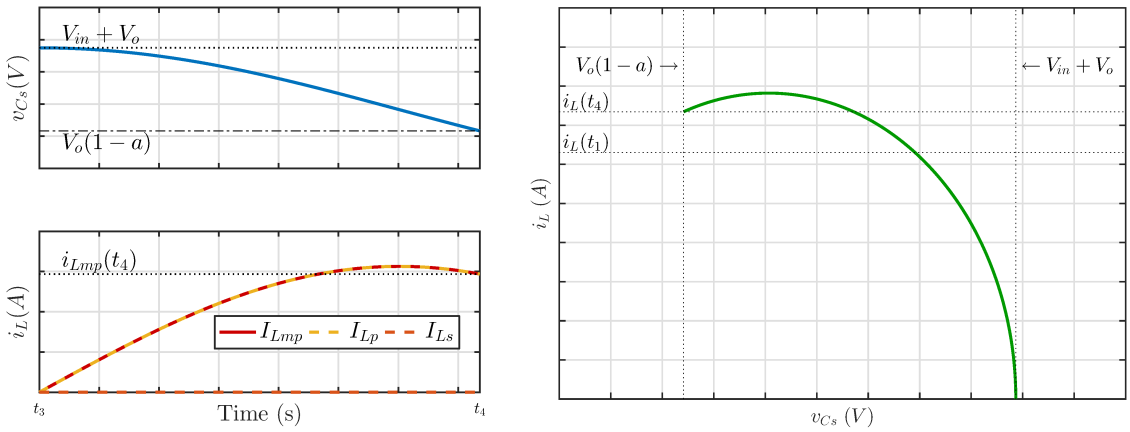
$$I_{Lm}(s) = C_s\,V_{in}\,\frac{1}{C_s\,L_{mp}\,s^2+1} = C_s\,V_{in}\,\frac{\omega_0^2}{s^2+\omega_0^2}. \tag{A.129}$$

And finally, the inverse Laplace transforms gives the inductor current at the time domain as

$$i_{Lm}(t) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.130}$$

The resulted waveforms described are shown in Figure 119.

Figure 119 – Flyback RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

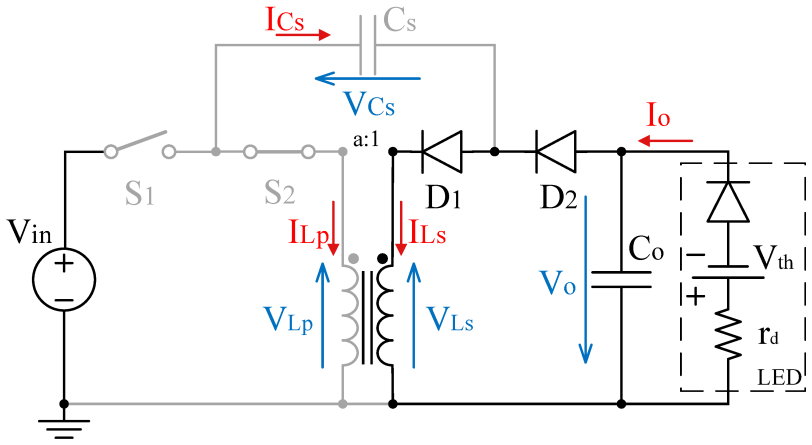
Source: Author (2020).

With the complete discharge of the switched capacitor its voltage is maintained in zero and no current flows through it, as shown in Figure 120. Once again, remnant energy

on the inductor forward bias both diodes creating a current flow in order to discharge it

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = V_o\,(1-a) \\ i_{Lm}(t_4) = I_{Lm\,(t1)}. \end{cases} \tag{A.131}$$

Figure 120 – Flyback RSC: stage 5.



Source: Author (2020).

Stage 5 conditions for the semiconductors are summarized in Table 33.

Table 33 – Semiconductor Conditions for RSC flyback: stage 5.

	State	Voltages	Currents
S1	Blocking	$v_{S1} = V_{in} + V_o - v_{Cs}(t)$	$i_{S1} = 0$
S2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{Ls}(t)$
D2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{Ls}(t)$

Source: Author (2020).

The loop equation for this stage is described as (A.132).

Time Domain		Frequency Domain	
$0 = L_{ms}\,\frac{d}{dt} i_{Lms}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$0 = \frac{1}{a}\,L_{mp}\,(s\,I_{Lm}(s) - I_{Lm(t4)}) + \frac{V_o}{s}$	(A.132)

With the capacitor completely discharged, its voltage remains zero

$$v_{Cs}(t) = V_{Cs\,min} = 0. \tag{A.133}$$

The inductor behavior can be solved by isolating $I_{Lm}(s)$ from (A.132), which yields

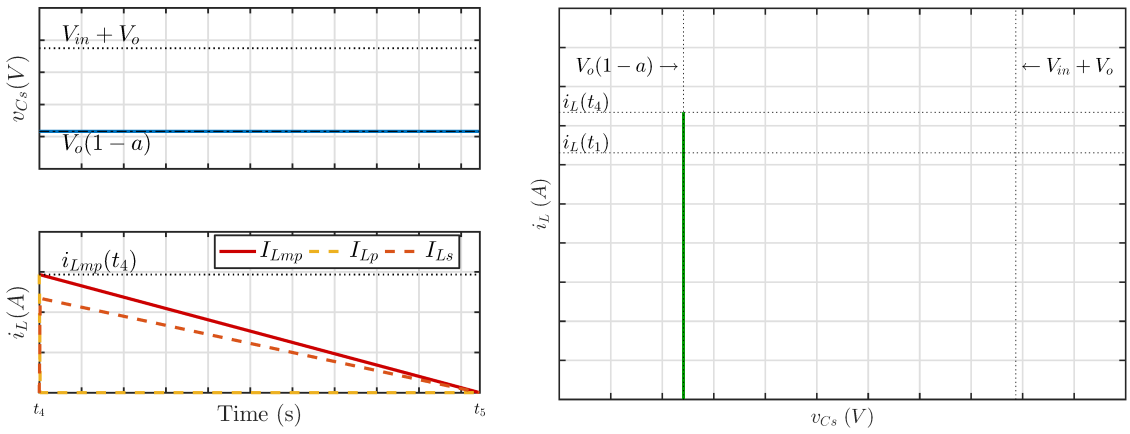
$$I_{Lm}(s) = \frac{I_{Lm(t4)}}{s} - a\,\frac{V_o}{L_{mp}\,s^2}. \tag{A.134}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{Lm}(t) = I_{Lm(t4)} - a\,\frac{V_o}{L_{mp}}\,t. \tag{A.135}$$

The resulted waveforms described are shown in Figure 121.

Figure 121 – Flyback RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



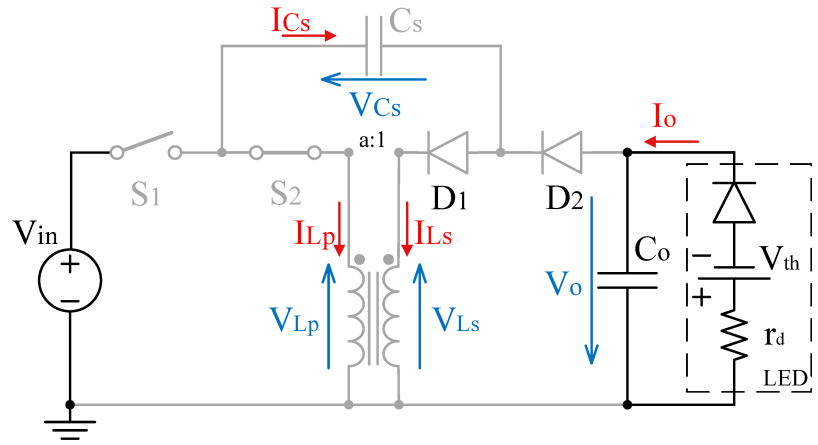
(a) (b)

Source: Author (2020).

Finally, with the end of the energy at the inductors, its current reaches zero before the ending of the switching cycle, resulting in Figure 122. The time between these two events characterizes the stage 6, which presents as initial condition the following

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = V_o\,(1-a) \\ i_{Lm}(t_5) = 0. \end{cases} \tag{A.136}$$

Figure 122 – Flyback RSC: stage 6.



Source: Author (2020).

Table 34 displays the current and voltage conditions at each semiconductor for this stage.

Table 34 – Semiconductor Conditions for RSC flyback: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage 6 both capacitor voltage and inductor current are constant

$$v_{Cs}(t) = V_{Cs\,min} = V_o\,(1 - a) \tag{A.137}$$

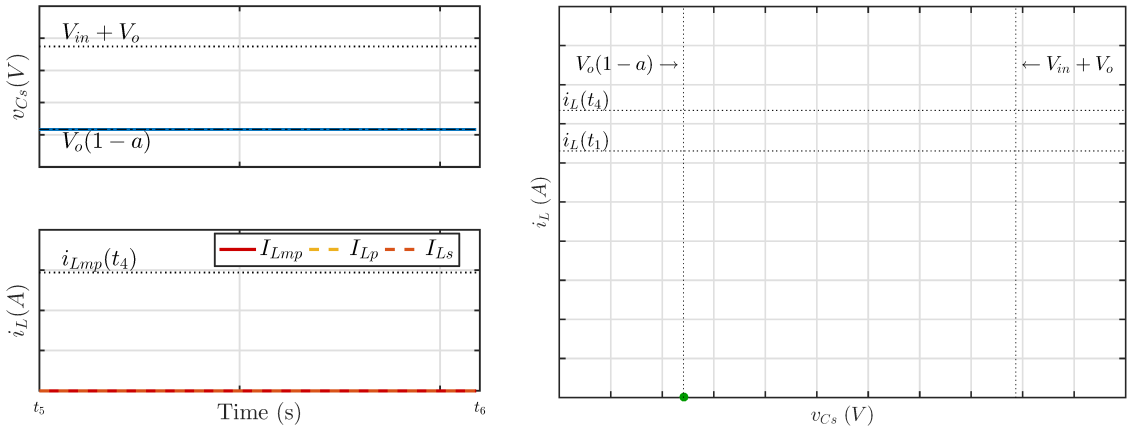
$$i_{Lm}(t) = 0. \tag{A.138}$$

The resulted waveforms described are shown in Figure 123.

A.3.3 Time Analysis

In order to fully characterize the behavior of the converter, the time of each state must be determined.

Figure 123 – Flyback RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.3.3.1 Stage 1

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using the Eq (A.113) it is known that

$$v_{Cs}(t_1) = V_{in} + [(1-a)\,V_o - V_{in}]\cos(\Delta t_1\, a\,\omega_0) = V_{in} + V_o. \tag{A.139}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$:

$$\Delta t_1 = t_1 - t_0 = \frac{1}{a\,\omega_0}\,acos\left(\frac{G}{G\,(1-a)-1}\right). \tag{A.140}$$

Applying the time duration for stage 1 into (A.115) it is possible to find the inductor current by the end of that stage which is required as one of the initial conditions for stage 2:

$$i_{Lm}(t_1) = C_s\,\omega_0\,[V_{in} + V_o\,(a-1)]\,\sin(\Delta t_1\, a\,\omega_0). \tag{A.141}$$

The result is given by (A.142):

$$I_{Lm\,t1} = C_s\,\omega_0\,[V_{in} + V_o\,(a-1)]\sqrt{1-\left(\frac{G}{G\,(1-a)-1}\right)^2}. \tag{A.142}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $(G\,(1-a)-1)^2 - G^2 > 0$, which results in a design requirement given in (A.143):

$$G < \frac{1}{2-a}. \tag{A.143}$$

A.3.3.2 Stage 2

The second stage is characterized by the discharge of the remnant energy on the inductors. From (A.120) and (A.142) it is known that

$$i_{Lm}(t_2) = C_s\,\omega_0\,[V_{in} + V_o\,(a-1)]\sqrt{1-\left(\frac{G}{G\,(1-a)-1}\right)^2} - a\,\frac{V_o}{Lm}\,\Delta t_2 = 0. \tag{A.144}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{a\,\omega_0}\,\left(\frac{1}{G} + (a-1)\right)\sqrt{1-\left(\frac{G}{G\,(1-a)-1}\right)^2}. \tag{A.145}$$

A.3.3.3 Stage 4

Unlike non-isolated topologies, the flyback present asymmetrical current behavior between the time-periods of a given switching cycle. In order to ensure DCM operation, both restrictions for each half-period must be met, and therefore stages four and five must be analyzed accordingly. stage 4 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using the (A.128) it is known that

$$v_{Cs}(t_4) = V_o + V_{in}\,\cos(\Delta t_4\,\omega_0) = V_o\,(1-a). \tag{A.146}$$

Isolating Δt_4 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$:

$$\Delta t_4 = t_4 - t_3 = \frac{1}{\omega_0}\,acos\,(-\,a\,G)\,. \tag{A.147}$$

Applying the time duration for stage 4 into (A.130) it is possible to find the inductor current by the end of that stage which is required as one of the initial conditions for stage 5:

$$i_{Lm}(t_4) = C_s\,\omega_0\,V_{in}\,\sin(\Delta t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin\left(\frac{1}{\omega_0}\,acos(-a\,G)\,\omega_0\right). \tag{A.148}$$

The result is given by (A.149):

$$I_{Lm\,t4} = C_s\,V_{in}\,\omega_0\,\sqrt{1-(a\,G)^2}. \tag{A.149}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1-(a\,G)^2 > 0$, which results in a design requirement given in (A.150):

$$a\,G < 1. \tag{A.150}$$

A.3.3.4 Stage 5

The fifth stage is characterized by the discharge of the remnant energy on the inductors. From (A.135) and (A.149) it is known that

$$i_{Lm}(t_5) = I_{Lm(t4)} - a\,\frac{V_o}{L_{mp}}\,\Delta t_5 = C_s\,V_{in}\,\omega_0\,\sqrt{1-(a\,G)^2} - a\,\frac{V_o}{L_{mp}}\,\Delta t_5 = 0. \tag{A.151}$$

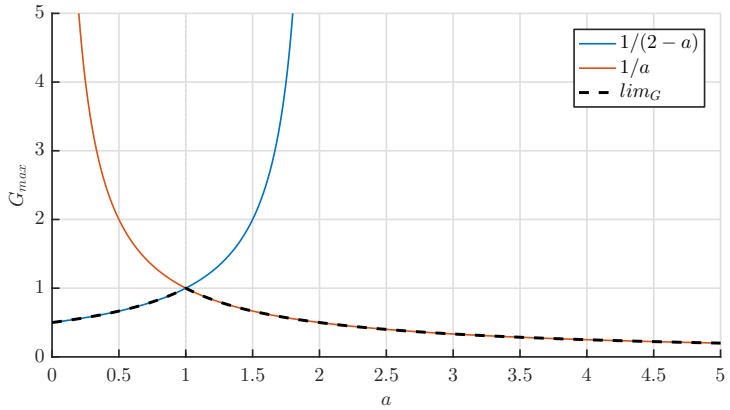
Isolating the time duration of the stage two, it can be found by

$$\Delta t_5 = t_5 - t_4 = \frac{1}{a\,\omega_0\,G}\,\sqrt{1-(a\,G)^2}. \tag{A.152}$$

A.3.3.5 Static gain relation with turns ratio

The requirement for the static gain in isolated converters differs from its non-isolated equivalent by the addition of the variable turns ratio 'a'. In order for the correct operation of the converter, both requirements given by stages 1 and 4 resulted by (A.143) and (A.150) respectively must be met. Figure 124 displays both requirements so the static gain limitation can be visualized by each value of turns-ratio 'a'. As it is shown, just as the non-isolated buck-boost topologies, the isolated version is also limited into step-down applications once the static gain G cannot be above 1.

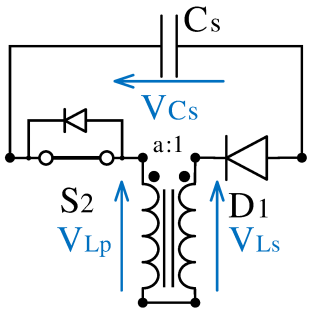
Figure 124 – Static gain limitations regarding turns-ratio 'a' for the flyback RSC converter



Source: Author (2020).

Furthermore, the turns ratio also presents limitation regarding the operation of the resonant circuit due to the intrinsic anti-parallel diode on the S_2 switch. The expected operation of the circuit should allow only direct current, yet conditions of reverse current can be analyzed over the L_p-S_2-C_s-L_s loop, explicit in Figure 125.

Figure 125 – Limiting loop for turns ratio a.



Source: Author (2020).

In order to assure reverse biasing of the intrinsic diode, $V_{Ls} + v_{Cs}(t) > V_{Lp}$ even for worst-case scenario, that is, for the smaller value of v_{Cs}. As previous described, stage 5 must allow mutual conduction on diodes D_1 and D_2 while maintaining the switched capacitor to its minimum voltage, so assuring reverse bias of the intrinsic diode during this period is essential to the correct operation of the system. In order to assure this reverse bias, the relation $V_{Ls} + V_o\,(1-a) > a\,V_{Ls}$ must be met. Therefore, the turns ratio is limited by

$$(V_{Ls} + V_o)\,(1-a) > 0 \rightarrow a < 1. \tag{A.153}$$

A.3.3.6 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}. \tag{A.154}$$

Which expands to

$$\frac{1}{a\,\omega_0}\,acos\left(\frac{G}{G\,(1-a)-1}\right) + \frac{1}{a\,\omega_0}\left(\frac{1}{G} + (a-1)\right)\sqrt{1-\left(\frac{G}{G\,(1-a)-1}\right)^2} < \frac{1}{2\,f_s}. \tag{A.155}$$

Solving for the resonant frequency gives

$$\omega_0 > \frac{2\,f_s}{a}\left(acos\left(\frac{G}{G\,(1-a)-1}\right) + \left(\frac{1}{G} + (a-1)\right)\sqrt{1-\left(\frac{G}{G\,(1-a)-1}\right)^2}\right). \tag{A.156}$$

The same requirement must be made for the second half of the switching period, mathematically described as

$$\Delta t_4 + \Delta t_5 < \frac{T_s}{2}. \tag{A.157}$$

Which expands to

$$\frac{1}{\omega_0}\,acos\,(-a\,G) + \frac{1}{a\,\omega_0\,G}\,\sqrt{1-(a\,G)^2} < \frac{1}{2\,f_s}. \tag{A.158}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\,f_s\,\left(acos\,(-a\,G) + \frac{1}{a\,G}\,\sqrt{1-(a\,G)^2}\right). \tag{A.159}$$

A.3.4 Average Magnetizing Current

The average current at the magnetizing inductor of the transformer is found by integrating the current waveform over a switching cycle:

$$\begin{aligned} I_{Lm} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{Lm}(t)_1 dt + \int_{t_1}^{t_2} i_{Lm}(t)_2 dt + \int_{t_2}^{t_3} i_{Lm}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} i_{Lm}(t)_4 dt + \int_{t_4}^{t_5} i_{Lm}(t)_5 dt + \int_{t_5}^{t_6} i_{Lm}(t)_6 dt\Bigg) \end{aligned} \tag{A.160}$$

$$\begin{aligned} I_{Lm} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} C_s\,\omega_0\,[V_{in} + V_o\,(a-1)]\,\sin(t\,a\,\omega_0) dt + \int_{t_1}^{t_2} I_{Lm(t1)} - a\,\frac{V_o}{L_{mp}}\,t + \int_{t_2}^{t_3} 0 dt + \\ &+ \int_{t_3}^{t_4} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0) dt + \int_{t_4}^{t_5} I_{Lm(t4)} - a\,\frac{V_o}{L_{mp}}\,t dt + \int_{t_5}^{t_6} 0 dt\Bigg). \end{aligned} \tag{A.161}$$

Solving the equation above and making use of the relations given by (A.140), (A.142), (A.145), (A.147), (A.149) and (A.152) the average output current can be simplified as (A.162):

$$I_{Lm} = C_s\,f_s\,V_{in}\,\frac{(a\,G+1)^2}{a\,G}. \tag{A.162}$$

A.3.5 Average Output Current

For the flyback converter, the output current is the same as the current at diode D_2. Following the operational stages, it can be seen that the output current is null for stages 1, 3 and 6, where for stages 2 and 5 the output current is the same as the current at the secondary of the transformer. At stage 4 the output current is the same as the current at the primary coil. Integrating such waveform over a period of time equal to the switching period yields the average output current

$$I_o = \frac{1}{T_s}\,\left(\int_{t_0}^{t_1} 0 dt + \int_{t_1}^{t_2} i_{Ls}(t)_2 dt \int_{t_2}^{t_3} 0 dt \int_{t_3}^{t_4} i_{Lp}(t)_4 dt \int_{t_4}^{t_5} i_{Ls}(t)_5 dt \int_{t_5}^{t_6} 0 dt\right). \tag{A.163}$$

The currents at the primary and secondary coils of the transformers are described according to the magnetizing current, which yields

$$\begin{aligned} I_o = f_s\Bigg[a\,\left(\int_{t_1}^{t_2} I_{Lm(t1)} - a\,\frac{V_o}{L_{mp}}\,t\,dt\right) + \int_{t_3}^{t_4} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt \\ + a\,\left(\int_{t_4}^{t_5} I_{Lm(t4)} - a\,\frac{V_o}{L_{mp}}\,t\,dt\right)\Bigg]. \end{aligned} \tag{A.164}$$

Solving the equation above and making use of the relations given by (A.140), (A.142), (A.145), (A.147), (A.149) and (A.152), the average output current can be simplified as (A.165):

$$I_o = C_s\, f_s\, V_{in}\, \frac{a\, G + 1}{G}. \tag{A.165}$$

A.3.6 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\, V_o = C_s\, f_s\, V_{in}\, \frac{a\, G + 1}{G}\, V_o. \tag{A.166}$$

Using the static gain definition stated as $V_o = G\, V_{in}$ the output power is given by

$$P_o = C_s\, f_s\, V_{in}^2\, (a\, G + 1). \tag{A.167}$$

The capacitor must be sized accordingly to the output power, using the relation given by (A.168):

$$C_s = \frac{P_o}{f_s\, V_{in}^2\, (a\, G + 1)}. \tag{A.168}$$

A.3.7 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 35.

Table 35 – RSC flyback simulation values for (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

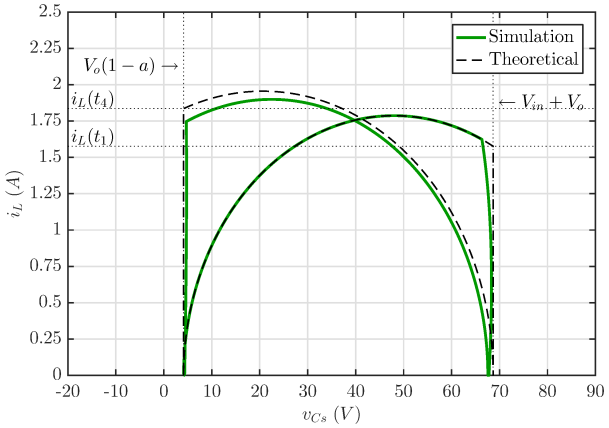
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$7.8\,nF$
Inductance	L	$4.7\,\mu H$
Transformer Turns-Ratio	a	0.8

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 126 yields a precise comparison between theoretical prediction and simulation result, highlighting specially the slightly lower current during the discharging stage 4.

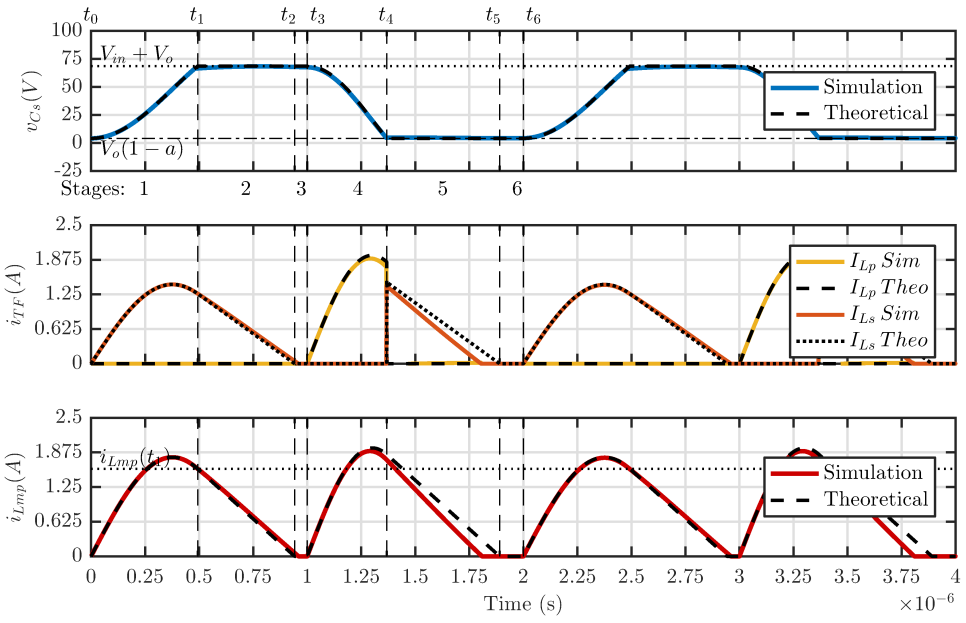
Figure 126 – State Plan for the RSC flyback converter.



Source: Author (2020).

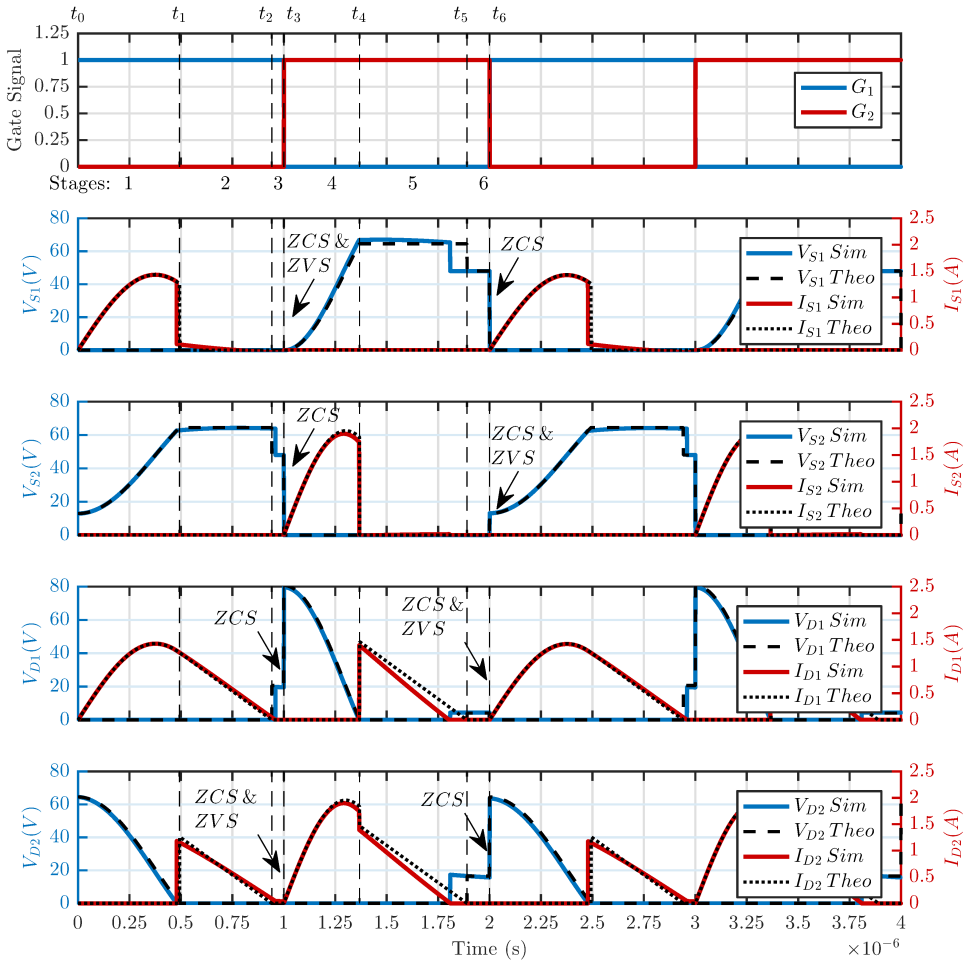
Thus, the waveform comparison of the RSC flyback converter states for each stage in their respective timespans is shown in Figure 127. In the time domain, only a small difference can be perceived in stage 5, where the demagnetizing of the inductor happens somewhat faster then theoretically predicted. Finally, Figure 128 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 127 – Theoretical waveforms of the state variables for the RSC flyback converter.



Source: Author (2020).

Figure 128 – Soft-switching on the semiconductors for the RSC flyback converter.

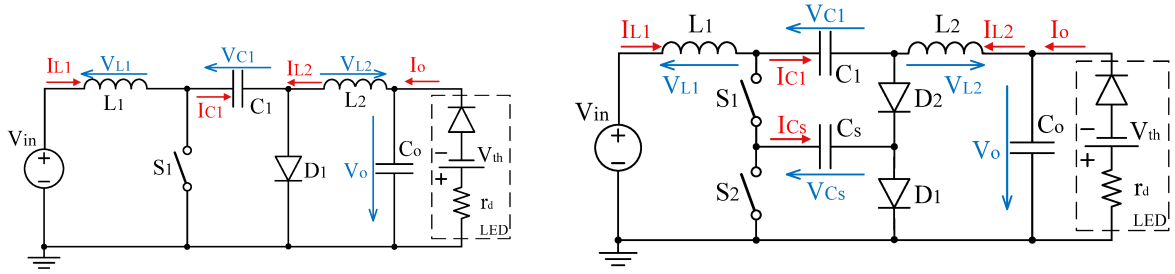


Source: Author (2020).

A.4 RSC ĆUK ANALYSIS

The classic Ćuk converter is shown on Figure 129 alongside the RSC Ćuk converter.

Figure 129 – Classic Ćuk converter (a) and RSC Ćuk converter (b).

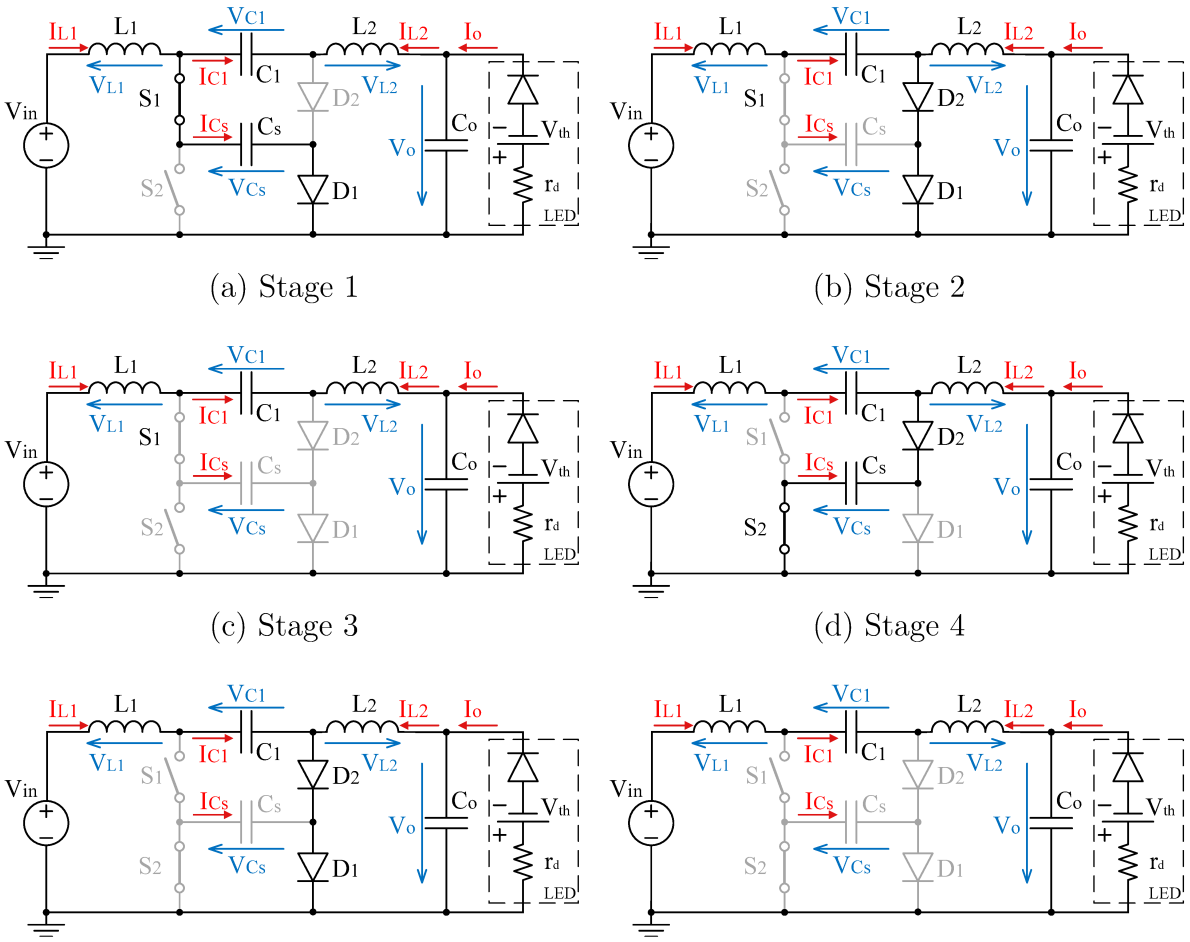


(a) (b)

Source: Author (2020).

The operation of the converter is divided in six distinct stages, highlighted in Figure 130.

Figure 130 – Stages of operation of the RSC Ćuk converter.



(a) Stage 1

(b) Stage 2

(c) Stage 3

(d) Stage 4

(e) Stage 5

(f) Stage 6

Source: Author (2020).

A.4.1 Input capacitor analysis

For the higher-order converters, a simplification can be made by assuming a high capacitance value for the input capacitor C_1, which keeps its voltage constant. Consequently, the additional state can be ignored on the high-frequency analysis decreasing by a considerable amount the complexity of the converter model.

The constant value of the capacitor voltage V_{C1} can be determined by the low-frequency analysis of the circuit. For the Ćuk converter, the analysis of the loop containing $[V_{in} - L_1 - C_1 - L_2 - V_o]$ yields, considering the inductors as short-circuits, the voltage value given by

$$V_{C1} = V_{in} + V_o \tag{A.169}$$

A.4.2 Switched capacitor analysis

The next step on the analysis of the converter is to determine the maximum and minimum voltages at the switched capacitor C_s.

The charge of the switched capacitor occurs during stage 1, highlighted in Figure 131a, where the active switch S_1 and diode D_1 conducting. The end of this stage is characterized by the complete charging of the capacitor, that is, when its voltage reaches the required value in order allow D_2 diode to be forward biased. For the Ćuk RSC converter the analysis of the loop containing $[C_1 - S_1 - C_s - D_2]$ yields that the D_2 diode voltage is given by

$$v_{D2}(t) = V_{C1} - v_{Cs}(t). \tag{A.170}$$

This implies that when the capacitor voltage reaches $v_{Cs}(t) = V_{C1}$, diode D2 is forward biased and allows current conduction. Therefore, the maximum voltage for the charged capacitor is given by $V_{Cs\,max} = V_{in} + V_o$.

Similarly, the analysis of the discharged capacitor is given by stage 4, shown in Figure 131a. The appropriate loop is comprised solely of $[C_s - S_2 - D_1]$. Once $v_{Cs}(t)$ is positive, diode D_1 is reverse biased. The voltage at this D_1 diode is given by

$$v_{D1}(t) = v_{Cs}(t). \tag{A.171}$$

Therefore, this condition ceases once the capacitor voltage reaches zero, allowing the diode D_1 to enter in conduction mode, which therefore forces the capacitor voltage to keep null value. In summation, the minimum and maximum voltages for the switched capacitor C_s are given by

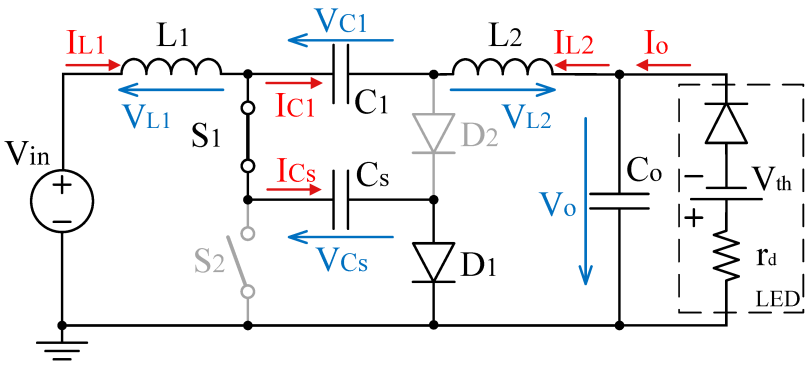
$$V_{Cs\,max} = V_{in} + V_o \; ; \; V_{Cs\,min} = 0. \tag{A.172}$$

A.4.3 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor through the highlighted path shown in Figure 131. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = 0 \\ i_{L_1}(t_0) = I_{L\,DCM} \\ i_{L_2}(t_0) = -I_{L\,DCM} \end{cases} \tag{A.173}$$

Figure 131 – Ćuk RSC: stage 1.



Source: Author (2020).

The conditions of current and voltage for each semiconductor can be found through loop and node equations, and are summarized in Table 36.

Table 36 – Semiconductor Conditions for RSC Ćuk: stage 1.

	State	Voltages	Currents
$\mathbf{S_1}$	Conducting	$v_{S1} = 0$	$i_{S1} = i_{L1}(t) + i_{L2}(t)$
$\mathbf{S_2}$	Blocking	$v_{S2} = v_{Cs}(t)$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
$\mathbf{D_2}$	Blocking	$v_{D2} = V_{C1} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described in time and frequency domain as (A.174), (A.175) and (A.176).

Time Domain		Frequency Domain
$V_{in} = L_1 \frac{d}{dt} i_{L1}(t) + v_{Cs}(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + V_{Cs}(s)$ (A.174)
$v_{Cs}(t) = V_{C1} - L_2 \frac{d}{dt} i_{L2}(t) - V_o$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = \frac{V_{C1}}{s} - L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) - \frac{V_o}{s}$ (A.175)
$C_s \frac{d}{dt} v_{Cs}(t) = i_{L1}(t) + i_{L2}(t)$	$\xrightarrow{\mathcal{L}}$	$s\, C_s\, V_{Cs}(s) = I_{L1}(s) + I_{L2}(s)$ (A.176)

Once multiple state variables are included in the set of equations, a certain effort must be made in order to isolate each of them. The results are summarized as follows.

Isolating Switched Capacitor Voltage:		
From (A.174)	$V_{Cs}(s) = -L_1\,(s\,I_{L1}(s) - I_{L1(t0)}) + \dfrac{V_{in}}{s}$	(A.177)
From (A.175)	$V_{Cs}(s) = \dfrac{V_{in} + V_o}{s} - L_2\,(s\,I_{L2}(s) - I_{L2(t0)})$	(A.178)
From (A.176)	$V_{Cs}(s) = \dfrac{I_{L1}(s)}{C_s\,s} + \dfrac{I_{L2}(s)}{C_s\,s} + \dfrac{V_{Cs(t0)}}{s}$	(A.179)
Isolating Inductor Currents:		
From (A.174)	$I_{L1}(s) = \dfrac{-V_{Cs}(s)}{L_1\,s} + \dfrac{I_{L1(t0)}}{s} + \dfrac{V_{in}}{L_1\,s^2}$	(A.180)
From (A.175)	$I_{L2}(s) = \dfrac{-V_{Cs}(s)}{L_2\,s} + \dfrac{I_{L2(t0)}}{s} + \dfrac{V_{in} + V_o}{L_2\,s^2}$	(A.181)
From (A.176)	$\begin{cases} I_{L1}(s) = C_s\,s\,V_{Cs}(s) - I_{L2}(s) - C_s\,V_{Cs(t0)} \\ I_{L2}(s) = C_s\,s\,V_{Cs}(s) - I_{L1}(s) - C_s\,V_{Cs(t0)} \end{cases}$	(A.182)

Using the relation for $V_{Cs}(s)$ given by (A.179) and substituting the inductor currents given by (A.180) and (A.181) yields

$$V_{Cs}(s) = \frac{V_{in}}{s}\,\frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.183}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in}\,(1 - \cos(t\,\omega_0)). \tag{A.184}$$

On the other hand, using the relation for the current at inductor L_1 given by (A.182) and substituting $I_{L2}(s)$ from (A.181) and $V_{Cs}(s)$ from (A.177) in that order, yields the inductor current of

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} + \frac{V_{in}}{L_1}\,\frac{1}{s^2 + \omega_0^2}. \tag{A.185}$$

The inverse Laplace transform gives the inductor current in time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0). \tag{A.186}$$

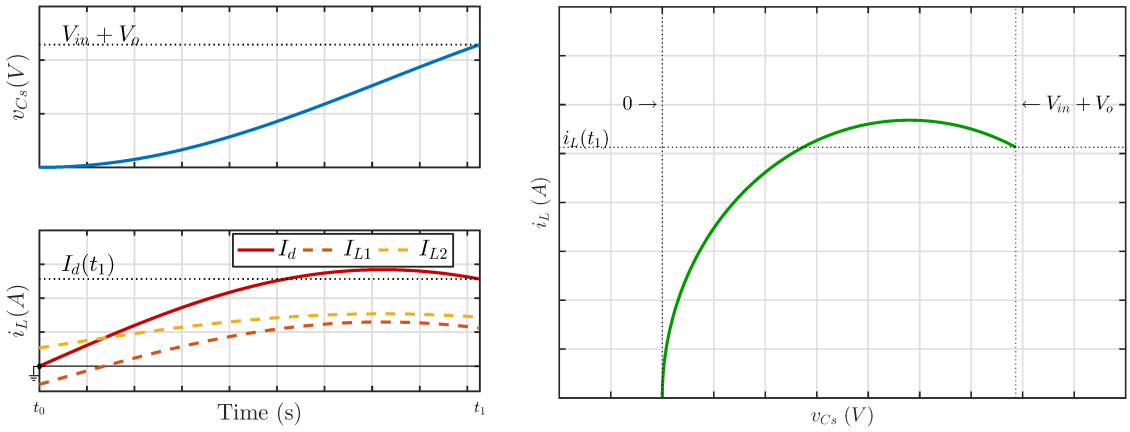
Similarly, an equivalent procedure yields the current at the inductor L_2 as

$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.187}$$

Adding the inductor currents gives the overall diode current I_d as

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.188}$$

Figure 132 – Ćuk RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

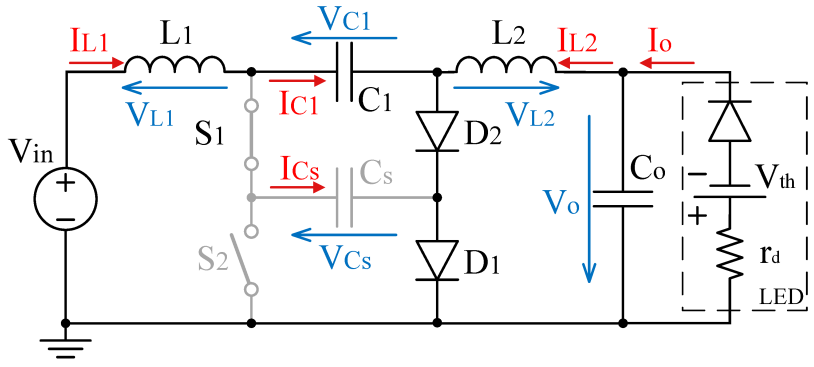
Source: Author (2020).

The resulted waveforms described are shown in Figure 132.

When the capacitor reaches sufficient voltage to forward bias the diode D_2, the magnetizing energy on the inductors forces a current through the passive semiconductors accordingly to Figure 133. Once the diode D_2 starts and keeps conducting current, the voltage at the switched capacitor C_s is forced to remain unchanged, keeping its maximum value. The energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_{in} + V_o \\ i_{L_1}(t_1) = I_{L1\,(t1)} \\ i_{L_2}(t_1) = I_{L2\,(t1)} \end{cases} \tag{A.189}$$

Figure 133 – Ćuk RSC: stage 2.



Source: Author (2020).

Semiconductor conditions for this stage are displayed in Table 37.

Table 37 – Semiconductor Conditions for RSC Ćuk: stage 2.

	State	Voltages	Currents
$\mathbf{S_1}$	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
$\mathbf{S_2}$	Blocking	$v_{S2} = V_{C1} - v_{Cs}(t)$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
$\mathbf{D_2}$	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described through (A.190) and (A.191).

Time Domain		Frequency Domain	
$V_{in} = L_1 \frac{d}{dt} i_{L1}(t) + V_{C1}$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \frac{V_{C1}}{s}$	(A.190)
$L_2 \frac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = \frac{V_o}{s}$	(A.191)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max} = V_{in} + V_o. \tag{A.192}$$

The inductor behavior can be solved separately once the states don't depend on each other. Using (A.190) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.193}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t1)} - \frac{V_o}{L_1}\, t. \tag{A.194}$$

Similarly, solving (A.191) for $I_{L2}(s)$ yields

$$i_{L2}(t) = I_{L2(t1)} - \frac{V_o}{L_2}\, t. \tag{A.195}$$

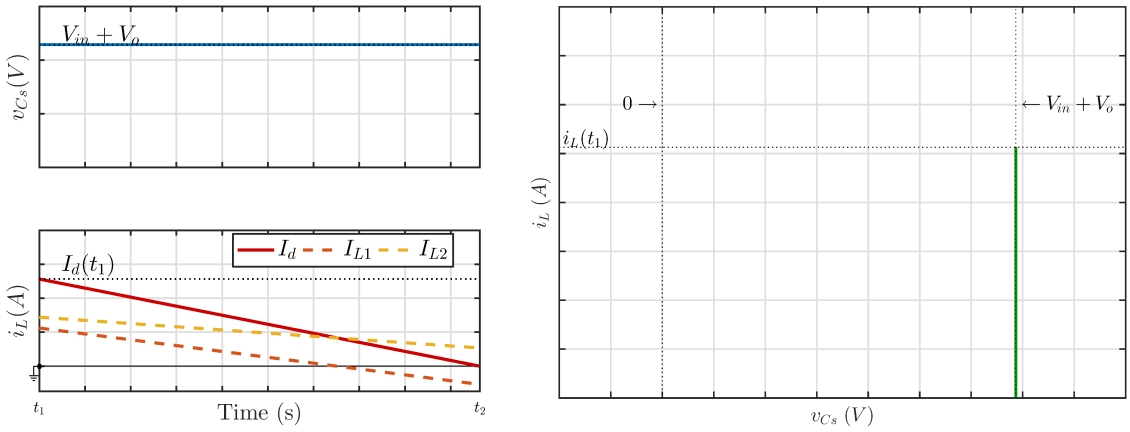
Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t1)} - \frac{V_o}{L_e}\, t. \tag{A.196}$$

The resulted waveforms described are shown in Figure 134.

As oppose to lower-order converter, in higher-order converters DCM operation does not imply a complete depletion of current from the inductors since an equilibrium

Figure 134 – Ćuk RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



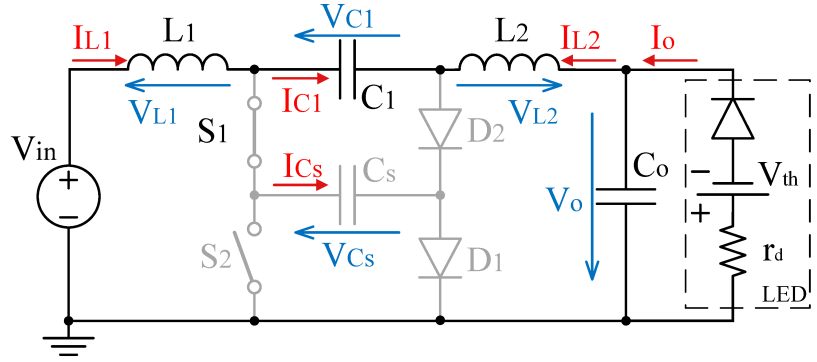
(a) (b)

Source: Author (2020).

point where both currents cancel each other is possible. Thus, the equivalent stage of null voltage occurs with the inductor currents keeping a constant value at a given DCM offset with opposing direction, circulating current through the path shown in Figure 135. The initial conditions for this stage are described by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_{in} + V_o \\ i_{L_1}(t_2) = I_{L\,DCM} \\ i_{L_2}(t_2) = -I_{L\,DCM}. \end{cases} \tag{A.197}$$

Figure 135 – Ćuk RSC: stage 3.



Source: Author (2020).

Through loop and node equations the descriptions of the semiconductor behavior can be found, being summarized in Table 38.

Table 38 – Semiconductor Conditions for RSC Ćuk: stage 3.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t) - V_{in}$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_{C1} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,max} \tag{A.198}$$

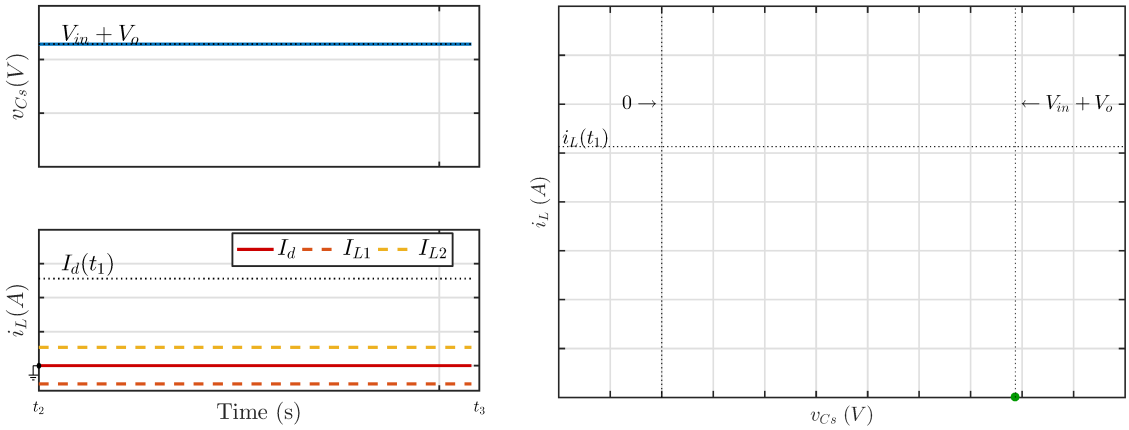
$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.199}$$

The equivalent current $i_d(t)$ is then given by

$$i_d(t) = 0. \tag{A.200}$$

The resulted waveforms described are shown in Figure 136.

Figure 136 – Ćuk RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



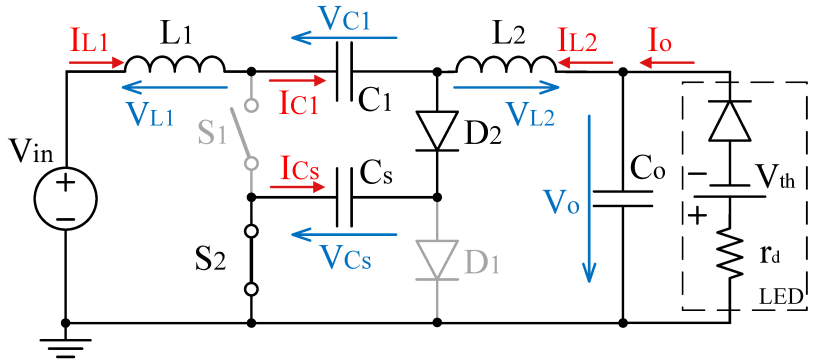
(a) (b)

Source: Author (2020).

The second half of the switching period is initiated when the active switch S_2 begins conducting as opposed to S_1, resulting in the circuit shown in Figure 137. The switched capacitor C_s is once again added to the active part of the circuit allowing its stored energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_{in} + V_o \\ i_{L_1}(t_3) = I_{L\,DCM} \\ i_{L_2}(t_3) = -I_{L\,DCM} \end{cases} \tag{A.201}$$

Figure 137 – Ćuk RSC: stage 4.



Source: Author (2020).

Semiconductor behavior for this stage is highlighted in Table 39.

Table 39 – Semiconductor Conditions for RSC Ćuk: stage 4.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{C1} - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = i_{L1}(t) + i_{L2}(t)$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The node and loop equations for this stage are described by (A.202), (A.203) and (A.204).

Time Domain		Frequency Domain
$V_{in} = L_1 \frac{d}{dt} i_{L1}(t) + V_{C1} - v_{Cs}(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \frac{V_{C1}}{s} - V_{Cs}(s)$ (A.202)
$v_{Cs}(t) = V_o - L_2 \frac{d}{dt} i_{L2}(t)$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = \frac{V_o}{s} - L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right)$ (A.203)
$C_s \frac{d}{dt} v_{Cs}(t) = -(i_{L1}(t) + i_{L2}(t))$	$\xrightarrow{\mathcal{L}}$	$s\, C_s\, V_{Cs}(s) = -(I_{L1}(s) + I_{L2}(s))$ (A.204)

Isolating each of the states for every equation yields the relations describes as follows.

Isolating Switched Capacitor Voltage:		
From (A.202)	$V_{Cs}(s) = L_1\,(s\,I_{L1}(s) - I_{L1(t3)}) + \frac{V_o}{s}$	(A.205)
From (A.203)	$V_{Cs}(s) = L_2\,(s\,I_{L2}(s) - I_{L2(t3)}) + \frac{V_o}{s}$	(A.206)
From (A.204)	$V_{Cs}(s) = -\frac{I_{L1}(s)}{C_s\,s} - \frac{I_{L2}(s)}{C_s\,s} + \frac{V_{Cs(t3)}}{s}$	(A.207)
Isolating Inductor Currents:		
From (A.202)	$I_{L1}(s) = \frac{V_{Cs}(s)}{L_1\,s} + \frac{I_{L1(t3)}}{s} - \frac{V_o}{L_1\,s^2}$	(A.208)
From (A.203)	$I_{L2}(s) = \frac{V_{Cs}(s)}{L_2\,s} + \frac{I_{L2(t3)}}{s} - \frac{V_o}{L_2\,s^2}$	(A.209)
From (A.204)	$\begin{cases} I_{L1}(s) = -C_s\,s\,V_{Cs}(s) - I_{L2}(s) + C_s\,V_{Cs(t3)} \\ I_{L2}(s) = -C_s\,s\,V_{Cs}(s) - I_{L1}(s) + C_s\,V_{Cs(t0)} \end{cases}$	(A.210)

Using the V_{Cs} relation given by (A.207) and substituting the I_{L1} and I_{L2} relations given from (A.208) and (A.209) respectively, the capacitor voltage can be given as

$$V_{Cs}(s) = \frac{V_o}{s}\,\frac{\omega_0^2}{s^2+\omega_0^2} + (V_{in}+V_o)\,\frac{s}{s^2+\omega_0^2}. \tag{A.211}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_o + V_{in}\,\cos(t\,\omega_0). \tag{A.212}$$

Similarly, using the $I_{L1}(s)$ relation given by (A.210) following by the use of (A.209) for $I_{L2}(s)$ and (A.205) for $V_{Cs}(s)$ in that order yields

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} + \frac{V_{in}}{L_1}\,\frac{1}{s^2+\omega_0^2}. \tag{A.213}$$

The inverse Laplace transforms gives the inductor current at the time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0). \tag{A.214}$$

Using equivalent manipulation, the current for the L_2 inductor can be found as

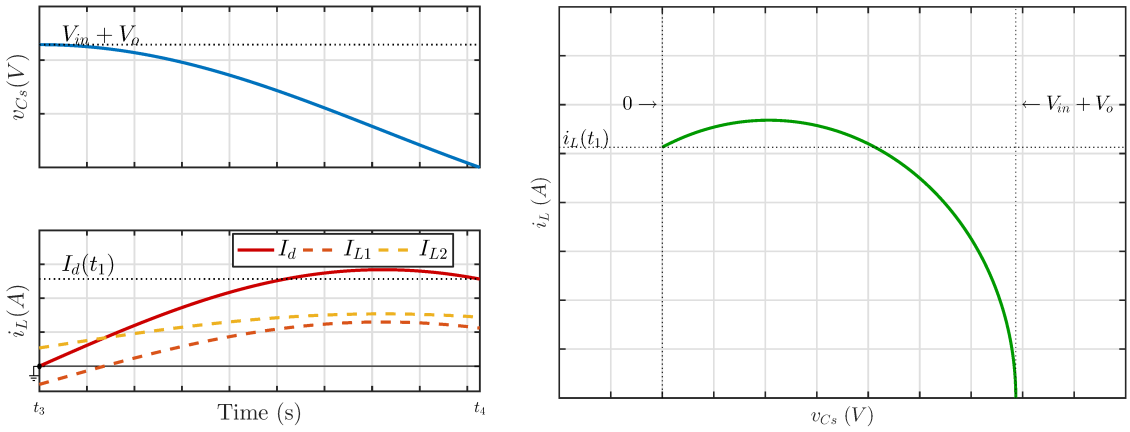
$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.215}$$

Finally, the equivalent diode current $I_d(t)$ is given by

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.216}$$

The resulted waveforms described are shown in Figure 138.

Figure 138 – Ćuk RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



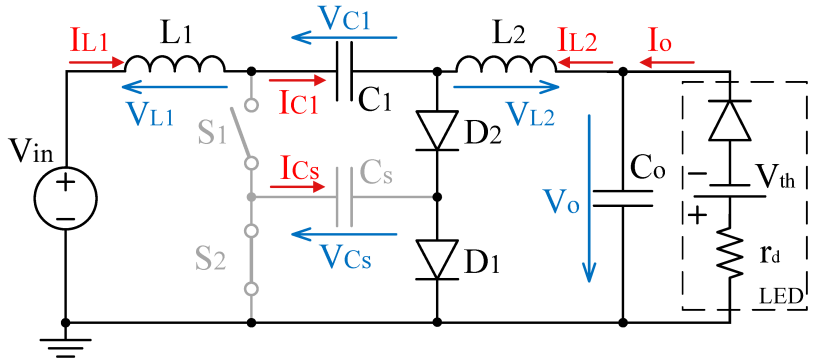
(a) (b)

Source: Author (2020).

With the complete discharge of the switched capacitor its voltage is maintained in zero, allowing the diode D_1 to be forward biased. Once again, remnant magnetizing energy on the inductor forces a current flow into both diodes as shown in Figure 139. The initial conditions to this stage are described by

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = 0 \\ i_{L_1}(t_4) = I_{L1\,(t4)} \\ i_{L_2}(t_4) = I_{L2\,(t4)} \end{cases} \tag{A.217}$$

Figure 139 – Ćuk RSC: stage 5.



Source: Author (2020).

The semiconductor behavior during this stage are shown in Table 40.

Table 40 – Semiconductor Conditions for RSC Ćuk: stage 5.

	State	Voltages	Currents
$\mathbf{S_1}$	Blocking	$v_{S1} = V_{C1} - v_{Cs}(t)$	$i_{S1} = 0$
$\mathbf{S_2}$	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
$\mathbf{D_2}$	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described by (A.218) and (A.219).

Time Domain		Frequency Domain	
$V_{in} = L_1 \frac{d}{dt} i_{L1}(t) + V_{C1}$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \frac{V_{C1}}{s}$	(A.218)
$L_2 \frac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = \frac{V_o}{s}$	(A.219)

During this stage the switched capacitor C_s remains discharged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,min}. \tag{A.220}$$

The inductor behavior can be solved separately once the states are independent from each other. Using (A.218) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.221}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t4)} - \frac{V_o}{L_1}\, t. \tag{A.222}$$

Similarly, solving (A.219) for $I_{L2}(s)$ yields

$$i_{L2}(t) = I_{L2(t4)} - \frac{V_o}{L_2}\, t. \tag{A.223}$$

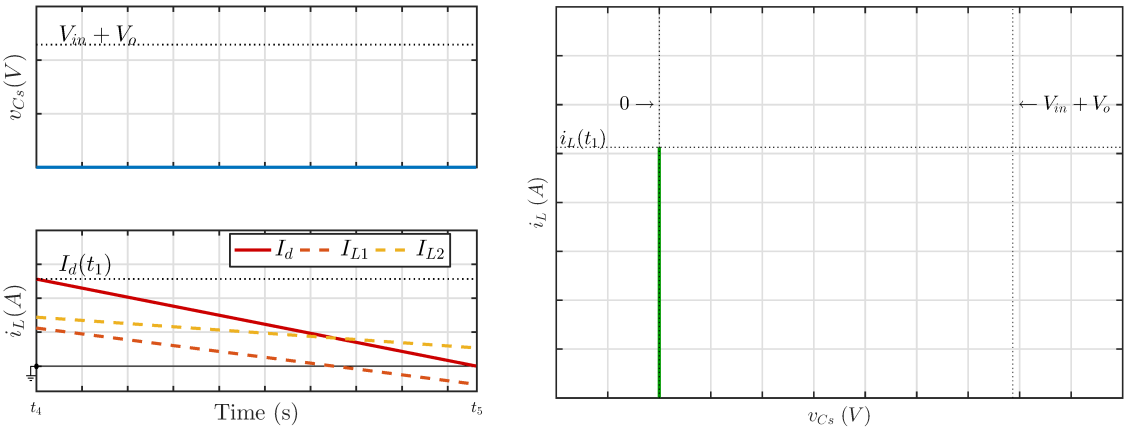
Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t4)} - \frac{V_o}{L_e}\, t. \tag{A.224}$$

The resulted waveforms described are shown in Figure 140.

Once again, this stage is characterized by a null equivalent diode current $i_d(t)$, caused by the inductor currents reaching a point of mutual cancellation, resulting in the

Figure 140 – Ćuk RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



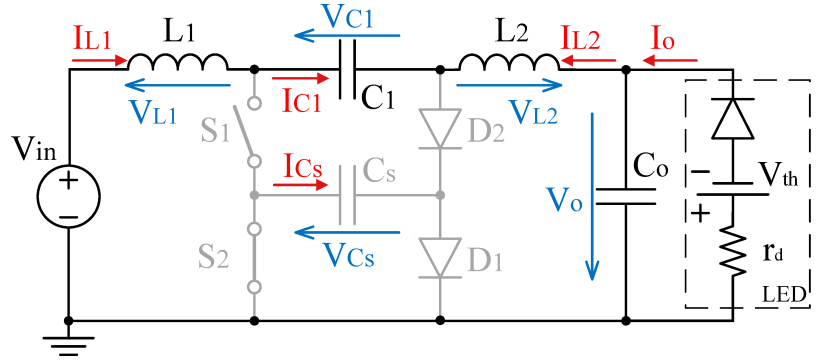
(a) (b)

Source: Author (2020).

path shown in Figure 141. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = 0 \\ i_{L_1}(t_5) = I_{L\,DCM} \\ i_{L_2}(t_5) = -I_{L\,DCM} \end{cases} \tag{A.225}$$

Figure 141 – Ćuk RSC: stage 6.



Source: Author (2020).

Table 41 summarizes the semiconductor conditions during this stage.

Table 41 – Semiconductor Conditions for RSC Ćuk: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,min} = 0 \tag{A.226}$$

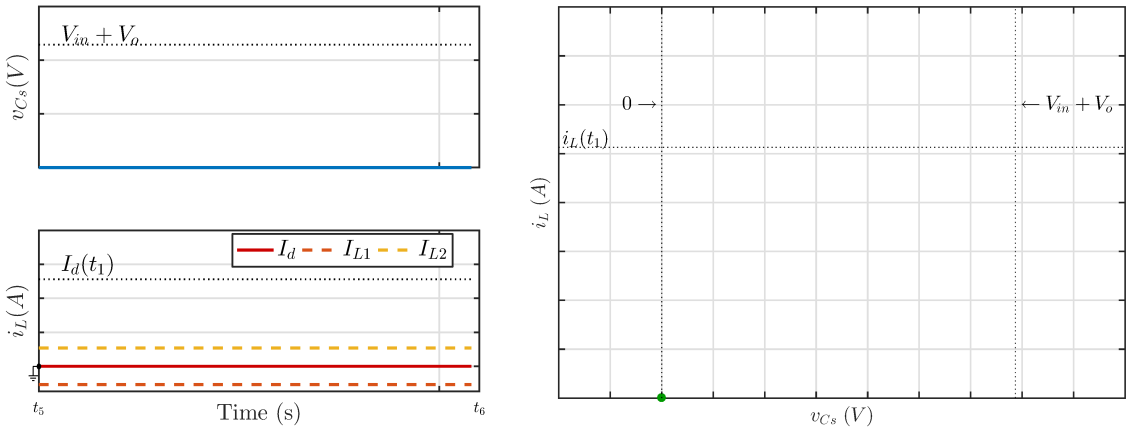
$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.227}$$

The equivalent current $i_d(t)$ is then given by

$$i_d(t) = 0. \tag{A.228}$$

The resulted waveforms described are shown in Figure 142.

Figure 142 – Ćuk RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.4.4 Time Analysis

In order to fully characterize the behavior of the converter, the time delay of each state must be determined.

A.4.4.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using (A.184) it is known that

$$v_{Cs}(t_1) = V_{in}\,(1 - \cos(\Delta t_1\,\omega_0)) = V_{in} + V_o. \tag{A.229}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$ yields

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{-V_o}{V_{in}}\right) = \frac{1}{\omega_0}\,acos\,(-G)\,. \tag{A.230}$$

Applying the time duration for stage 1 into (A.186) it is possible to find the current at the L_1 inductor by the end of that stage which is required as one of the initial conditions for stage 2 as

$$I_{L1\,t1} = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t_1\,\omega_0) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sqrt{1-G^2}. \tag{A.231}$$

Similarly, the current at $t = t_1$ for L_2 inductor is given by

$$I_{L2\,t1} = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t_1\,\omega_0) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sqrt{1-G^2}. \tag{A.232}$$

And by adding both equations, the equivalent current $i_d(t)$ at the same instant is given by the sum of both inductor currents, given by

$$I_{d(t1)} = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sqrt{1-G^2}. \tag{A.233}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1 - G^2 > 0$, which results in a design requirement given in (A.234):

$$G < 1. \tag{A.234}$$

A.4.4.2 Stages 2 and 5

The second stage is characterized by the mutual cancellation of the inductor currents until no current is left to keep the diodes forward biased. Henceforth, for the higher-order converters this stage is reached not when a given inductor current reaches zero, but when the sum of the inductor currents does. From (A.196) and (A.233) it is known that

$$i_d(t_2) = I_{d(t1)} - \frac{V_o}{L_e}\,\Delta t_2 = \frac{V_{in}}{L_e\,\omega_0}\,\sqrt{1-G^2} - \frac{V_o}{L_e}\,\Delta t_2 = 0. \tag{A.235}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,G}\,\sqrt{1-G^2}. \tag{A.236}$$

A.4.5 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}. \tag{A.237}$$

Which expands to

$$\frac{1}{\omega_0}\, acos\,(-G) + \frac{1}{\omega_0\, G}\,\sqrt{1-G^2} < \frac{1}{2\, f_s}. \tag{A.238}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\, f_s\, \left(acos\,(-G) + \frac{1}{G}\,\sqrt{1-G^2}\right). \tag{A.239}$$

A.4.6 Average Equivalent Diode Current

The average inductor current is found by integrating the equivalent diode waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period as follows

$$I_{Ld} = \frac{1}{T_s/2}\,\left(\int_{t_0}^{t_1}[i_{L1}(t)_1 + i_{L2}(t)_1]dt + \int_{t_1}^{t_2}[i_{L1}(t)_2 + i_{L2}(t)_2]dt\right) \tag{A.240}$$

$$I_{Ld} = 2\, f_s\,\left(\int_{t_0}^{t_1} C_s\,\omega_0\, V_{in}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{d(t1)} - \frac{V_o}{L_e}\,t\,dt\right). \tag{A.241}$$

Solving the equation above and making use of the relations given by (A.230) (A.231) and (A.236), the average output current can be simplified as (A.242):

$$I_d = C_s\, f_s\, V_{in}\,\frac{(G+1)^2}{G}. \tag{A.242}$$

A.4.7 DCM Current Offset

For the higher-order converters DCM operation does not imply on null current values for inductors during stage three. This characteristic is due to the capability of the inductors on storing energy such that the its opposite values of constant current can cancel each other and are therefore unable to keep the diodes forward biased.

In order to accurately characterize the current on the inductors, this constant current level of opposite values must be found, which requires an additional steady-state description of the system (ZHU; LUO; HE, 2008). This new description can be made for the charge balance of the input capacitor C_1 in high-frequency.

As stated, the capacitor C_1 is at first considered as a constant-voltage component which simplifies the calculations while still maintaining certain accuracy given a high

capacitance value. Still, the voltage at the capacitor is directly affected by the charge count in each instant which is consequently an integration of the current waveform. Once the currents at the capacitor C_1 are not constant, it can be assumed a high-frequency voltage change in the capacitor related to the charge differences between stages. Yet, for a given switching period, it is expected that the initial and final changes of charge can cancel themselves in order to maintain constant voltage. This statement can be mathematically described as

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{C1}(t)_1 dt + \int_{t_1}^{t_2} i_{C1}(t)_2 dt + \int_{t_2}^{t_3} i_{C1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} i_{C1}(t)_4 dt + \int_{t_4}^{t_5} i_{C1}(t)_5 dt + \int_{t_5}^{t_6} i_{C1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.243}$$

During stage 1, the input capacitor current is the opposite to the current at inductor L_2 according to the assigned positive current flow for each component. For every other stage, the input capacitor current is the same as the current at inductor L_1 which van be translated to

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} -i_{L2}(t)_1 dt + \int_{t_1}^{t_2} i_{L1}(t)_2 dt + \int_{t_2}^{t_3} i_{L1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} i_{L1}(t)_4 dt + \int_{t_4}^{t_5} i_{L1}(t)_5 dt + \int_{t_5}^{t_6} i_{L1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.244}$$

Replacing the inductor waveforms on the equation above yields

$$\begin{aligned}\int_{t_0}^{t_1} -\left(-I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0)\right) dt + &\int_{t_1}^{t_2} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_2}^{t_3} I_{L\,DCM} dt + \int_{t_3}^{t_4} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0) dt + \\ &+ \int_{t_4}^{t_5} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_5}^{t_6} I_{L\,DCM} dt = 0.\end{aligned} \tag{A.245}$$

Solving the equation for $I_{L\,DCM}$ and using the time steps defined in the previous section,

$$I_{L\,DCM} = C_s\,V_{in}\,f_s\,\frac{G+1}{G}\,\frac{G\,L_1 - L_2}{L_1 + L_2}. \tag{A.246}$$

Which can also be written as

$$I_{L\,DCM} = \frac{I_d}{G+1}\,\frac{G\,L_1 - L_2}{L_1 + L_2}. \tag{A.247}$$

A.4.8 Average Output Current

For the Ćuk converter, the output current is the same as the current at inductor L_2 according to the assigned direction of positive current flow. Once the inductor current

repeats itself after the first switching period, the integration can be made over only half a witching period as

$$I_o = \frac{1}{T_s/2}\left(\int_{t_0}^{t_1} i_{L2}(t)_1 dt + \int_{t_1}^{t_2} i_{L2}(t)_2 dt + \int_{t_2}^{t_3} i_{L2}(t)_3 dt\right) \tag{A.248}$$

$$I_o = 2\,f_s\left(\int_{t_0}^{t_1} -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{L2(t1)} - \frac{V_o}{L_2}\,t\,dt + \int_{t_2}^{t_3} -I_{L\,DCM}\,dt\right). \tag{A.249}$$

Solving the equation above and making use of the relations given by (A.230), (A.232) and (A.236), the average output current can be simplified as (A.250):

$$I_o = C_s\,V_{in}\,f_s\,\frac{G+1}{G}. \tag{A.250}$$

Which can also be written as

$$I_o = \frac{I_d}{G+1}. \tag{A.251}$$

A.4.9 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\,V_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}\,V_o. \tag{A.252}$$

Using the static gain definition stated as $V_o = G\,V_{in}$ the output power is given by

$$P_o = C_s\,f_s\,V_{in}^2\,(G+1). \tag{A.253}$$

The capacitor must be sized accordingly to the output power, relation given by (A.254):

$$C_s = \frac{P_o}{f_s\,V_{in}^2\,(G+1)}. \tag{A.254}$$

A.4.10 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 42.

Table 42 – RSC Ćuk simulation values fos (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

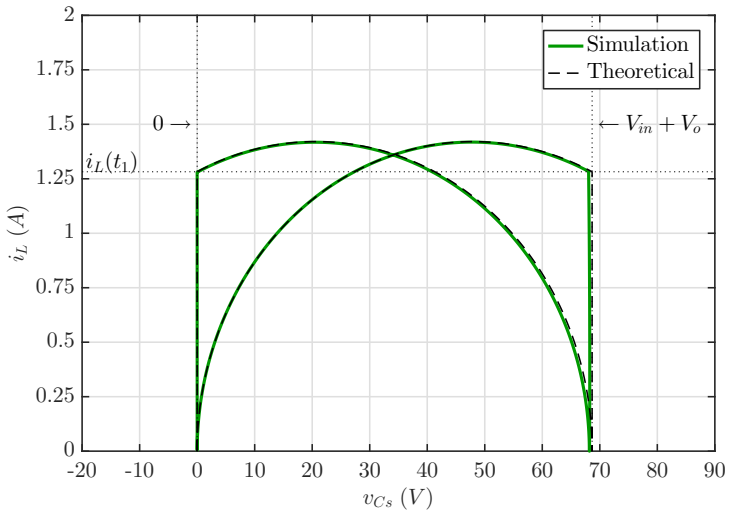
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Input Capacitance	C_1	$470\,nF$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$6.8\,nF$
Input Inductance	L_1	$12\,\mu H$
Output Inductance	L_2	$22\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 143 yields a precise comparison between theoretical prediction and simulation result, where the only apparent difference lies on a slightly lower value for maximum switched capacitor voltage.

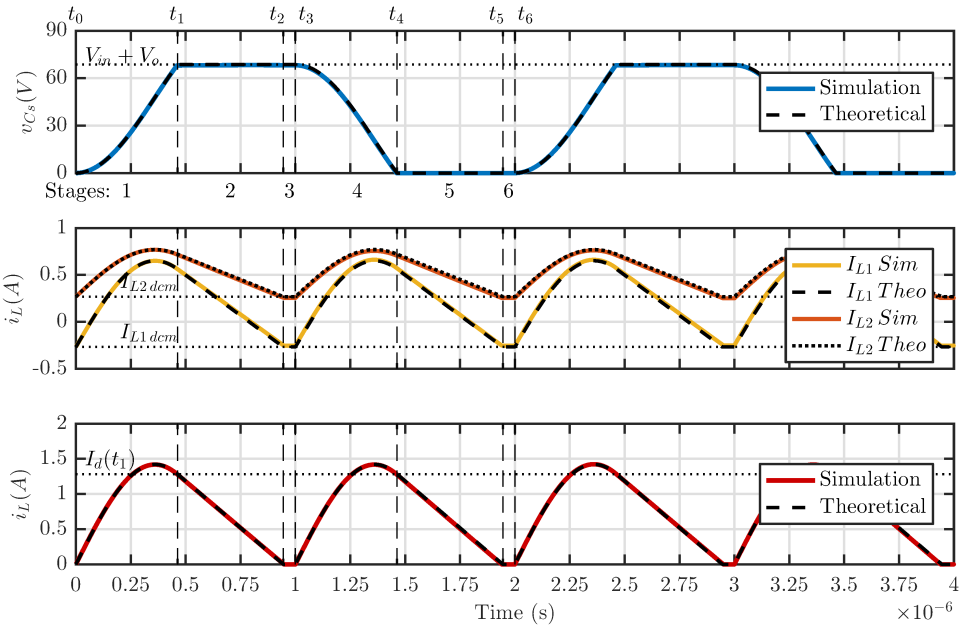
Figure 143 – State Plan for the RSC Ćuk converter.



Source: Author (2020).

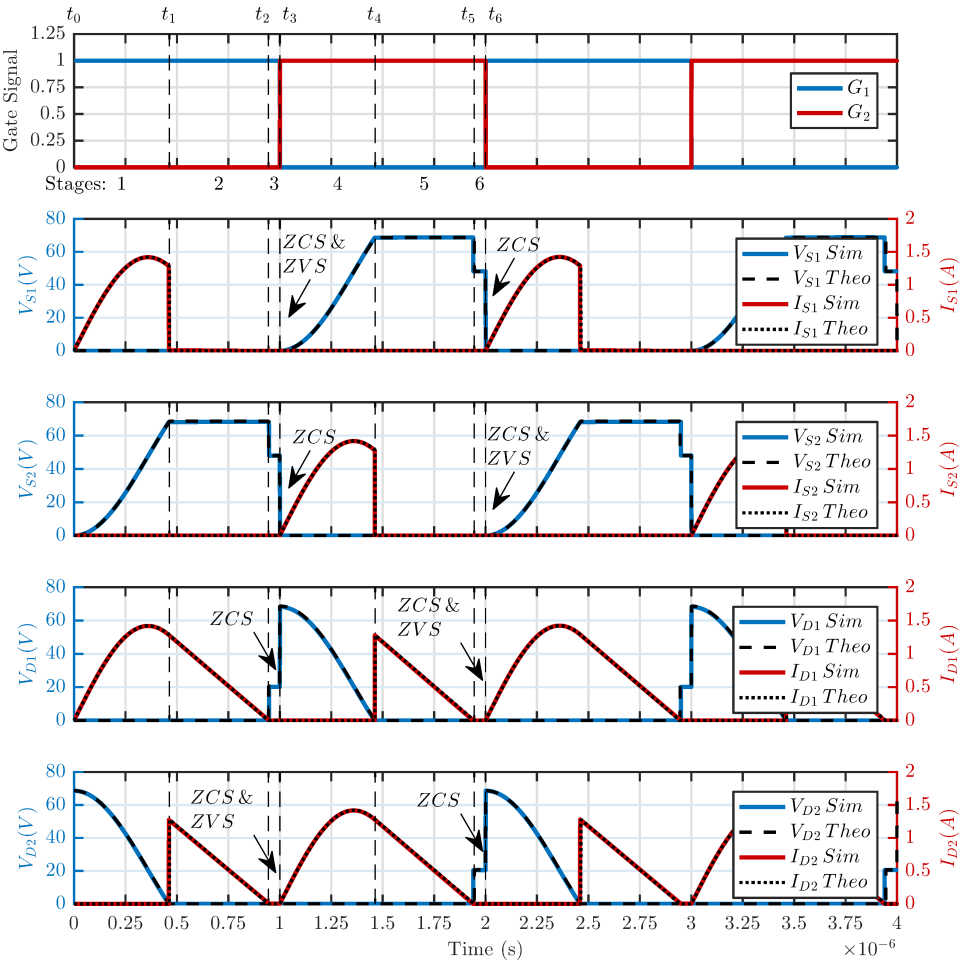
Thus, the waveform comparison of the RSC Cuk converter states for each stage in their respective timespans is shown in Figure 144, following prediction as expected. Finally, Figure 145 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 144 – Theoretical waveforms of the state variables for the RSC Ćuk converter.



Source: Author (2020).

Figure 145 – Soft-switching on the semiconductors for the RSC Ćuk converter.

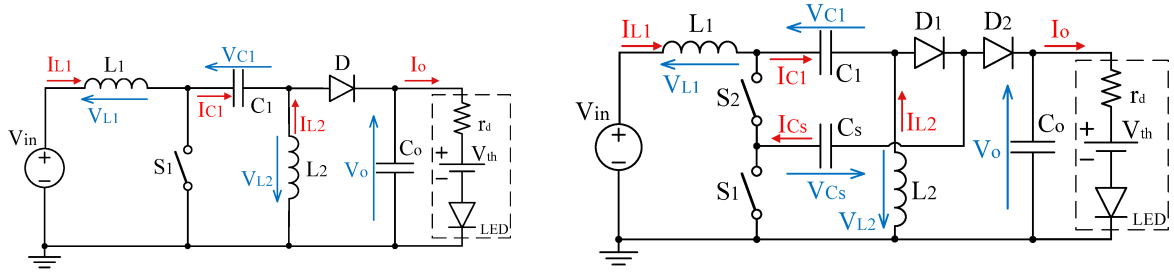


Source: Author (2020).

A.5 RSC SEPIC ANALYSIS

The RSC SEPIC converter is shown on Figure 146 in comparison to the SEPIC converter.

Figure 146 – Classic SEPIC converter (a) and RSC SEPIC converter (b).

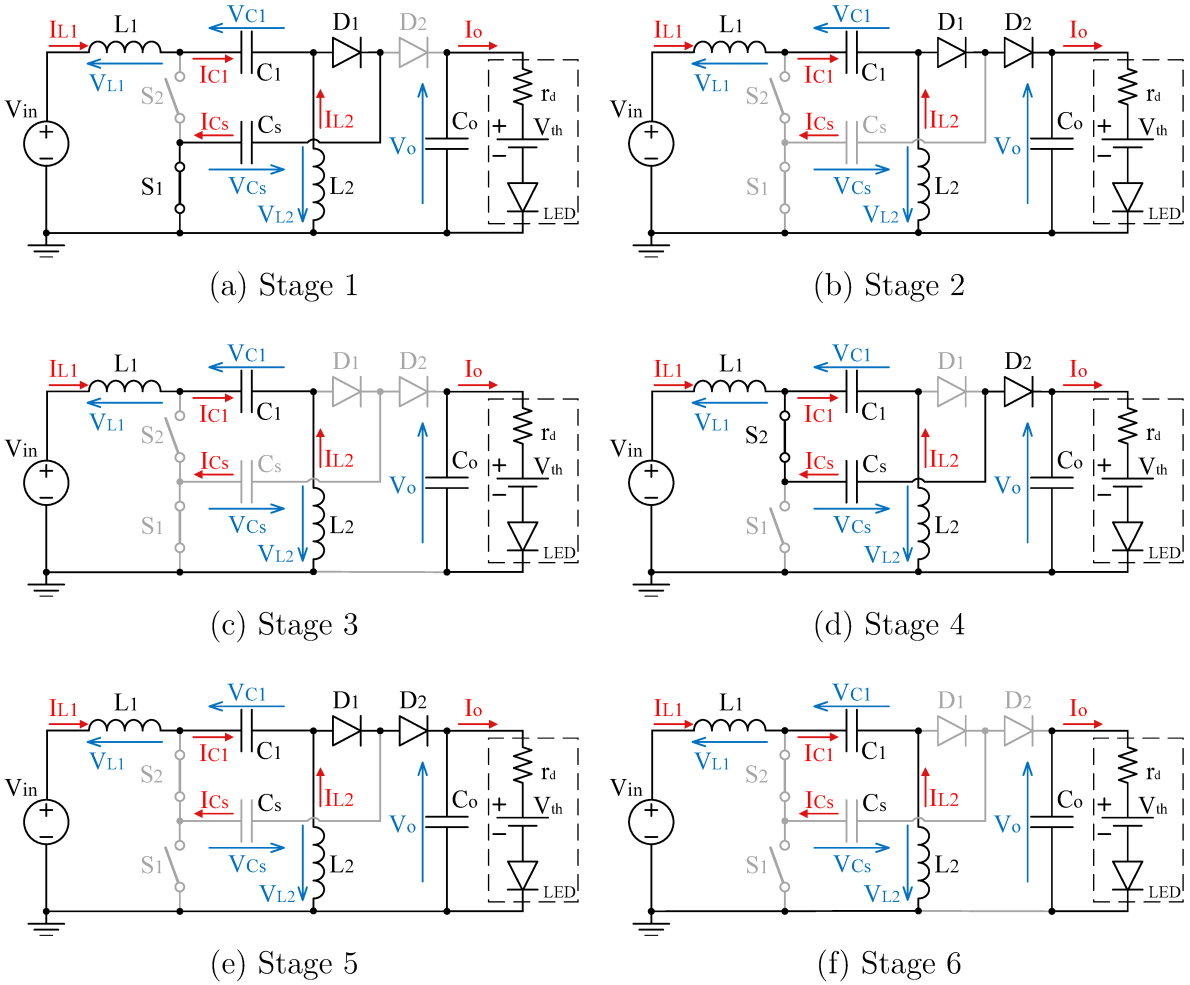


(a) (b)

Source: Author (2020).

The distinct stages of operation are shown in Figure 147.

Figure 147 – Stages of operation of the RSC SEPIC converter.



(a) Stage 1 (b) Stage 2

(c) Stage 3 (d) Stage 4

(e) Stage 5 (f) Stage 6

Source: Author (2020).

A.5.1 Input capacitor analysis

The low-frequency analysis of the converter allows for the identification of the constant average voltage at the input capacitor C_1. The appropriate loop to consider contains $[V_{in} - L_1 - C_1 - L_2]$, with the inductors being considered short-circuits with null voltage at very low frequency. The voltage at the input capacitor is then given by

$$V_{C1} = V_{in}. \tag{A.255}$$

A.5.2 Switched capacitor analysis

Once again, the maximum and minimum voltages at the switch capacitor C_s must be found in order to initiate the time analysis of the circuit. During stage 1, shown in Figure 148a, the reverse biased diode is D_2, which starts conducting when the voltage at the switching capacitor C_s reaches its maximum value. In that regard, the appropriate loop to analyze contains $[S_1 - C_s - D_2 - V_o]$, yielding a diode voltage of

$$v_{D2}(t) = V_o - v_{Cs}(t). \tag{A.256}$$

Thus, by achieving a voltage of $v_{Cs}(t) = V_o$ at the switched capacitor C_s, the diode D_2 becomes forward biased and stops the capacitor from further charging, fixing its voltage at $V_{Cs\,max} = V_o$.

In the same way, the stage 4 highlighted in Figure 148a allows for the analysis of the minimum switched capacitor voltage through the $[C_1 - S_2 - C_s - D_1]$ loop. The voltage at the reverse biased diode D_1 is then given by

$$v_{D1}(t) = V_{C1} + v_{Cs}(t). \tag{A.257}$$

Which means that in order to forward bias the diode D_1, the switched capacitor C_s must discharge down to the negative voltage of $v_{Cs}(t) = -V_{C1}$. By applying (A.255), the maximum and minimum voltage levels at the switched capacitor C_s are given by

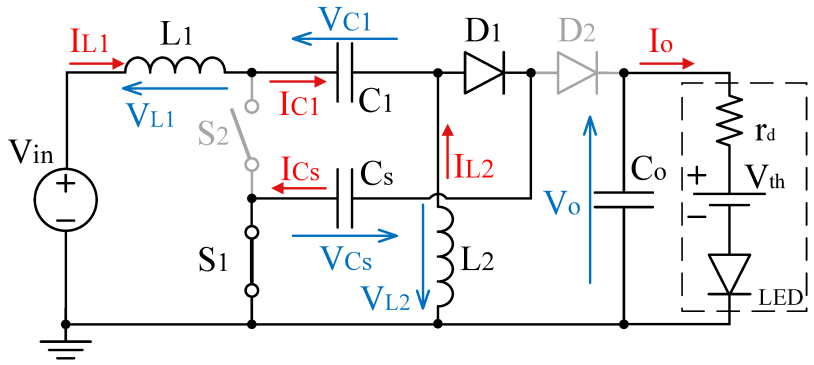
$$V_{Cs\,max} = V_o \; ; \; V_{Cs\,min} = -V_{in}. \tag{A.258}$$

A.5.3 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor Through the path shown in Figure 148. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = -V_{in} \\ i_{L_1}(t_0) = I_{L\,DCM} \\ i_{L_2}(t_0) = -I_{L\,DCM} \end{cases} \tag{A.259}$$

Figure 148 – SEPIC RSC: stage 1.



Source: Author (2020).

The behavior of each semiconductor can be found through the loop and node equations of the circuit, being summarized in Table 43.

Table 43 – Semiconductor Conditions for RSC SEPIC: stage 1.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = i_{L1}(t) + i_{L2}(t)$
S_2	Blocking	$v_{S2} = v_{Cs}(t) + V_{C1}$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described by (A.260), (A.261) and (A.262).

Time Domain		Frequency Domain
$V_{in} = L_1 \dfrac{d}{dt} i_{L1}(t) + V_{C1} + v_{Cs}(t)$	$\xrightarrow{\mathcal{L}}$	$\dfrac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \dfrac{V_{C1}}{s} + V_{Cs}(s)$ (A.260)
$v_{Cs}(t) = -L_2 \dfrac{d}{dt} i_{L2}(t)$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = -L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right)$ (A.261)
$C_s \dfrac{d}{dt} v_{Cs}(t) = i_{L1}(t) + i_{L2}(t)$	$\xrightarrow{\mathcal{L}}$	$C_s \left(s\, V_{Cs}(s) - V_{Cs(t0)}\right) = I_{L1}(s) + I_{L2}(s)$ (A.262)

Isolating each of the states for every equation yields the relations described as follows.

Isolating Switched Capacitor Voltage:		
From (A.260)	$V_{Cs}(s) = -L_1\,(s\,I_{L1}(s) - I_{L1(t0)})$	(A.263)
From (A.261)	$V_{Cs}(s) = -L_2\,(s\,I_{L2}(s) - I_{L2(t0)})$	(A.264)
From (A.262)	$V_{Cs}(s) = \dfrac{I_{L1}(s)}{C_s\,s} + \dfrac{I_{L2}(s)}{C_s\,s} + \dfrac{V_{Cs(t0)}}{s}$	(A.265)
Isolating Inductor Currents:		
From (A.260)	$I_{L1}(s) = \dfrac{-V_{Cs}(s)}{L_1\,s} + \dfrac{I_{L1(t0)}}{s}$	(A.266)
From (A.261)	$I_{L2}(s) = \dfrac{-V_{Cs}(s)}{L_2\,s} + \dfrac{I_{L2(t0)}}{s}$	(A.267)
From (A.262)	$\begin{cases} I_{L1}(s) = C_s\,s\,V_{Cs}(s) - I_{L2}(s) - C_s\,V_{Cs(t0)} \\ I_{L2}(s) = C_s\,s\,V_{Cs}(s) - I_{L1}(s) - C_s\,V_{Cs(t0)} \end{cases}$	(A.268)

Using the relation for $V_{Cs}(t)$ given by (A.265) and substituting the inductor currents given by (A.266) and (A.267) yields

$$V_{Cs}(s) = V_{Cs(t0)}\,\frac{s}{s^2 + \omega_0^2}. \tag{A.269}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = -V_{in}\,\cos(t\,\omega_0). \tag{A.270}$$

On the other hand, using the relation for the current at inductor L_1 given by (A.268) and substituting $I_{L2}(s)$ from (A.267) and $V_{Cs}(s)$ from (A.263) in that order, yields the inductor current as

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} - \frac{V_{Cs(t0)}}{L_1}\,\frac{1}{s^2 + \omega_0^2}. \tag{A.271}$$

The inverse Laplace transform gives the inductor current at the time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0). \tag{A.272}$$

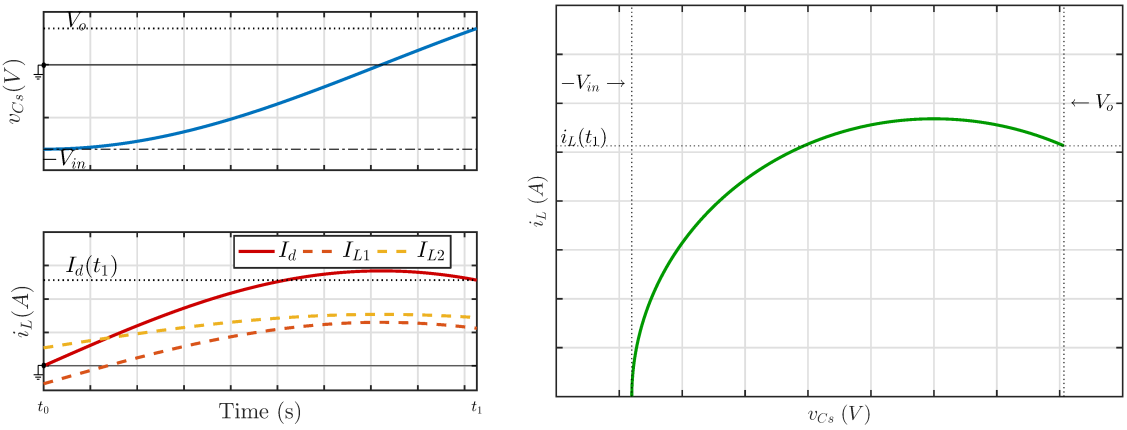
Similarly, an equivalent procedure yields the current at the inductor L_2 as

$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.273}$$

Adding the inductor currents gives the overall diode current I_d as

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.274}$$

Figure 149 – SEPIC RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

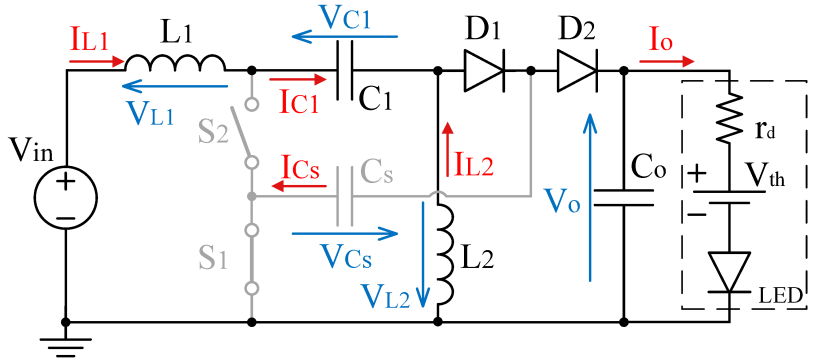
Source: Author (2020).

The resulted waveforms described are shown in Figure 149.

When the capacitor reaches sufficient voltage to forward bias the diode D_2 the remaining energy on the inductor forces a current through the passive semiconductors as seen in Figure 150. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_o \\ i_{L_1}(t_1) = I_{L1\,(t1)} \\ i_{L_2}(t_1) = I_{L2\,(t1)} \end{cases} \tag{A.275}$$

Figure 150 – SEPIC RSC: stage 2.



Source: Author (2020).

Table 44 displays the operational conditions of each semiconductor.

Table 44 – Semiconductor Conditions for RSC SEPIC: stage 2.

	State	Voltages	Currents
$\mathbf{S_1}$	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
$\mathbf{S_2}$	Blocking	$v_{S2} = V_{C1} + v_{Cs}(t)$	$i_{S2} = 0$
$\mathbf{D_1}$	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
$\mathbf{D_2}$	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described by (A.276) and (A.277).

Time Domain		Frequency Domain	
$V_{in} = L_1 \dfrac{d}{dt} i_{L1}(t) + V_{C1} + V_o$	$\xrightarrow{\mathcal{L}}$	$\dfrac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \dfrac{V_{C1} + V_o}{s}$	(A.276)
$L_2 \dfrac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = \dfrac{V_o}{s}$	(A.277)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max} = V_o. \tag{A.278}$$

The inductor behavior can be solved separately once the states don't depend on each other. Using (A.276) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.279}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t1)} - \frac{V_o}{L_1}\, t. \tag{A.280}$$

Similarly, solving (A.277) for $I_{L2}(s)$ yields

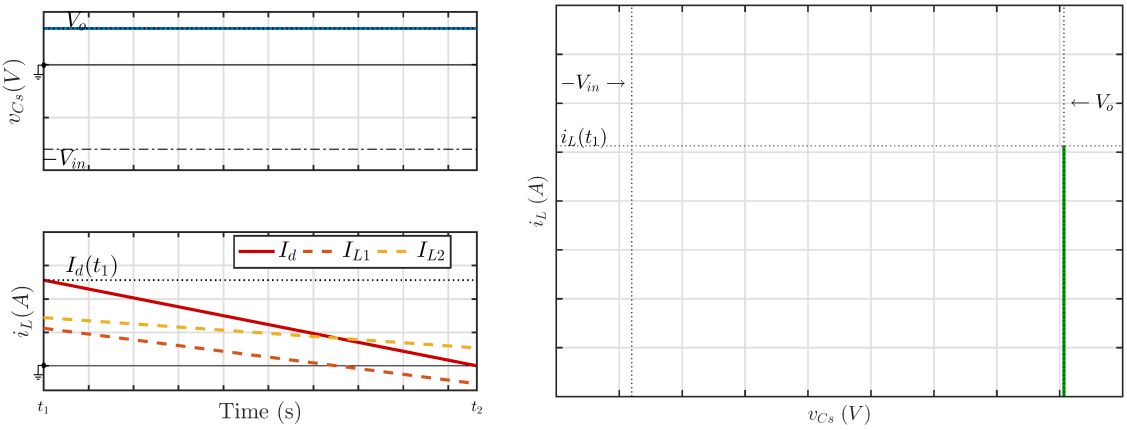
$$i_{L2}(t) = I_{L2(t1)} - \frac{V_o}{L_2}\, t. \tag{A.281}$$

Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t1)} - \frac{V_o}{L_e}\, t. \tag{A.282}$$

The resulted waveforms described are shown in Figure 151.

Figure 151 – SEPIC RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



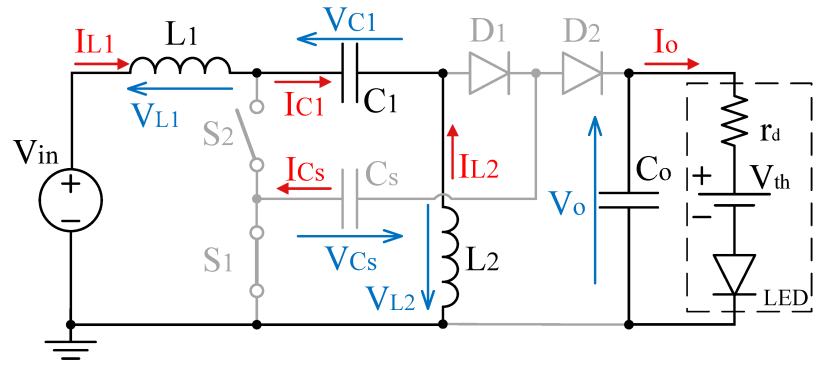
(a) (b)

Source: Author (2020).

For higher-order converters, DCM operation does not imply a complete depletion of current from the inductors since an equilibrium point where both currents cancel each other is possible, resulting in current through the path shown in Figure 152. The initial conditions for this stage are described by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_o \\ i_{L_1}(t_2) = I_{L\,DCM} \\ i_{L_2}(t_2) = -I_{L\,DCM} \end{cases} \tag{A.283}$$

Figure 152 – SEPIC RSC: stage 3.



Source: Author (2020).

The description of each semiconductor for this stage is highlighted in Table 45.

Table 45 – Semiconductor Conditions for RSC SEPIC: stage 3.

	State	Voltages	Currents
S₁	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S₂	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D₁	Blocking	$v_{D1} = v_{Cs}(t)$	$i_{D1} = 0$
D₂	Blocking	$v_{D2} = V_o - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,max} \tag{A.284}$$

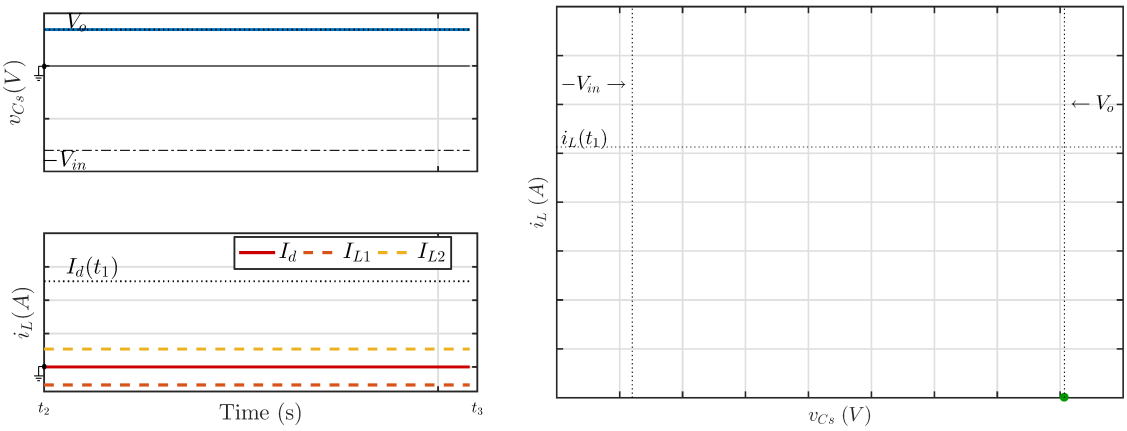
$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.285}$$

The equivalent current $i_d(t)$ is then given by

$$i_d(t) = 0. \tag{A.286}$$

The resulted waveforms described are shown in Figure 153.

Figure 153 – SEPIC RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

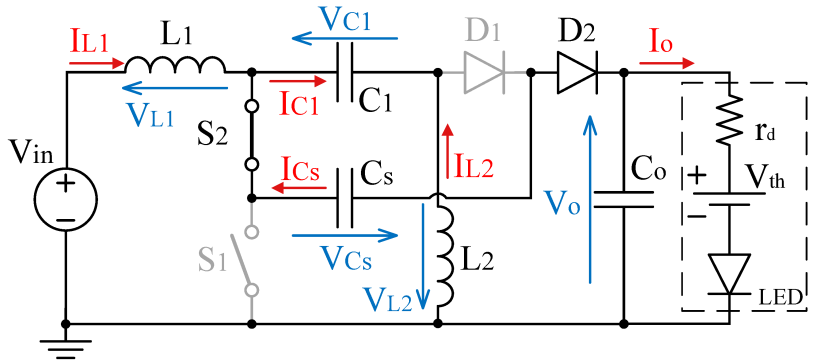
Source: Author (2020).

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1, resulting in the circuit shown in Figure 154. The switched capacitor is once again added to the active part of the circuit allowing its storage

energy to supply the load. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_o \\ i_{L_1}(t_3) = I_{L\,DCM} \\ i_{L_2}(t_3) = -I_{L\,DCM}. \end{cases} \tag{A.287}$$

Figure 154 – SEPIC RSC: stage 4.



Source: Author (2020).

The semiconductor conditions for this stage are displayed in Table 46.

Table 46 – Semiconductor Conditions for RSC SEPIC: stage 4.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_o - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = i_{L1}(t) + i_{L2}(t)$
D_1	Blocking	$v_{D1} = V_{C1} + v_{Cs}(t)$	$i_{D1} = 0$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The node and loop equations for this stage are described by (A.288), (A.289) and (A.290).

Time Domain		Frequency Domain
$V_{in} = L_1 \dfrac{d}{dt} i_{L1}(t) + V_{C1} - v_{Cs}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\dfrac{V_{in}}{s} = L_1 \left(s\, I_{L1}(s) - I_{L1(t3)}\right) - V_{Cs}(s) + \dfrac{V_o}{s}$ (A.288)
$L_2 \dfrac{d}{dt} i_{L2}(t) + V_o = V_{C1} + v_{Cs}(t)$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t3)}\right) + \frac{V_o}{s} = \dfrac{V_{C1}}{s} + V_{Cs}(s)$ (A.289)
$C_s \dfrac{d}{dt} v_{Cs}(t) = -(i_{L1}(t) + i_{L2}(t))$	$\xrightarrow{\mathcal{L}}$	$C_s \left(s\, V_{Cs}(s) - V_{Cs(t3)}\right) = -(I_{L1}(s) + I_{L2}(s))$ (A.290)

Isolating each of the states for every equation yields the relations described as follows.

Isolating Switched Capacitor Voltage:		
From (A.288)	$V_{Cs}(s) = L_1\, s\, I_{L1}(s) + \dfrac{V_o - V_{in}}{s} - L_1\, I_{L1(t3)}$	(A.291)
From (A.289)	$V_{Cs}(s) = L_2 \left(s\, I_{L2}(s) - I_{L2(t3)}\right) + \dfrac{V_o - V_{C1}}{s}$	(A.292)
From (A.290)	$V_{Cs}(s) = -\dfrac{I_{L1}(s)}{C_s\, s} - \dfrac{I_{L2}(s)}{C_s\, s} + \dfrac{V_{Cs(t3)}}{s}$	(A.293)
Isolating Inductor Currents:		
From (A.288)	$I_{L1}(s) = \dfrac{V_{Cs}(s)}{L_1\, s} + \dfrac{I_{L1(t3)}}{s} + \dfrac{V_{in} - V_o}{L_1\, s^2}$	(A.294)
From (A.289)	$I_{L2}(s) = \dfrac{V_{Cs}(s)}{L_2\, s} + \dfrac{I_{L2(t3)}}{s} + \dfrac{V_{C1} - V_o}{L_2\, s^2}$	(A.295)
From (A.290)	$\begin{cases} I_{L1}(s) = -C_s\, s\, V_{Cs}(s) - I_{L2}(s) + C_s\, V_{Cs(t3)} \\ I_{L2}(s) = -C_s\, s\, V_{Cs}(s) - I_{L1}(s) + C_s\, V_{Cs(t0)} \end{cases}$	(A.296)

Using the V_{Cs} relation given by (A.293) and substituting the I_{L1} and I_{L2} relations given from (A.294) and (A.295) respectively, the capacitor voltage can be given as

$$V_{Cs}(s) = \frac{V_o - V_{in}}{s} \frac{\omega_0^2}{s^2 + \omega_0^2} + V_o \frac{s}{s^2 + \omega_0^2}. \tag{A.297}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_o - V_{in}\left(1 - \cos(t\,\omega_0)\right). \tag{A.298}$$

Similarly, using the $I_{L1}(s)$ relation given by (A.296) following by the use of (A.295) for $I_{L2}(s)$ and (A.293) for $V_{Cs}(s)$ in that order yields

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} + \frac{V_{in}}{L_1}\,\frac{1}{s^2+\omega_0^2}. \tag{A.299}$$

The inverse Laplace transforms gives the inductor current at the time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0). \tag{A.300}$$

Using equivalent manipulation, the current for the L_2 inductor can be found as

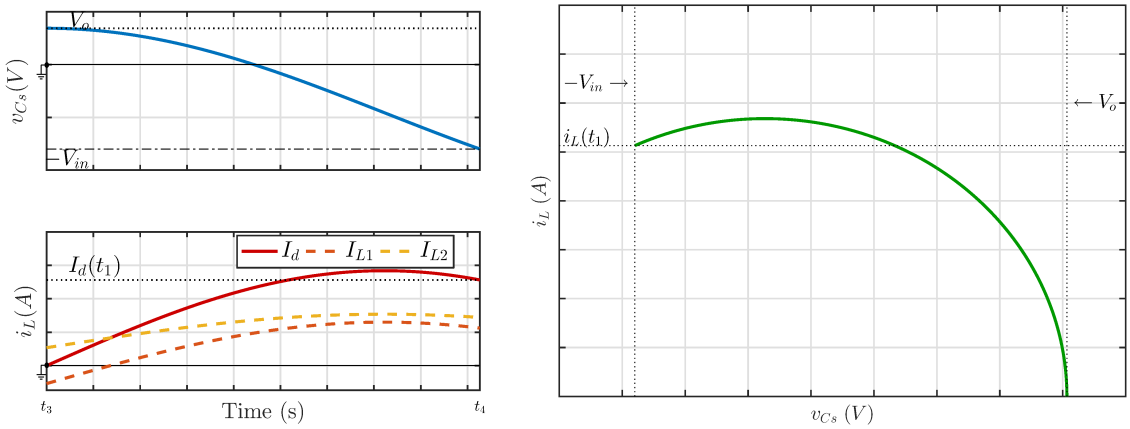
$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.301}$$

Finally, the equivalent diode current $I_d(t)$ is given by

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.302}$$

The resulted waveforms described are shown in Figure 155.

Figure 155 – SEPIC RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



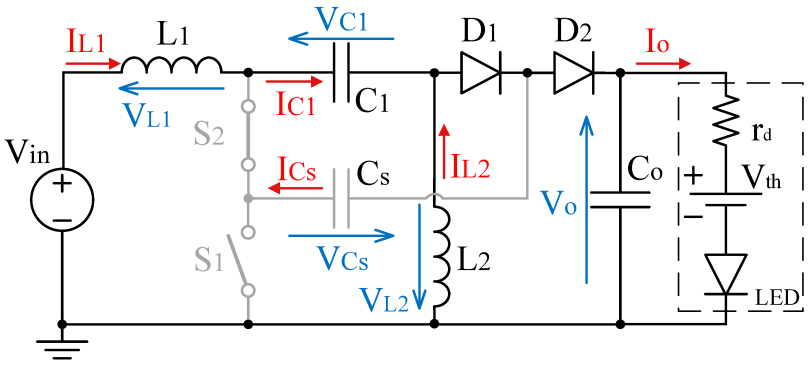
(a) (b)

Source: Author (2020).

With the capacitor reaching its minimum voltage, the diode D_1 begins conduction, which stops the discharging process of the capacitor and results in the closed path shown in Figure 156. Once again, remnant energy on the inductor forward bias both diodes creating a current flow in order to discharge it

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = -V_{in} \\ i_{L_1}(t_4) = I_{L1\,(t4)} \\ i_{L_2}(t_4) = I_{L2\,(t4)}. \end{cases} \tag{A.303}$$

Figure 156 – SEPIC RSC: stage 5.



Source: Author (2020).

Table 47 shows the semiconductor conditions for this stage.

Table 47 – Semiconductor Conditions for RSC SEPIC: stage 5.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{C1} + V_o$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described as (A.304) and (A.305).

Time Domain		Frequency Domain	
$V_{in} = L_1 \dfrac{d}{dt} i_{L1}(t) + V_{C1} + V_o$	$\xrightarrow{\mathcal{L}}$	$\dfrac{V_{in}}{s} = L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) + \dfrac{V_{C1} + V_o}{s}$	(A.304)
$L_2 \dfrac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = \dfrac{V_o}{s}$	(A.305)

During this stage the switched capacitor remains discharged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,min}. \tag{A.306}$$

The inductor behavior can be solved separately once the states don't depend on each other. Using (A.304) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.307}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t4)} - \frac{V_o}{L_1}\, t. \tag{A.308}$$

Similarly, solving (A.305) for $I_{L2}(s)$ yields

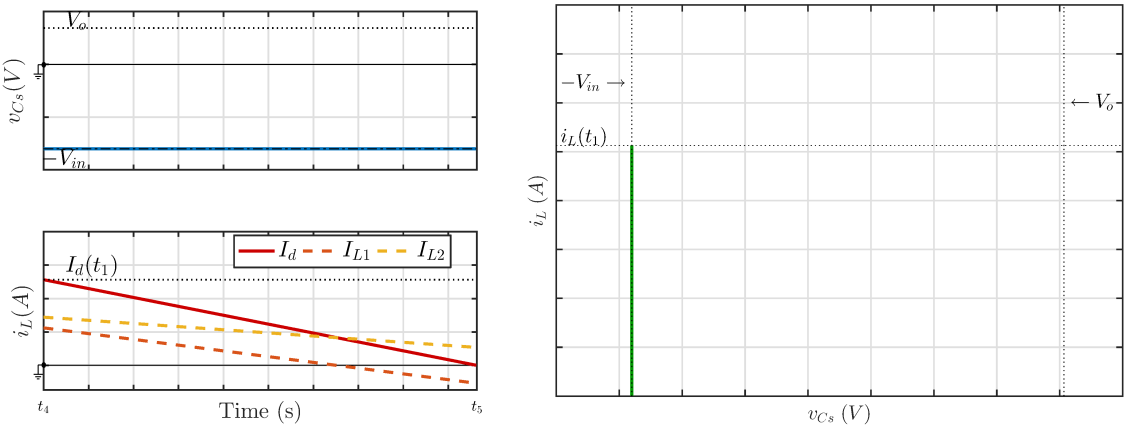
$$i_{L2}(t) = I_{L2(t4)} - \frac{V_o}{L_2}\, t. \tag{A.309}$$

Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t4)} - \frac{V_o}{L_e}\, t. \tag{A.310}$$

The resulted waveforms described are shown in Figure 157.

Figure 157 – SEPIC RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



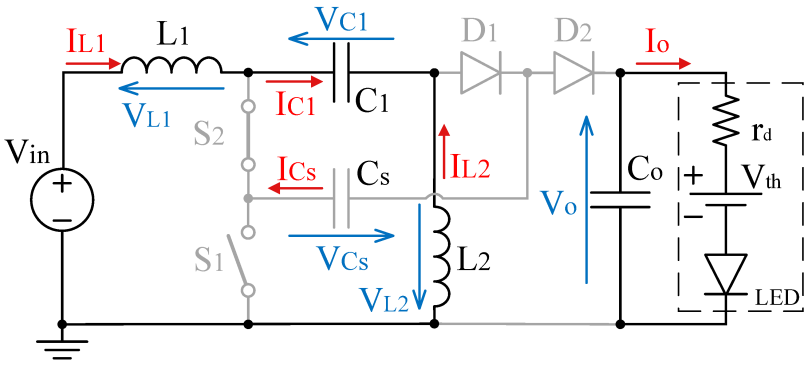
(a) (b)

Source: Author (2020).

Once again, this stage is characterized by a null current through the diodes, caused by the inductor currents reaching a point of mutual cancellation through the path highlighted in Figure 158. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = -V_{in} \\ i_{L_1}(t_5) = I_{L\,DCM} \\ i_{L_2}(t_5) = -I_{L\,DCM} \end{cases} \tag{A.311}$$

Figure 158 – SEPIC RSC: stage 6.



Source: Author (2020).

The semiconductor behavior for this stage are displayed in Table 48.

Table 48 – Semiconductor Conditions for RSC SEPIC: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = V_{C1} + v_{Cs}(t)$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - v_{Cs}(t) - V_{in}$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,min} \tag{A.312}$$

$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.313}$$

The equivalent current $i_d(t)$ is then given by

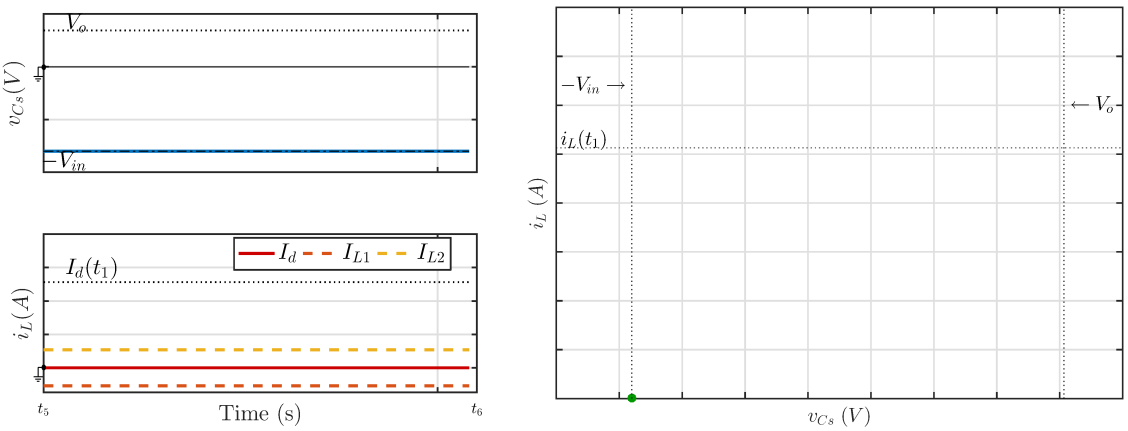
$$i_d(t) = 0. \tag{A.314}$$

The resulted waveforms described are shown in Figure 159.

A.5.4 Time Analysis

In order to fully characterize the behavior of the converter, the time delay of each state must be determined.

Figure 159 – SEPIC RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.5.4.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using (A.270) it is known that

$$v_{Cs}(t_1) = -V_{in}\,\cos(\Delta t_1\,\omega_0) = V_o. \tag{A.315}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{-V_o}{V_{in}}\right) = \frac{1}{\omega_0}\,acos\left(-G\right). \tag{A.316}$$

Applying the time duration for stage 1 into (A.272) it is possible to find the current at the L_1 inductor by the end of that stage, required as one of the initial conditions for stage 2:

$$I_{L1\,t1} = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t_1\,\omega_0) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sqrt{1-G^2}. \tag{A.317}$$

Similarly, the current at $t = t_1$ for L_2 inductor is given by

$$I_{L2\,t1} = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t_1\,\omega_0) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sqrt{1-G^2}. \tag{A.318}$$

And by adding both equations, the equivalent current $i_d(t)$ at the same instant is given by the sum of both inductor currents, given by

$$I_{d(t1)} = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sqrt{1-G^2}. \tag{A.319}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1 - G^2 > 0$, which results in a design requirement given in (A.320):

$$G < 1. \tag{A.320}$$

A.5.4.2 Stages 2 and 5

The second stage is characterized by the mutual cancellation of the inductor currents until no current is left to forward bias the diodes. Henceforth, for the higher-order converters this stage is reached not when a given inductor current reaches zero, but when the sum of the inductor currents does. From (A.282) and (A.319) it is known that

$$i_d(t_2) = I_{d(t1)} - \frac{V_o}{L_e}\,\Delta t_2 = \frac{V_{in}}{L_e\,\omega_0}\,\sqrt{1-G^2} - \frac{V_o}{L_e}\,\Delta t_2 = 0. \tag{A.321}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,G}\,\sqrt{1-G^2}. \tag{A.322}$$

A.5.4.3 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement must be noted:

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2}. \tag{A.323}$$

which expands to

$$\frac{1}{\omega_0}\,acos\,(-G) + \frac{1}{\omega_0\,G}\,\sqrt{1-G^2} < \frac{1}{2\,f_s}. \tag{A.324}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\,f_s\,\left(acos\,(-G) + \frac{1}{G}\,\sqrt{1-G^2}\right). \tag{A.325}$$

A.5.5 Average Equivalent Diode Current

The average inductor current is found by integrating the equivalent diode waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period:

$$I_{Ld} = \frac{1}{T_s/2}\,\left(\int_{t_0}^{t_1}[i_{L1}(t)_1 + i_{L2}(t)_1]dt + \int_{t_1}^{t_2}[i_{L1}(t)_2 + i_{L2}(t)_2]dt\right) \tag{A.326}$$

$$I_{Ld} = 2\,f_s\,\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{d(t1)} - \frac{V_o}{L_e}\,t\,dt\right). \tag{A.327}$$

Solving the equation above and making use of the relations given by (A.316), (A.319) and (A.322), the average output current can be simplified as (A.328).

$$I_d = C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}. \tag{A.328}$$

A.5.6 DCM Current Offset

For the higher-order converters DCM operation does not imply on null current values for inductors during stage three. This characteristic is due to the capability of the inductors on storing energy such that the its opposite values of constant current can cancel each other and are therefore unable to keep the diodes under forward bias.

In order to accurately characterize the current on the inductors, this constant current level of opposite values must be found, which requires an additional steady-state description of the system (ZHU; LUO; HE, 2008). This new description can be made for the charge balance of the input capacitor C_1 in high-frequency.

As stated, the capacitor C_1 is at first considered as a constant-voltage component which simplifies the calculations while still maintaining certain accuracy given a high capacitance value. Still, the voltage at the capacitor is directly affected by the charge count in each instant which is consequently an integration of the current waveform. Once the currents at the capacitor C_1 are not constant, it can be assumed a high-frequency voltage change in the capacitor related to the charge differences between stages. Yet, for a given switching period, it is expected that the initial and final changes of charge can cancel themselves in order to maintain constant voltage. This statement can be mathematically described as

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{C1}(t)_1 dt + \int_{t_1}^{t_2} i_{C1}(t)_2 dt + \int_{t_2}^{t_3} i_{C1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} i_{C1}(t)_4 dt + \int_{t_4}^{t_5} i_{C1}(t)_5 dt + \int_{t_5}^{t_6} i_{C1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.329}$$

During stage 4, the input capacitor current is the opposite to the current at inductor L_2 according to the assigned positive current flow for each component. For every other stage, the input capacitor current is the same as the current at inductor L_1 which van be translated to

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{L1}(t)_1 dt + \int_{t_1}^{t_2} i_{L1}(t)_2 dt + \int_{t_2}^{t_3} i_{L1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} -i_{L2}(t)_4 dt + \int_{t_4}^{t_5} i_{L1}(t)_5 dt + \int_{t_5}^{t_6} i_{L1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.330}$$

Replacing the inductor waveforms on the equation above yields

$$\begin{aligned}\int_{t_0}^{t_1} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sin(t\,\omega_0)dt + &\int_{t_1}^{t_2} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_2}^{t_3} I_{L\,DCM} dt + \int_{t_3}^{t_4} -\left(-I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\sin(t\,\omega_0)\right) dt + \\ &+ \int_{t_4}^{t_5} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_5}^{t_6} I_{L\,DCM} dt = 0.\end{aligned} \tag{A.331}$$

Solving the equation for $I_{L\,DCM}$ and using the time steps defined in the previous section yields

$$I_{L\,DCM} = C_s\,V_{in}\,f_s\,\frac{G+1}{G}\,\frac{G\,L_1 - L_2}{L_1 + L_2}, \tag{A.332}$$

which can also be written as

$$I_{L\,DCM} = \frac{I_d}{G+1}\,\frac{G\,L_1 - L_2}{L_1 + L_2}. \tag{A.333}$$

A.5.7 Average Output Current

For the SEPIC converter, the output current is the same as the current at diode D_2. Integrating its waveform over a period of time equal to the switching period yields the average output current

$$I_o = \frac{1}{T_s}\left(\int_{t_0}^{t_1} 0dt + \int_{t_1}^{t_2} i_d(t)_2 dt \int_{t_2}^{t_3} i_d(t)_3 dt \int_{t_3}^{t_4} i_d(t)_4 dt \int_{t_4}^{t_5} i_d(t)_5 dt \int_{t_5}^{t_6} i_d(t)_6 dt\right) \tag{A.334}$$

$$I_o = f_s\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + 2\cdot\int_{t_1}^{t_2} I_{d(t1)} - \frac{V_o}{L_e}\,t\,dt\right). \tag{A.335}$$

Solving the equation above and making use of the relations given by (A.316), (A.319) and (A.322), the average output current can be simplified as (A.336)

$$I_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}. \tag{A.336}$$

A.5.8 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\,V_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}\,V_o. \tag{A.337}$$

Using the static gain definition stated as $V_o = G\,V_{in}$ the output power is given by

$$P_o = C_s\,f_s\,V_{in}^2\,(G+1). \tag{A.338}$$

The capacitor must be sized accordingly to the output power, relation given by (A.339):

$$C_s = \frac{P_o}{f_s\,V_{in}^2\,(G+1)}. \tag{A.339}$$

A.5.9 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 49.

Table 49 – RSC SEPIC simulation values fos (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

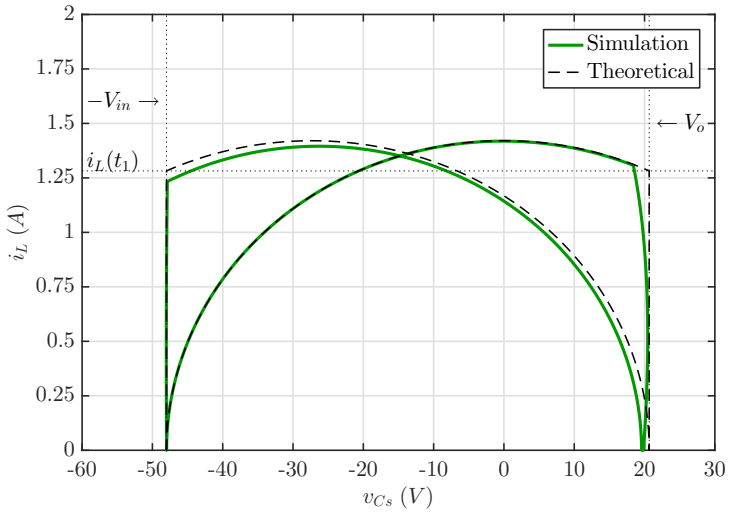
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Input Capacitance	C_1	$470\,nF$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$6.8\,nF$
Input Inductance	L_1	$12\,\mu H$
Output Inductance	L_2	$22\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 160 yields a precise comparison between theoretical prediction and simulation result. The presence of the output loop seems to alter stage 2, adding a dynamics that disallow the expected constant-voltage line. This dissonance, however, seems sufficiently small.

Figure 160 – State Plan for the RSC SEPIC converter.

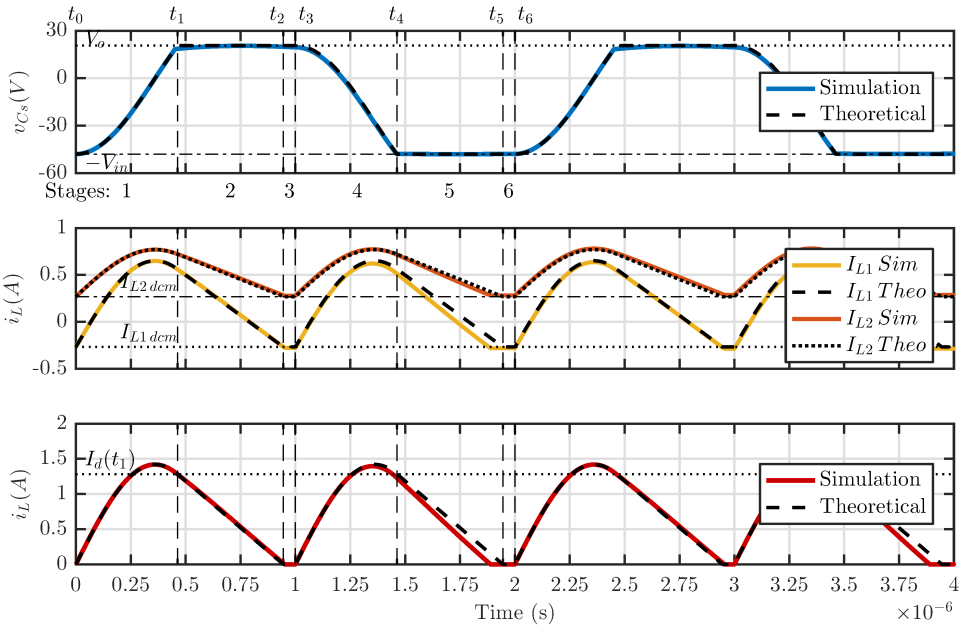


Source: Author (2020).

The waveform comparison of the RSC SEPIC converter states for each stage in their respective timespans is shown in Figure 161, following prediction as expected except by the inductor demagnetizing of state 5, that occurs faster than expected. The previous noticed dissonance on the maximum switched capacitor voltage is shown to be imperceptible in the time domain analysis.

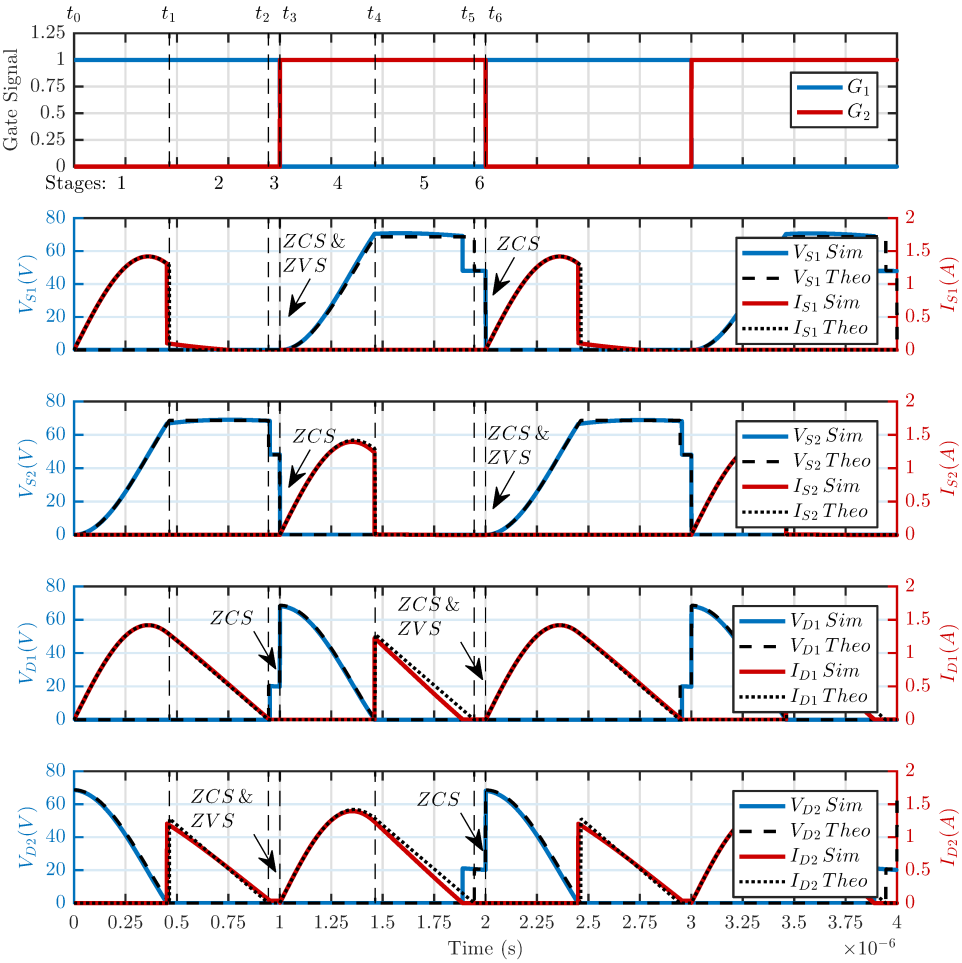
Finally, Figure 162 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 161 – Theoretical waveforms of the state variables for the RSC SEPIC converter.



Source: Author (2020).

Figure 162 – Soft-switching on the semiconductors for the RSC SEPIC converter.

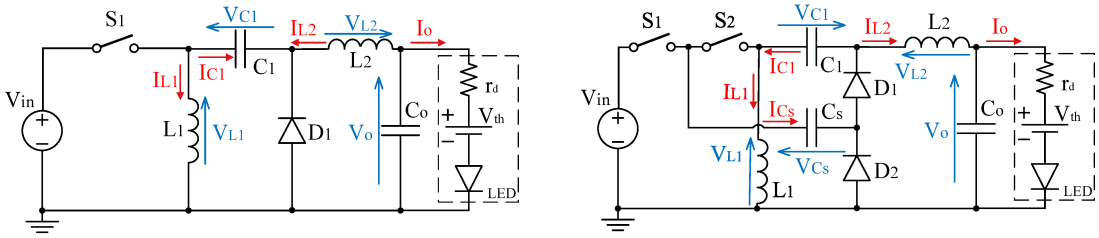


Source: Author (2020).

A.6 RSC ZETA ANALYSIS

The Zeta converter is displayed on Figure 163 as well as the RSC Zeta converter.

Figure 163 – Classic Zeta converter (a) and RSC Zeta converter (b).

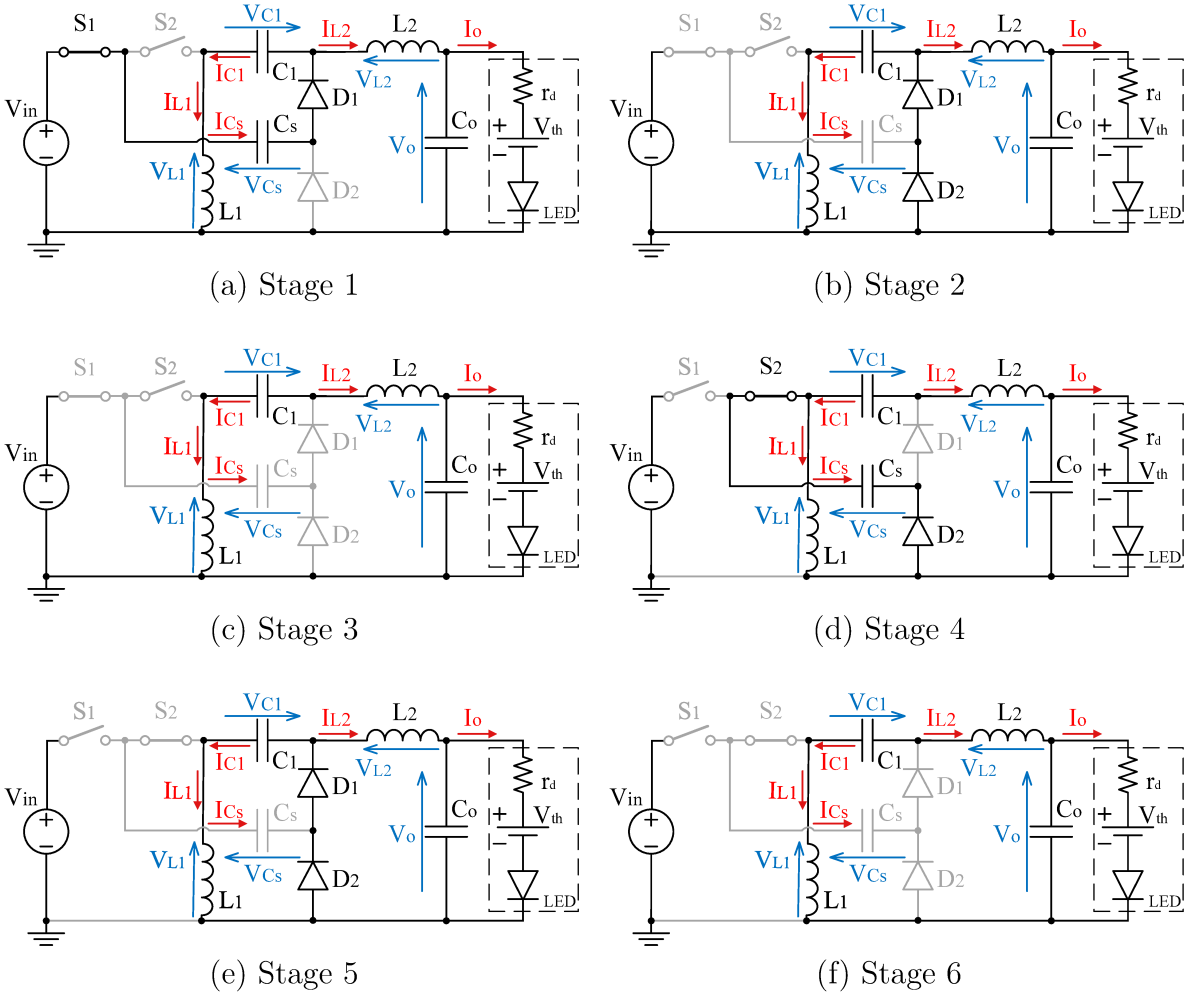


(a) (b)

Source: Author (2020).

The operation of the circuit can, once again, be divided in six separate stages, highlighted in Figure 147.

Figure 164 – Stages of operation of the RSC Zeta converter.



(a) Stage 1 (b) Stage 2

(c) Stage 3 (d) Stage 4

(e) Stage 5 (f) Stage 6

Source: Author (2020).

A.6.1 Input capacitor analysis

In order to begin the circuit analysis, the voltage across the input capacitor C_1 must be determined by approximating it to a constant value. This simplification is valid if considered a high enough input capacitance that reduces the resonant frequency between this capacitor and the other reactive elements of the circuit. Thus, a low-frequency analysis of the circuit yields this average constant value for the V_{C1} voltage through the loop $[L_1 - C_1 - L_2 - V_o]$. By considering the inductances as short-circuits of null average voltages (an implication of the low-frequency analysis) the voltage at the input capacitor is given by

$$V_{C1} = V_o. \tag{A.340}$$

A.6.2 Switched capacitor analysis

With the voltage at input capacitor C_1 known, the respective loops can be analyzed in order to determine maximum and minimum voltages at switched capacitor C_s. The maximum voltage is the one required to forward bias the blocking diode at stage 1, displayed ad 165a. The appropriate loop to analyze contains $[V_{in} - S_1 - C_s - D_2]$, yielding a diode D_2 voltage of

$$v_{D2}(t) = V_{in} - v_{Cs}(t). \tag{A.341}$$

The maximum possible voltage at the switched capacitor C_s is then determined as $V_{Cs\,max} = V_{in}$, the required voltage to allow conduction at diode D_2, stopping the switched capacitor C_s of further charging.

Similarly, Figure 165d displays stage 4, where the $[C_s - S_2 - C_1 - D_1]$ loop defines the minimum voltage at the switched capacitor C_s required to allow the reverse biased diode D_1 to start conducting. The voltage at the D_1 diode is then given by

$$v_{D1}(t) = V_{C1} + v_{Cs}(t). \tag{A.342}$$

Once again, in order to allow conduction at the D_1 diode, the switched capacitor C_s must discharge down to the negative value of V_{C1}, nulling it in the voltage loop. Having known the input capacitor voltage V_{C1} from (A.340), the maximum and minimum voltages at the switched capacitor can be summarized as

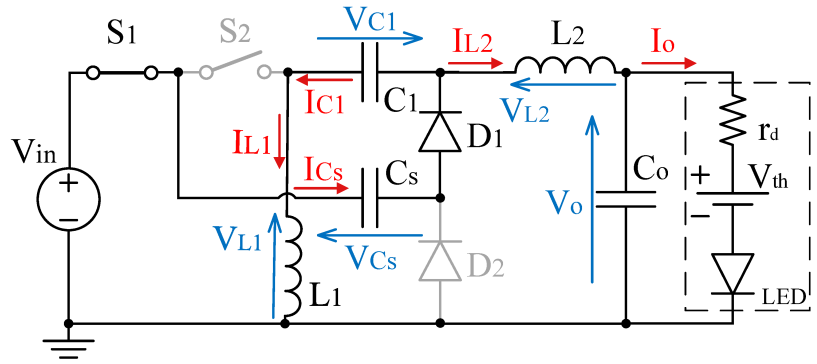
$$V_{Cs\,max} = V_{in}\ ;\ V_{Cs\,min} = -V_o. \tag{A.343}$$

A.6.3 Circuit Analysis

The first stage is characterized by the charging of the switched capacitor due to the closed path shown in Figure 165. The initial conditions are given by

$$\begin{cases} v_{Cs}(t_0) = V_{Cs\,min} = -V_o \\ i_{L_1}(t_0) = I_{L\,DCM} \\ i_{L_2}(t_0) = -I_{L\,DCM} \end{cases} \tag{A.344}$$

Figure 165 – Zeta RSC: stage 1.



Source: Author (2020).

The conditions of current and voltage for each semiconductor can be found through loop and node equations, and are summarized in Table 50.

Table 50 – Semiconductor Conditions for RSC Zeta: stage 1.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = i_{L1}(t) + i_{L2}(t)$
S_2	Blocking	$v_{S2} = v_{Cs}(t) + V_{C1}$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
D_2	Blocking	$v_{D2} = V_{in} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

The node and loop equations for this stage are described by (A.345) and (A.346).

Time Domain		Frequency Domain	
$V_{in} = v_{Cs}(t) + V_{C1} + L_1 \frac{d}{dt} i_{L1}(t)$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + \frac{V_{C1}}{s} + L_1 \left(s\, I_L(s) - I_{L1(t0)}\right)$	(A.345)
$V_{in} = v_{Cs}(t) + L_2 \frac{d}{dt} i_{L2}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$\frac{V_{in}}{s} = V_{Cs}(s) + L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) + \frac{V_o}{s}$	(A.346)
$C_s \frac{d}{dt} v_{Cs}(t) = i_{L1}(t) + i_{L2}(t)$	$\xrightarrow{\mathcal{L}}$	$C_s \left(s\, V_{Cs}(s) - V_{Cs(t0)}\right) = I_{L1}(s) + I_{L2}(s)$	(A.347)

Isolating each of the states for every equation yields the relations described as follows.

	Isolating Switched Capacitor Voltage:	
From (A.345)	$V_{Cs}(s) = -L_1 \left(s\, I_{L1}(s) - I_{L1(t0)}\right) + \frac{V_{in} - V_{C1}}{s}$	(A.348)
From (A.346)	$V_{Cs}(s) = -L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) + \frac{V_{in} - V_o}{s}$	(A.349)
From (A.347)	$V_{Cs}(s) = \frac{I_{L1}(s)}{C_s\, s} + \frac{I_{L2}(s)}{C_s\, s} + \frac{V_{Cs(t0)}}{s}$	(A.350)
	Isolating Inductor Currents:	
From (A.345)	$I_{L1}(s) = \frac{-V_{Cs}(s)}{L_1\, s} + \frac{I_{L1(t0)}}{s} + \frac{V_{in} - V_{C1}}{L_1\, s^2}$	(A.351)
From (A.346)	$I_{L2}(s) = \frac{-V_{Cs}(s)}{L_2\, s} + \frac{I_{L2(t0)}}{s} + \frac{V_{in} - V_o}{L_2\, s^2}$	(A.352)
From (A.347)	$\begin{cases} I_{L1}(s) = C_s \left(s\, V_{Cs}(s) - V_{Cs(t0)}\right) - I_{L2}(s) \\ I_{L2}(s) = C_s \left(s\, V_{Cs}(s) - V_{Cs(t0)}\right) - I_{L1}(s) \end{cases}$	(A.353)

Using the relation for $V_{Cs}(t)$ given by (A.348) and substituting the inductor currents given by (A.351) and (A.352) yields

$$V_{Cs}(s) = V_{Cs(t0)} \frac{s}{s^2 + \omega_0^2} + \frac{V_{in} - V_o}{s} \frac{\omega_0^2}{s^2 + \omega_0^2}. \tag{A.354}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in} \left(1 - \cos(t\, \omega_0)\right) - V_o. \tag{A.355}$$

On the other hand, using the relation for the current at inductor L_1 given by (A.353) and substituting $I_{L2}(s)$ from (A.352) and $V_{Cs}(s)$ from (A.348) in that order, yields the inductor current as

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} - \frac{V_{Cs(t0)}}{L_1} \frac{1}{s^2 + \omega_0^2}. \tag{A.356}$$

The inverse Laplace transforms gives the inductor current at the time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0). \tag{A.357}$$

Similarly, an equivalent procedure yields the current at the inductor L_2 as

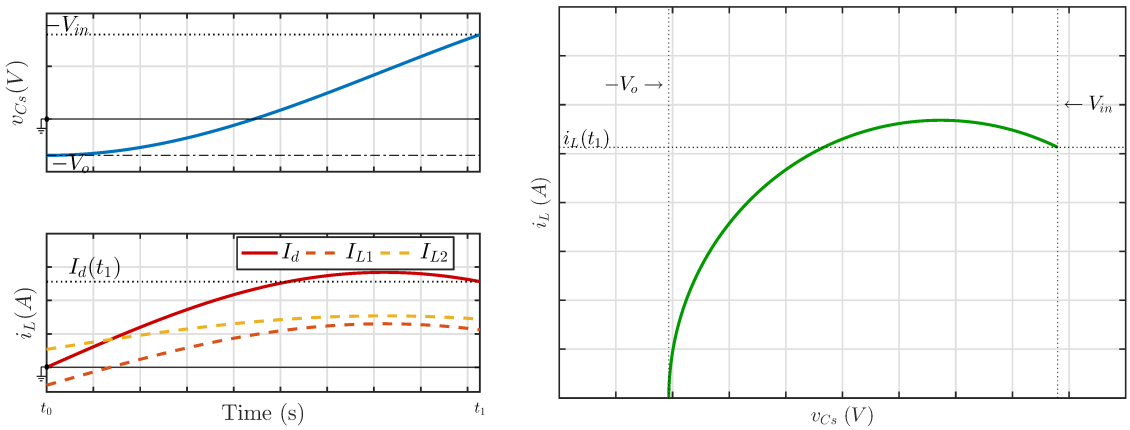
$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.358}$$

Adding the inductor currents gives the overall diode current I_d as

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.359}$$

The resulted waveforms described are shown in Figure 166.

Figure 166 – Zeta RSC: stage 1 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



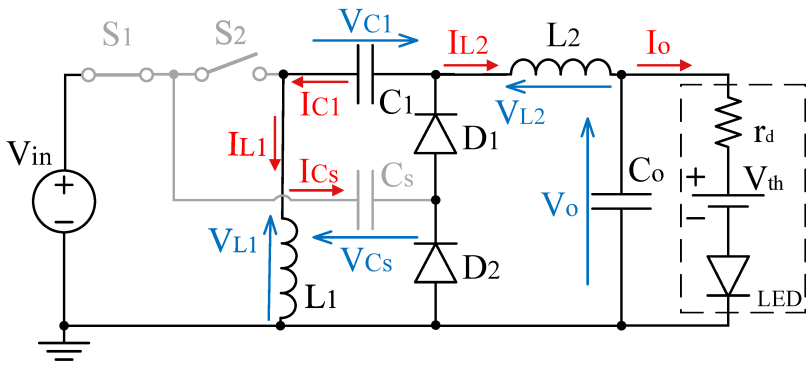
(a) (b)

Source: Author (2020).

When the capacitor reaches sufficient voltage to forward bias the diode D_2 the remaining energy on the inductor forces a current through the passive semiconductors in the path described in Figure 167. Once the diode D_2 starts and keeps conducting current, the voltage at the capacitor is forced to remain unchanged, keeping its maximum value. The remaining energy at the inductor is described through its current during the time $t = t_1$. The initial condition of this stage therefore is described by

$$\begin{cases} v_{Cs}(t_1) = V_{Cs\,max} = V_{in} \\ i_{L_1}(t_1) = I_{L1\,(t1)} \\ i_{L_2}(t_1) = I_{L2\,(t1)} \end{cases} \tag{A.360}$$

Figure 167 – Zeta RSC: stage 2.



Source: Author (2020).

The semiconductor conditions of current and voltage for this stage are shown in Table 51.

Table 51 – Semiconductor Conditions for RSC Zeta: stage 2.

	State	Voltages	Currents
S1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S2	Blocking	$v_{S2} = V_{C1} + v_{Cs}(t)$	$i_{S2} = 0$
D1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
D2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described through (A.361) and (A.362).

Time Domain		Frequency Domain	
$L_1 \frac{d}{dt} i_{L1}(t) = -V_{C1}$	$\xrightarrow{\mathcal{L}}$	$L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) = -\frac{V_{C1}}{s}$	(A.361)
$L_2 \frac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = \frac{V_o}{s}$	(A.362)

During this stage the switched capacitor remains charged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,max} = V_{in}. \tag{A.363}$$

The inductor behavior can be solved separately once the states don't depend on each other. Using the relation (A.361) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.364}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t1)} - \frac{V_o}{L_1}\, t. \tag{A.365}$$

Similarly, solving relation (A.362) for $I_{L2}(s)$ yields

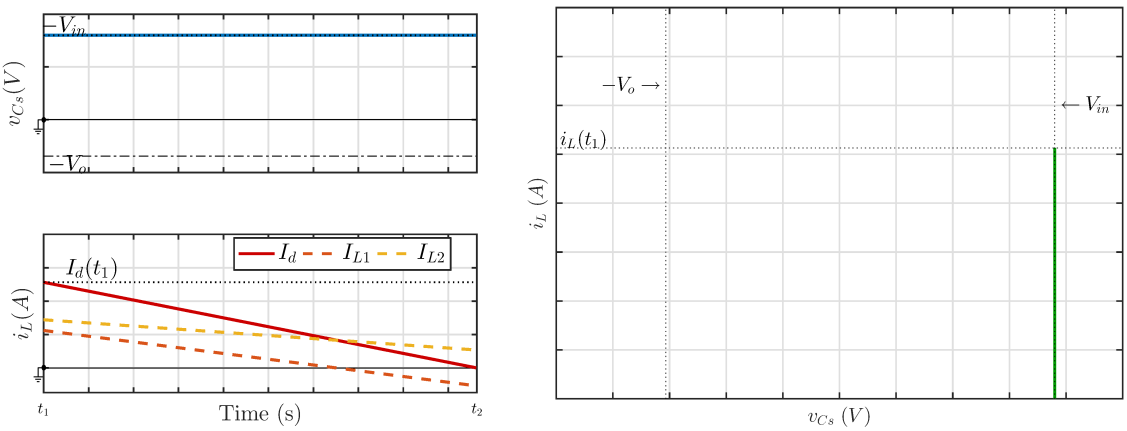
$$i_{L2}(t) = I_{L2(t1)} - \frac{V_o}{L_2}\, t. \tag{A.366}$$

Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t1)} - \frac{V_o}{L_e}\, t. \tag{A.367}$$

The resulted waveforms described are shown in Figure 168.

Figure 168 – Zeta RSC: stage 2 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



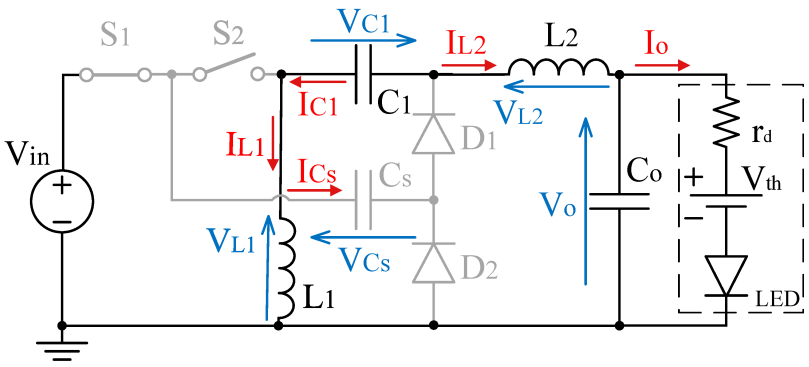
(a) (b)

Source: Author (2020).

For higher-order converters, DCM operation does not imply a complete depletion of current from the inductors since an equilibrium point where both currents cancel each other is possible in the path shown in Figure 169. The initial conditions for this stage are described by

$$\begin{cases} v_{Cs}(t_2) = V_{Cs\,max} = V_{in} \\ i_{L_1}(t_2) = I_{L\,DCM} \\ i_{L_2}(t_2) = -I_{L\,DCM} \end{cases} \tag{A.368}$$

Figure 169 – Zeta RSC: stage 3.



Source: Author (2020).

Talbe 52 describes the current and voltage conditions for each semiconductor.

Table 52 – Semiconductor Conditions for RSC Zeta: stage 3.

	State	Voltages	Currents
S_1	Conducting	$v_{S1} = 0$	$i_{S1} = 0$
S_2	Blocking	$v_{S2} = V_{in}$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t) + V_o - V_{in}$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_{in} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,max} = V_{in} \tag{A.369}$$

$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.370}$$

The equivalent current $i_d(t)$ is then given by

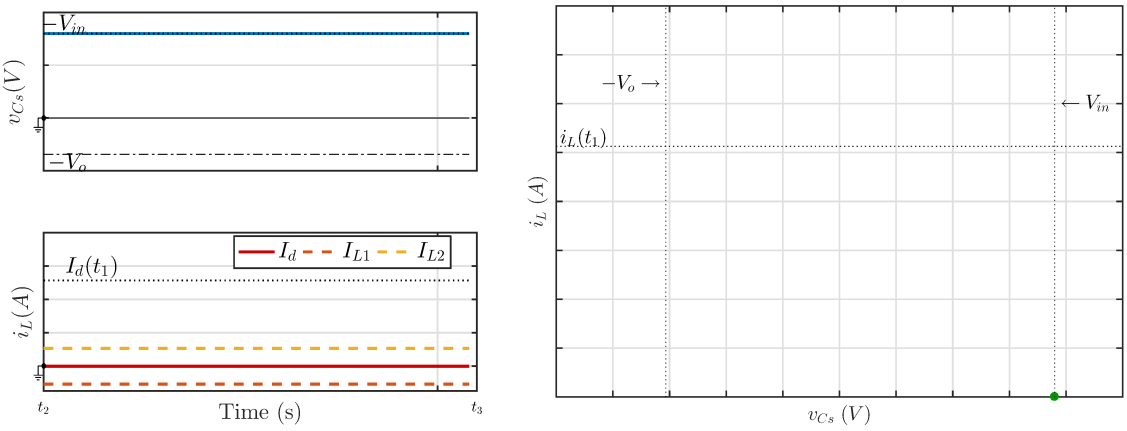
$$i_d(t) = 0. \tag{A.371}$$

The resulted waveforms described are shown in Figure 170.

The second half of the switching period is initiated when the active switch S_2 begins conducting as oppose to S_1. The switched capacitor is once again added to the active part of the circuit allowing its storage energy to supply the load as described by Figure 171. The initial conditions of this stage are given by

$$\begin{cases} v_{Cs}(t_3) = V_{Cs\,max} = V_{in} \\ i_{L_1}(t_3) = I_{L\,DCM} \\ i_{L_2}(t_3) = -I_{L\,DCM}. \end{cases} \tag{A.372}$$

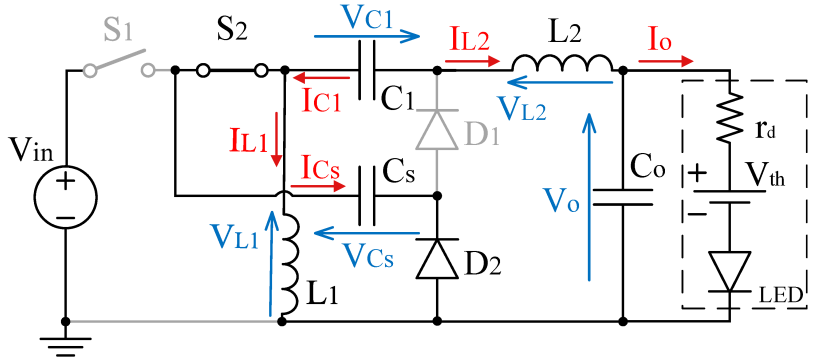
Figure 170 – Zeta RSC: stage 3 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

Figure 171 – Zeta RSC: stage 4.



Source: Author (2020).

Node and loop equations yield the semiconductor behavior during this stage, highlighted in Table 53.

Table 53 – Semiconductor Conditions for RSC Zeta: stage 4.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = i_{L1}(t) + i_{L2}(t)$
D_1	Blocking	$v_{D1} = V_{C1} + v_{Cs}(t)$	$i_{D1} = 0$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The node and loop equations for this stage are described by (A.373), (A.374) and (A.375).

Time Domain		Frequency Domain
$v_{Cs}(t) = L_1 \frac{d}{dt} i_{L1}(t)$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = L_1 \left(s\, I_{L1}(s) - I_{L1(t3)}\right)$ (A.373)
$v_{Cs}(t) = -V_{C1} + L_2 \frac{d}{dt} i_{L2}(t) + V_o$	$\xrightarrow{\mathcal{L}}$	$V_{Cs}(s) = -\frac{V_{C1}}{s} + L_2 \left(s\, I_{L2}(s) - I_{L2(t3)}\right) + \frac{V_o}{s}$ (A.374)
$C_s \frac{d}{dt} v_{Cs}(t) = -(i_{L1}(t) + i_{L2}(t))$	$\xrightarrow{\mathcal{L}}$	$C_s \left(s\, V_{Cs}(s) - V_{Cs(t3)}\right) = -(I_{L1}(s) + I_{L2}(s))$ (A.375)

Isolating each of the states for every equation yields the relations described as follows.

Isolating Switched Capacitor Voltage:		
From (A.373)	$V_{Cs}(s) = L_1 \left(s\, I_{L1}(s) - I_{L1(t3)}\right)$	(A.376)
From (A.374)	$V_{Cs}(s) = L_2 \left(s\, I_{L2}(s) - I_{L2(t3)}\right) + \frac{V_o - V_{C1}}{s}$	(A.377)
From (A.375)	$V_{Cs}(s) = -\frac{I_{L1}(s)}{C_s\, s} - \frac{I_{L2}(s)}{C_s\, s} + \frac{V_{Cs(t3)}}{s}$	(A.378)
Isolating Inductor Currents:		
From (A.373)	$I_{L1}(s) = \frac{V_{Cs}(s)}{L_1\, s} + \frac{I_{L1(t3)}}{s}$	(A.379)
From (A.374)	$I_{L2}(s) = \frac{V_{Cs}(s)}{L_2\, s} + \frac{I_{L2(t3)}}{s} + \frac{V_o - V_{C1}}{L_2\, s^2}$	(A.380)
From (A.375)	$\begin{cases} I_{L1}(s) = -C_s\, s\, V_{Cs}(s) - I_{L2}(s) + C_s\, V_{Cs(t3)} \\ I_{L2}(s) = -C_s\, s\, V_{Cs}(s) - I_{L1}(s) + C_s\, V_{Cs(t0)} \end{cases}$	(A.381)

Using the V_{Cs} relation given by (A.378) and substituting the I_{L1} and I_{L2} relations given from (A.379) and (A.380) respectively, the capacitor voltage can be given as

$$V_{Cs}(s) = V_{in}\, \frac{s}{s^2 + \omega_0^2}. \tag{A.382}$$

Applying the inverse Laplace transform, the capacitor voltage on the first stage is defined at the time domain by

$$v_{Cs}(t) = V_{in}\, \cos(t\, \omega_0). \tag{A.383}$$

Similarly, using the $I_{L1}(s)$ relation given by (A.353) following by the use of relations (A.352) for $I_{L2}(s)$ and (A.348) for $V_{Cs}(s)$ in that order yields

$$I_{L1}(s) = \frac{I_{L\,DCM}}{s} + \frac{V_{in}}{L_1}\, \frac{1}{s^2 + \omega_0^2}. \tag{A.384}$$

the inverse Laplace transforms gives the inductor current at the time domain as

$$i_{L1}(t) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t\,\omega_0), \tag{A.385}$$

Using equivalent manipulation, the current for the L_2 inductor can be found as

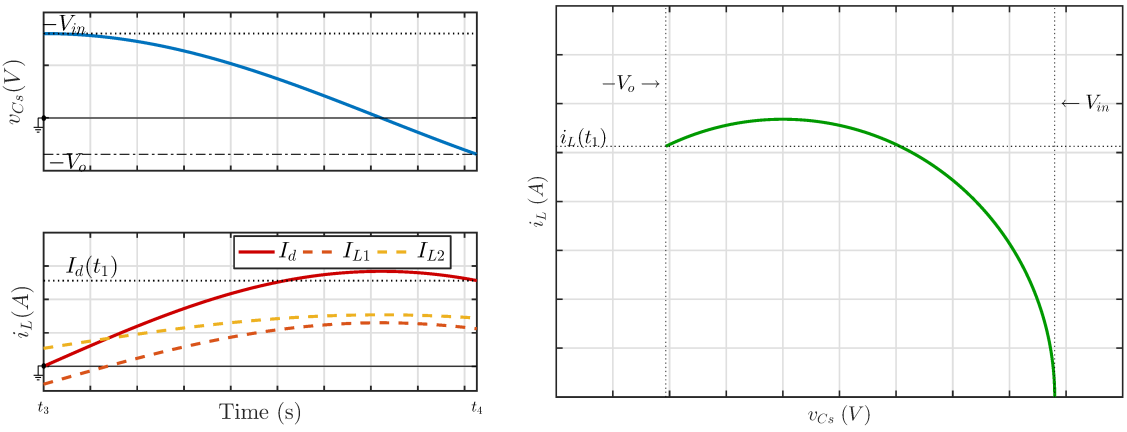
$$i_{L2}(t) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0). \tag{A.386}$$

Finally, the equivalent diode current $I_d(t)$ is given by

$$i_d(t) = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0). \tag{A.387}$$

The resulted waveforms described are shown in Figure 172.

Figure 172 – Zeta RSC: stage 4 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



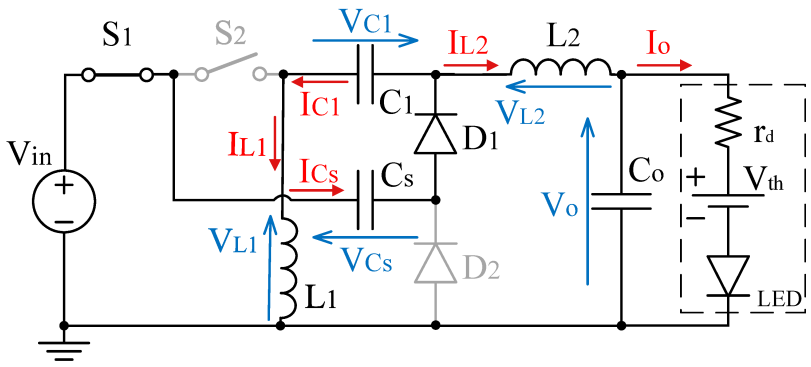
(a) (b)

Source: Author (2020).

With the capacitor reaching its minimum voltage, the diode D_1 begins conduction which stops the discharging process of the capacitor. Once again, remnant energy on the inductor forward bias both diodes creating a current flow in order to discharge it through the path shown in Figure 173.

$$\begin{cases} v_{Cs}(t_4) = V_{Cs\,min} = -V_o \\ i_{L_1}(t_4) = I_{L1\,(t4)} \\ i_{L_2}(t_4) = I_{L2\,(t4)}. \end{cases} \tag{A.388}$$

Figure 173 – Zeta RSC: stage 5.



Source: Author (2020).

For this stage, the description of the current and voltage at each semiconductor is displayed in Table 54.

Table 54 – Semiconductor Conditions for RSC Zeta: stage 5.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in} - v_{Cs}(t)$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Conducting	$v_{D1} = 0$	$i_{D1} = i_{L1}(t) + i_{L2}(t)$
D_2	Conducting	$v_{D2} = 0$	$i_{D2} = i_{L1}(t) + i_{L2}(t)$

Source: Author (2020).

The loop equations for this stage are described by (A.389) and (A.390).

Time Domain		Frequency Domain	
$L_1 \frac{d}{dt} i_{L1}(t) = -V_{C1}$	$\xrightarrow{\mathcal{L}}$	$L_1 \left(s\, I_L(s) - I_{L1(t0)}\right) = -\frac{V_{C1}}{s}$	(A.389)
$L_2 \frac{d}{dt} i_{L2}(t) = -V_o$	$\xrightarrow{\mathcal{L}}$	$L_2 \left(s\, I_{L2}(s) - I_{L2(t0)}\right) = -\frac{V_o}{s}$	(A.390)

During this stage the switched capacitor remains discharged, keeping its voltage constant as

$$v_{Cs}(t) = V_{Cs\,min}. \tag{A.391}$$

The inductor behavior can be solved separately once the states don't depend on each other. Using (A.389) and isolating the state $I_{L1}(s)$ yields

$$I_{L1}(s) = \frac{I_{L1(t1)}}{s} - \frac{V_o}{L_1\, s^2}. \tag{A.392}$$

Applying the inverse Laplace transform result in the time-domain behavior for the inductor current as

$$i_{L1}(t) = I_{L1(t4)} - \frac{V_o}{L_1}\, t. \tag{A.393}$$

Similarly, solving (A.390) for $I_{L2}(s)$ yields

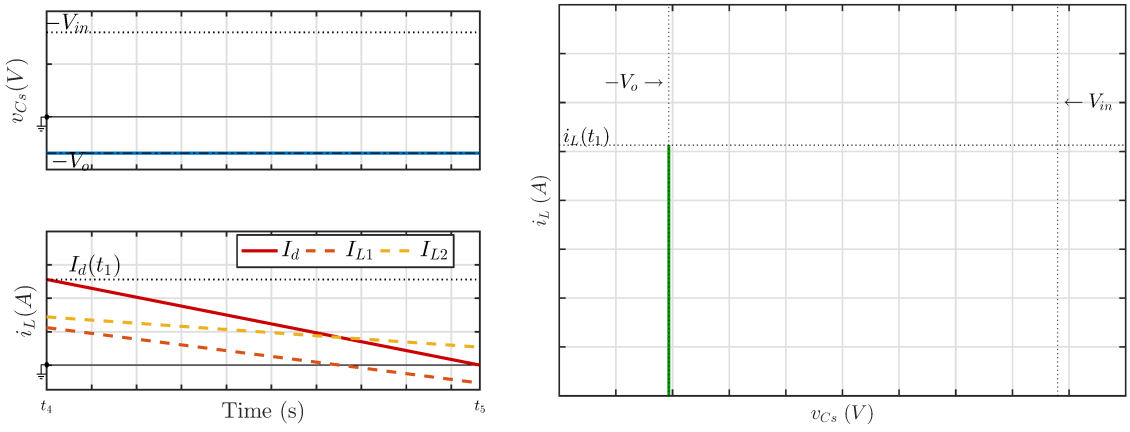
$$i_{L2}(t) = I_{L2(t4)} - \frac{V_o}{L_2}\, t. \tag{A.394}$$

Adding both equations gives the value of the equivalent diode current as

$$i_d(t) = I_{d(t4)} - \frac{V_o}{L_e}\, t. \tag{A.395}$$

The resulted waveforms described are shown in Figure 174.

Figure 174 – Zeta RSC: stage 5 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



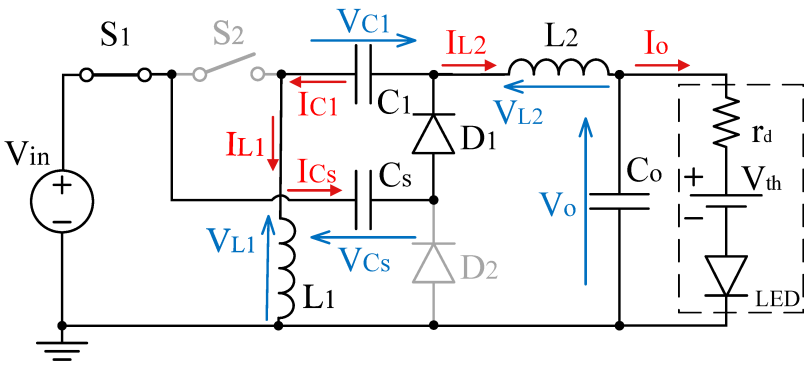
(a) (b)

Source: Author (2020).

Once again, this stage is characterized by a null current through the diodes as shown in Figure 175, caused by the inductor currents reaching a point of mutual cancellation. The initial conditions for this stage are given, henceforth, by

$$\begin{cases} v_{Cs}(t_5) = V_{Cs\,min} = -V_o \\ i_{L_1}(t_5) = I_{L\,DCM} \\ i_{L_2}(t_5) = -I_{L\,DCM} \end{cases} \tag{A.396}$$

Figure 175 – Zeta RSC: stage 6.



Source: Author (2020).

Table 55 highlights the behavior of each semiconductor during this stage.

Table 55 – Semiconductor Conditions for RSC Zeta: stage 6.

	State	Voltages	Currents
S_1	Blocking	$v_{S1} = V_{in}$	$i_{S1} = 0$
S_2	Conducting	$v_{S2} = 0$	$i_{S2} = 0$
D_1	Blocking	$v_{D1} = v_{Cs}(t) + V_{C1}$	$i_{D1} = 0$
D_2	Blocking	$v_{D2} = V_o - V_{C1} - v_{Cs}(t)$	$i_{D2} = 0$

Source: Author (2020).

During stage three both capacitor voltage and inductor currents are constant

$$v_{Cs}(t) = V_{Cs\,min} \tag{A.397}$$

$$i_{L1}(t) = I_{L\,DCM}\ ;\ i_{L2}(t) = -I_{L\,DCM}. \tag{A.398}$$

The equivalent current $i_d(t)$ is then given by

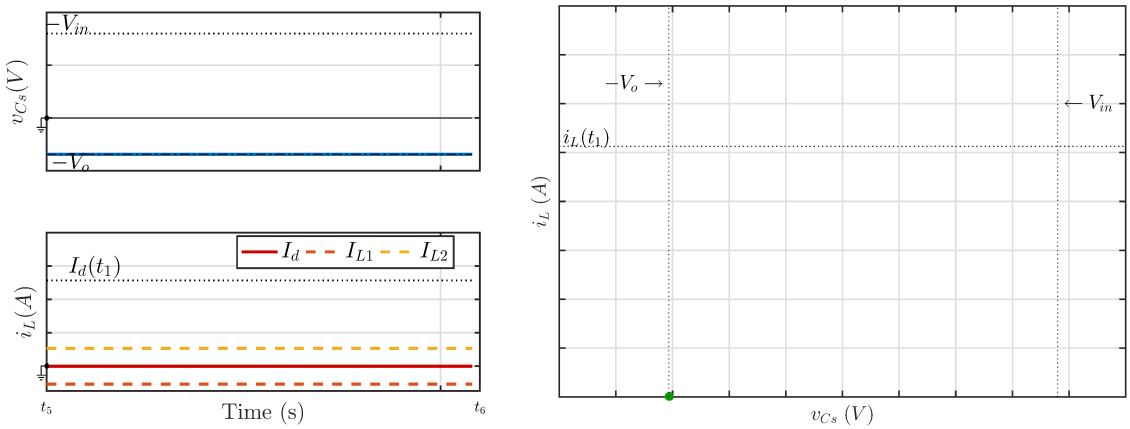
$$i_d(t) = 0. \tag{A.399}$$

The resulted waveforms described are shown in Figure 176.

A.6.4 Time Analysis

In order to fully characterize the behavior of the converter, the time of each state must be determined.

Figure 176 – Zeta RSC: stage 6 (a) waveforms for states v_{Cs} and i_L and (b) plane of states.



(a) (b)

Source: Author (2020).

A.6.4.1 Stages 1 and 4

Stage 1 is characterized by the charging of the switched capacitor, starting with its minimum voltage and ending with its maximum voltage. Using (A.355) it is known that

$$v_{Cs}(t_1) = V_{in}\left(1 - \cos(\Delta t_1\,\omega_0)\right) - V_o = V_{in}. \tag{A.400}$$

Isolating Δt_1 and considering the defines value of the voltage static gain as $G = {}^{V_o}/_{V_{in}}$ results in

$$\Delta t_1 = t_1 - t_0 = \frac{1}{\omega_0}\,acos\left(\frac{-V_o}{V_{in}}\right) = \frac{1}{\omega_0}\,acos\left(-G\right). \tag{A.401}$$

Applying the time duration for stage 1 into (A.357) it is possible to find the inductor current by the end of such stage which is one of the initial conditions for stage 2.

$$I_{L1\,t1} = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sin(t_1\,\omega_0) = I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\,\sqrt{1-G^2} \tag{A.402}$$

Similarly, the current at $t = t_1$ for L_2 is given by

$$I_{L2\,t1} = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t_1\,\omega_0) = -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sqrt{1-G^2} \tag{A.403}$$

And by adding both equations, the equivalent current $i_d(t)$ at the same instant is given by the sum of both inductor currents, given by

$$I_{d(t1)} = \frac{V_{in}}{L_e\,\omega_0}\,\sin(t_1\,\omega_0) = C_s\,\omega_0\,V_{in}\,\sqrt{1-G^2} \tag{A.404}$$

In order to ensure the DCM operation the voltage static gain must respect the constraint $1 - G^2 > 0$, which results in a design requirement given in (A.405).

$$G < 1 \tag{A.405}$$

A.6.4.2 Stages 2 and 5

The second stage is characterized by the discharge of the remnant energy on the inductors until no current is left to forward bias the diodes. For the higher-order converters this stage is reached not when a given inductor current reaches zero, but when the sum of the inductor currents does. From (A.367) and (A.404) it is known that

$$i_d(t_2) = I_{d(t1)} - \frac{V_o}{L_e}\,\Delta t_2 = \frac{V_{in}}{L_e\,\omega_0}\,\sqrt{1-G^2} - \frac{V_o}{L_e}\,\Delta t_2 = 0. \tag{A.406}$$

Isolating the time duration of the stage two, it can be found by

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_0\,G}\,\sqrt{1-G^2}. \tag{A.407}$$

A.6.4.3 Requirement for DCM

In order to ensure DCM operation, stage 2 must end before the half period of the switching frequency, granting the current to reach zero value. Thus, the following requirement

$$\Delta t_1 + \Delta t_2 < \frac{T_s}{2} \tag{A.408}$$

must be noted, which expands to

$$\frac{1}{\omega_0}\,acos\,(-G) + \frac{1}{\omega_0\,G}\,\sqrt{1-G^2} < \frac{1}{2\,f_s}. \tag{A.409}$$

Solving for the resonant frequency gives

$$\omega_0 > 2\,f_s\,\left(acos\,(-G) + \frac{1}{G}\,\sqrt{1-G^2}\right). \tag{A.410}$$

A.6.5 Average Equivalent Diode Current

The average inductor current is found by integrating the equivalent diode waveform over a switching cycle. Once the current repeats its exact behavior for half a cycle, the integration can also be performed in half of the switching period:

$$I_{Ld} = \frac{1}{T_s/2}\,\left(\int_{t_0}^{t_1}[i_{L1}(t)_1 + i_{L2}(t)_1]dt + \int_{t_1}^{t_2}[i_{L1}(t)_2 + i_{L2}(t)_2]dt\right) \tag{A.411}$$

$$I_{Ld} = 2\,f_s\,\left(\int_{t_0}^{t_1} C_s\,\omega_0\,V_{in}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{d(t1)} - \frac{V_o}{L_e}\,t\,dt\right). \tag{A.412}$$

Solving the equation above and making use of the relations given by (A.401), (A.404) and (A.407), the average output current can be simplified as (A.413):

$$I_d = C_s\,f_s\,V_{in}\,\frac{(G+1)^2}{G}. \tag{A.413}$$

A.6.6 DCM Current Offset

For the higher-order converters DCM operation does not imply on null current values for inductors during stage three. This characteristic is due to the capability of the inductors on storing energy such that the its opposite values of constant current can cancel each other and are therefore unable to keep the diodes forward biased.

In order to accurately characterize the current on the inductors, this constant current level of opposite values must be found, which requires an additional steady-state description of the system (ZHU; LUO; HE, 2008). This new description can be achieved through the charge balance of the input capacitor C_1 in high-frequency.

As stated, the capacitor C_1 is at first considered as a constant-voltage component which simplifies the calculations while still maintaining certain accuracy given a high capacitance value. Still, the voltage at the capacitor is directly affected by the charge count in each instant which is consequently an integration of the current waveform. Once the currents at the capacitor C_1 are not constant, it can be assumed a high-frequency voltage change in the capacitor related to the charge differences between stages. Yet, for a given switching period, it is expected that the initial and final changes of charge can cancel themselves in order to maintain constant voltage. This statement can be mathematically described as

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{C1}(t)_1 dt + \int_{t_1}^{t_2} i_{C1}(t)_2 dt + \int_{t_2}^{t_3} i_{C1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} i_{C1}(t)_4 dt + \int_{t_4}^{t_5} i_{C1}(t)_5 dt + \int_{t_5}^{t_6} i_{C1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.414}$$

During stage 4, the input capacitor current is the opposite to the current at inductor L_2 according to the assigned positive current flow for each component. For every other stage, the input capacitor current is the same as the current at inductor L_1 which van be translated to

$$\begin{aligned}\Delta Q_{total} = \frac{1}{T_s}\Bigg(&\int_{t_0}^{t_1} i_{L1}(t)_1 dt + \int_{t_1}^{t_2} i_{L1}(t)_2 dt + \int_{t_2}^{t_3} i_{L1}(t)_3 dt + \\ &+ \int_{t_3}^{t_4} -i_{L2}(t)_4 dt + \int_{t_4}^{t_5} i_{L1}(t)_5 dt + \int_{t_5}^{t_6} i_{L1}(t)_6 dt\Bigg) = 0.\end{aligned} \tag{A.415}$$

Replacing the inductor waveforms on the equation above yields

$$\begin{aligned}\int_{t_0}^{t_1} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sin(t\,\omega_0)dt + &\int_{t_1}^{t_2} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_2}^{t_3} I_{L\,DCM} dt + \int_{t_3}^{t_4} -\left(-I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\sin(t\,\omega_0)\right) dt + \\ &+ \int_{t_4}^{t_5} I_{L\,DCM} + \frac{V_{in}}{L_1\,\omega_0}\sqrt{1-G^2} - \frac{V_o}{L_1}\,t dt + \\ &+ \int_{t_5}^{t_6} I_{L\,DCM} dt = 0.\end{aligned} \tag{A.416}$$

Solving the equation for $I_{L\,DCM}$ and using the time steps defined in the previous section, results in

$$I_{L\,DCM} = C_s\,V_{in}\,f_s\,\frac{G+1}{G}\,\frac{G\,L_1 - L_2}{L_1 + L_2}, \tag{A.417}$$

which can also be written as

$$I_{L\,DCM} = \frac{I_d}{G+1}\,\frac{G\,L_1 - L_2}{L_1 + L_2}. \tag{A.418}$$

A.6.7 Average Output Current

For the Ćuk converter, the output current is the current at inductor L_2. Once the inductor current repeats itself after the first switching period, the integration can be made over only half a witching period as

$$I_o = \frac{1}{T_s/2}\left(\int_{t_0}^{t_1} i_{L2}(t)_1 dt + \int_{t_1}^{t_2} i_{L2}(t)_2 dt + \int_{t_2}^{t_3} i_{L2}(t)_3 dt\right) \tag{A.419}$$

$$I_o = 2\,f_s\left(\int_{t_0}^{t_1} -I_{L\,DCM} + \frac{V_{in}}{L_2\,\omega_0}\,\sin(t\,\omega_0)\,dt + \int_{t_1}^{t_2} I_{L2(t1)} - \frac{V_o}{L_2}\,t\,dt + \int_{t_2}^{t_3} -I_{L\,DCM}\,dt\right). \tag{A.420}$$

Solving the equation above and making use of the relations given by (A.401) (A.403) and (A.407), the average output current can be simplified as (A.421):

$$I_o = C_s\,V_{in}\,f_s\,\frac{G+1}{G}. \tag{A.421}$$

Which can also be written as

$$I_o = \frac{I_d}{G+1}. \tag{A.422}$$

A.6.8 Output Power

Using the output current equation, the output power can be found by

$$P_o = I_o\,V_o = C_s\,f_s\,V_{in}\,\frac{G+1}{G}\,V_o. \tag{A.423}$$

Using the static gain definition stated as $V_o = G\,V_{in}$ the output power is given by

$$P_o = C_s\,f_s\,V_{in}^2\,(G+1). \tag{A.424}$$

The capacitor must be sized accordingly to the output power, relation given by (A.425):

$$C_s = \frac{P_o}{f_s\,V_{in}^2\,(G+1)}. \tag{A.425}$$

A.6.9 Theoretical Waveforms and Simulated Results

In order to verify the theoretical analysis a simulation can be made, comparing its result with the theoretical waveform. The load and converter values used in the simulation are highlighted in Table 56.

Table 56 – RSC Zeta simulation values for (a) load and (b) converter.

LED Load		
Dynamic Resistance	r_d	$6.16\,\Omega$
Threshold Voltage	V_t	$17.24\,V$
Nominal Current	I_s	$0.5\,A$
Output Power	P_L	$10\,W$

(a)

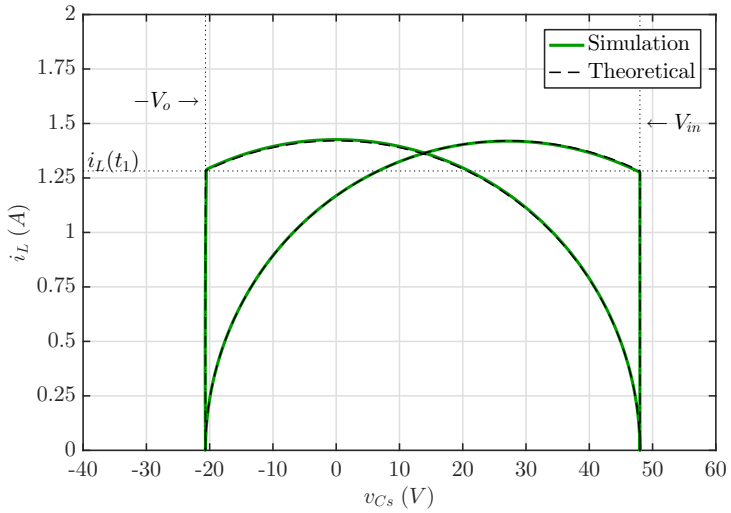
Source and Converter values		
Input Voltage	V_{in}	$48\,V$
Output Voltage	V_o	$20.662\,V$
Switching Frequency	f_s	$500\,kHz$
Input Capacitance	C_1	$470\,nF$
Output Capacitance	C_o	$68\,nF$
Switched Capacitance	C_s	$6.8\,nF$
Input Inductance	L_1	$12\,\mu H$
Output Inductance	L_2	$22\,\mu H$

(b)

Source: Author (2020).

The evaluation of the state plane shown in Figure 177 yields a precise comparison between theoretical prediction and simulation result, with the stages occurring as expected.

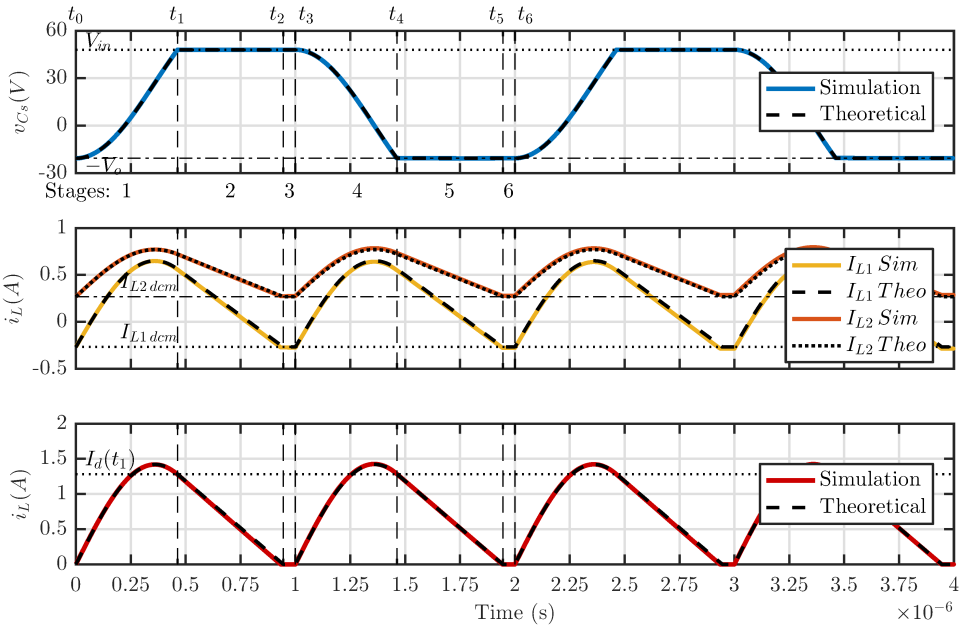
Figure 177 – State Plan for the RSC Zeta converter.



Source: Author (2020).

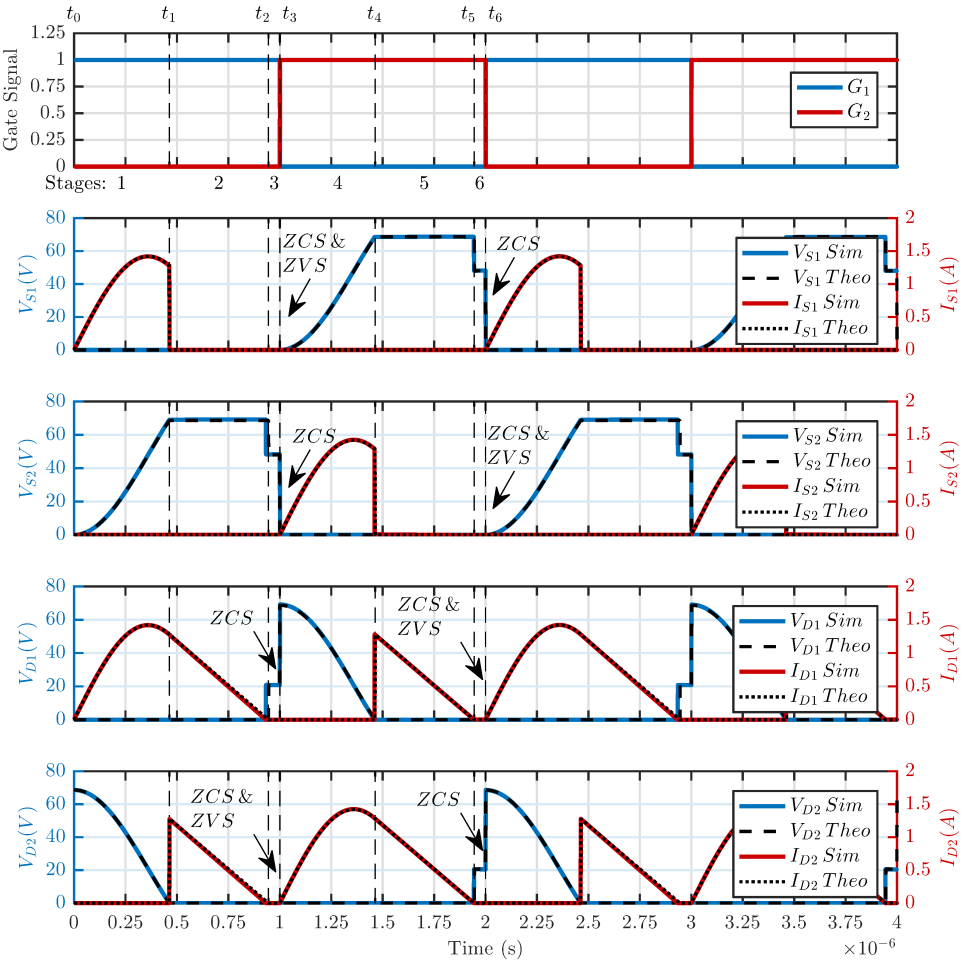
Thus, the waveform comparison of the RSC Zeta converter states for each stage in their respective timespans is shown in Figure 178, following prediction without noticeable differences. Finally, Figure 179 displays the voltage and current waveforms in each semiconductor switch, with highlighted soft-switching. As can be seen, each semiconductor operates in both ZCS and ZVS in half the switching points, while still presenting ZCS on the remaining switching instants due to the DCM operation.

Figure 178 – Theoretical waveforms of the state variables for the RSC Zeta converter.



Source: Author (2020).

Figure 179 – Soft-switching on the semiconductors for the RSC Zeta converter.



Source: Author (2020).

APPENDIX B – TIVA CODE

Listing B.1 – TIVA code for VPPM data moduling.

```
/* ---------------------------------------------------------------------- */
// Includes
/* ---------------------------------------------------------------------- */
#include <stdint.h>
#include <stdbool.h>

#include "inc/hw_ints.h"
#include "inc/hw_memmap.h"
#include "inc/hw_gpio.h"
#include "driverlib/debug.h"
#include "driverlib/fpu.h"
#include "driverlib/gpio.h"
#include "driverlib/interrupt.h"
#include "driverlib/pin_map.h"
#include "driverlib/sysctl.h"
#include "driverlib/pwm.h"
#include "driverlib/uart.h"
#include "utils/uartstdio.h"
#include "utils/ustdlib.h"
#include "inc/hw_types.h"
#include "driverlib/timer.h"

/* ---------------------------------------------------------------------- */
// Defines
/* ---------------------------------------------------------------------- */
#define MOGEN0_FREQ   500000   //Freq (Hz) Module 0 Gen 0
#define MOPWM0_DUTY   0.50f     //Duty (pu) Module 0 Gen 0 MOPWM0
#define DT_R          1         //Dead-time in clk tcks, rise
#define DT_F          1         //idem, fall
#define CLKTCK        12.5f     //Clock period, system, ns

#define FMIN          10000      //Min freq, Hz
#define FMAX          40000000   //Max freq, Hz
#define DMIN          0.05f     //Min d, pu
#define DMAX          0.95f     //Max d, pu

#define DATA_SIZE     512

```

```
39
40 /* ---------------------------------------------------------------------- */
41 // Variables definition
42 /* ---------------------------------------------------------------------- */
43 void ClearUART(uint32_t ui32Base);
44 float DUTY = M0PWM0_DUTY;
45 uint32_t FREQ = M0GEN0_FREQ;
46
47 int32_t aux=0;                                  //Auxiliary variable
48 uint32_t i=0, it=0, it2=0, ii=0, setD=0, setM=0, setT=0; //Index variables
49 int32_t UART[4];                            //Uart buffer
50 //Time variables, in clock ticks:
51 uint32_t M0GEN0_PERIOD; //Period, M0 Gen 0
52 uint32_t M0PWM0_PWIDTH; //Pulse width M0PWM0
53 uint32_t DT;          //Deadtime
54 // Timer Variables for PWM Data Modulation
55 uint32_t TIMER0_PERIOD, TIMER0_FREQ; //Period and Freq, Timer 0
56 int32_t DATA_MOD=1;           // Data Signal Modulation
57 int32_t DATA_SIZE_RECEIVED;
58 char DATA_VPPM[DATA_SIZE];
59 int32_t RECEIVED_FLAG=0,DATA_POS=0, STOP_FLAG=0, LOOP=0, DATA_i;
60 int32_t M = 5; // M = 5 -> fdata = 100kbps || M = 10 -> fdata = 50kbps
61 float VLC_DIM = 0.20; // Dim due to VPPM modulation
62 // Variables for Dimming Calculations
63 int32_t S_PERIOD_NS, D_PERIOD_NS; // Switching and Data periods in ns
64 int32_t T_DIM_NORM, T_DIM_COMP;
65 float N_CYC_TOT;
66 int N_CYC_0, N_CYC_1, CYC_i=0, FIRST_PWM=1;
67
68 /* ---------------------------------------------------------------------- */
69 // The error routine that is called if the driver library encounters an error.
70 /* ---------------------------------------------------------------------- */
71 #ifdef DEBUG
72 void
73 __error__(char *pcFilename, uint32_t ui32Line)
74 {
75 }
76 #endif
77 extern void UARTStdioInit(unsigned long ulPortNum);
78 void GPIOFIntHandler(void);
79 void TIMER0AIntHandler(void);
80 void PWM0Gen0IntHandler(void);
```

```
81
82  int main(void) {
83     /* ---------------------------------------------------------------- */
84      // MCU settings
85     /* ---------------------------------------------------------------- */
86      //Enable System clock at 80 Mhz with a PLL, with crystal 16Mhz
87     //(PLL = 200 MHz, Clock = PLL/div)
88      SysCtlClockSet(SYSCTL_SYSDIV_2_5 | SYSCTL_USE_PLL | SYSCTL_XTAL_16MHZ |
            SYSCTL_OSC_MAIN);
89
90     /* ---------------------------------------------------------------- */
91      // Enable FPU
92      FPUEnable();
93      // Configure FPU
94      FPULazyStackingEnable();
95      //FPUStackingEnable();
96      //FPUHalfPrecisionModeSet(FPU_HALF_IEEE);
97     /* ---------------------------------------------------------------- */
98      // Enable CPU interrupts
99      IntMasterEnable();
100
101    /* ---------------------------------------------------------------- */
102     // Variables definition
103    /* ---------------------------------------------------------------- */
104     //Time variables, first calculation, in clock ticks:
105     MOGEN0_PERIOD = (SysCtlClockGet()/MOGEN0_FREQ); //Period, M0 Gen 0
106     MOGEN0_PERIOD = MOGEN0_PERIOD-0;
107     M0PWM0_PWIDTH = MOGEN0_PERIOD*M0PWM0_DUTY; //Pulse width M0PWM0
108     //Time Variables for TIMER
109     TIMER0_PERIOD = MOGEN0_PERIOD*M;
110     TIMER0_FREQ  = MOGEN0_FREQ/(M);
111
112     S_PERIOD_NS = 1000000000*(float)MOGEN0_PERIOD/SysCtlClockGet();
113     D_PERIOD_NS = 1000000000*(float)TIMER0_PERIOD/SysCtlClockGet();
114
115    //Calculation of tonn and toff (ticks)
116     T_DIM_NORM = (VLC_DIM)*TIMER0_PERIOD - MOGEN0_PERIOD*0.5;
117     T_DIM_COMP = (1-VLC_DIM)*TIMER0_PERIOD - MOGEN0_PERIOD*0.5;
118    //Number of high-freq periods during onn and off times
119     N_CYC_TOT = TIMER0_PERIOD/MOGEN0_PERIOD;
120     N_CYC_0 = N_CYC_TOT*VLC_DIM + 0.5; //Number of HF periods when sending 0
121     N_CYC_1 = N_CYC_TOT*VLC_DIM; //Number of HF periods when sending 1
```

```
122
123   /* ------------------------------------------------------------ */
124    //PWM Module 0 Gen 0 Configure - M0PWM0 @ PB6 & PB7
125   /* ------------------------------------------------------------ */
126     SysCtlPWMClockSet(SYSCTL_PWMDIV_1); //Clock PWM = 80 MHz, div = 1
127     SysCtlPeripheralEnable(SYSCTL_PERIPH_PWM0); //Enable PWM Module 0
128     SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB); //Enable GPIO B
129
130    // PWM Config
131     PWMGenConfigure(PWM0_BASE,PWM_GEN_0,PWM_GEN_MODE_UP_DOWN |
           PWM_GEN_MODE_NO_SYNC); //Gen 0 = Up/Down, No Sync
132     PWMGenPeriodSet(PWM0_BASE,PWM_GEN_0,M0GEN0_PERIOD); //Gen 0
           frequency/period set
133     PWMDeadBandEnable(PWM0_BASE,PWM_GEN_0,DT_R,DT_F); //Config dead-band
           (rise, fall) on Module 0 Gen 0
134     PWMOutputInvert(PWM0_BASE,PWM_OUT_0_BIT | PWM_OUT_1_BIT,true); //Enable
           active-low mode
135     PWMOutputState(PWM0_BASE,PWM_OUT_0_BIT | PWM_OUT_1_BIT,true); //Enable
           M0PWM0 & M0PWM1 bits
136
137    // GPIO Config
138     GPIOPinConfigure(GPIO_PB6_M0PWM0); //Map Port B Pin 6 to M0PWM0
139     GPIOPinConfigure(GPIO_PB7_M0PWM1); //Map Port B Pin 7 to M0PWM1
140     GPIOPinTypePWM(GPIO_PORTB_BASE,GPIO_PIN_6 | GPIO_PIN_7); //Set PB6 & PB7
           as PWM
141     GPIOPadConfigSet(GPIO_PORTB_BASE,GPIO_PIN_6 |
           GPIO_PIN_7,GPIO_STRENGTH_2MA,GPIO_PIN_TYPE_STD); //Set PB6 Pad as
           push-pull
142
143    // PWM Enable
144     PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,M0PWM0_PWIDTH); //M0PWM0 duty set
145     PWMGenEnable(PWM0_BASE,PWM_GEN_0); //Enable Module 0 Gen 0
146
147    //GPIO Enable
148     GPIOPinTypeGPIOOutput(GPIO_PORTB_BASE, GPIO_PIN_3); //Config PB3 as outupt
149     GPIOPinTypeGPIOOutput(GPIO_PORTB_BASE, GPIO_PIN_2); //Config PB2 as outupt
150     GPIOPadConfigSet(GPIO_PORTB_BASE, GPIO_PIN_2, GPIO_STRENGTH_8MA,
           GPIO_PIN_TYPE_STD_WPD);
151     GPIOPadConfigSet(GPIO_PORTB_BASE, GPIO_PIN_3, GPIO_STRENGTH_8MA,
           GPIO_PIN_TYPE_STD_WPD);
152
153
```

```
154   /* ------------------------------------------------------------------ */
155     //GPIOF Configure, w/ RLED @ PF1, BLED @ PF2, GLED @ PF3, SW1 @ PF4
156   /* ------------------------------------------------------------------ */
157     SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOF); //Enable GPIO F
158     GPIOPinTypeGPIOOutput(GPIO_PORTF_BASE, GPIO_PIN_1 | GPIO_PIN_2); //Config
          PF1 & PF2 as output (PF1 = RLED, PF2 = BLED)
159     GPIOPinTypeGPIOInput(GPIO_PORTF_BASE, GPIO_PIN_4); //Config PF4 as input
          (PF4 = SW1)
160     GPIOPadConfigSet(GPIO_PORTF_BASE, GPIO_PIN_4, GPIO_STRENGTH_2MA,
          GPIO_PIN_TYPE_STD_WPU); //Config pad as weak pull up
161     IntEnable(INT_GPIOF); //Enable GPIOF interrupts
162     GPIOIntEnable(GPIO_PORTF_BASE, GPIO_INT_PIN_4); //Config interrupt @ PF4
163     GPIOIntTypeSet(GPIO_PORTF_BASE, GPIO_PIN_4, GPIO_FALLING_EDGE); //Config
          as falling-edge detection
164     GPIOIntRegister(GPIO_PORTF_BASE, GPIOFIntHandler); //
165
166     GPIOPinTypeGPIOOutput(GPIO_PORTF_BASE, GPIO_PIN_3);
167     GPIOPadConfigSet(GPIO_PORTF_BASE, GPIO_PIN_3, GPIO_STRENGTH_8MA,
          GPIO_PIN_TYPE_STD_WPD);
168
169   /* ------------------------------------------------------------------ */
170     //UART0 Configure
171   /* ------------------------------------------------------------------ */
172     SysCtlPeripheralEnable(SYSCTL_PERIPH_UART0); //Enable UART0
173     SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA); //Enable GPIO A (U0TX = PA0;
          U0RX = PA1)
174
175     GPIOPinConfigure(GPIO_PA0_U0RX); //Map Port A Pin 0 to UART0 - RX
176     GPIOPinConfigure(GPIO_PA1_U0TX); //Map Port A Pin 1 to UART0 - TX
177     GPIOPinTypeUART(GPIO_PORTA_BASE, GPIO_PIN_0 | GPIO_PIN_1); //Set PA0 &
          PA1 as UART
178
179     // UART 0: 115200 bauds, 80 MHz clock, 8 bits (word length), 1 stop bit,
          no parity
180     UARTConfigSetExpClk(UART0_BASE,SysCtlClockGet(),115200,(UART_CONFIG_WLEN_8
          | UART_CONFIG_STOP_ONE | UART_CONFIG_PAR_NONE));
181     IntEnable(INT_UART0); //Enable UART0 interrupts
182     UARTIntEnable(UART0_BASE, UART_INT_RX | UART_INT_RT); //Config interrupts
          from UART0 at RX and TX
183
184     UARTStdioInit(0);     //tem q adicionar o uartstdio.c igual ao q tem aqui
          no arquivo (velocidade certa)
```

```
185
186   /* ---------------------------------------------------------------- */
187     //TIMER Module Interrupt Config
188   /* ---------------------------------------------------------------- */
189     SysCtlPeripheralEnable(SYSCTL_PERIPH_TIMER0);
190     TimerConfigure(TIMER0_BASE, TIMER_CFG_PERIODIC); // Config Timer
191     TimerIntEnable(TIMER0_BASE, TIMER_TIMA_TIMEOUT);  // Config Int Timer
        (TIMEOUT)
192     TimerIntRegister(TIMER0_BASE, TIMER_A, TIMER0AIntHandler);
193     IntEnable(INT_TIMER0A);                // Enable Int Timer
194     TimerLoadSet(TIMER0_BASE, TIMER_A, TIMER0_PERIOD); // Sets Interrupt LOAD
195     TimerEnable(TIMER0_BASE, TIMER_A);          // Enables Interrupt Timer
196
197   /* ---------------------------------------------------------------- */
198     //PWM Pulse Counter: Config PWM Interruption
199   /* ---------------------------------------------------------------- */
200     PWMGenIntRegister(PWM0_BASE, PWM_GEN_0, PWM0Gen0IntHandler);
201     PWMIntEnable(PWM0_BASE, PWM_INT_GEN_0); // Configs PWM Interrupt
202     IntEnable(INT_PWM0_0);              // Enables PWM Interrupt
203     PWMGenIntTrigEnable(PWM0_BASE, PWM_GEN_0, PWM_INT_CNT_LOAD);
204
205   /* ---------------------------------------------------------------- */
206     // INITIALIZATION OF PROGRAM
207   /* ---------------------------------------------------------------- */
208     GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_1, 0xff); //Turn on the LED
209     SysCtlDelay((10000000/CLKTCK)/3);        //Delay, in ns
210     GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_1, 0x00); //Turn off the LED
211
212     ClearUART(UART0_BASE);
213     while (1)   // Infinite Loop
214    {
215     }
216 }
217 /* ---------------------------------------------------------------- */
218 // Functions and interrupt handlers
219 /* ---------------------------------------------------------------- */
220 // Clear UART Function
221 void ClearUART(uint32_t ui32Base) {
222    while(UARTCharsAvail(ui32Base)) {
223        UARTCharGet(ui32Base);
224    }
225 }
```

```
226
227 // TIMER Interrupt Handler
228 void TIMER0AIntHandler(void) {
229    TimerIntClear(TIMER0_BASE, TIMER_TIMA_TIMEOUT); // Clears Int
230
231    if (DATA_POS==0) { // Enable PWM Output at first iteraction (DATA_POS=0)
232       PWMOutputState(PWM0_BASE,PWM_OUT_0_BIT,1);
233       PWMOutputState(PWM0_BASE,PWM_OUT_1_BIT,1);
234    }
235
236    DATA_i = DATA_VPPM[DATA_POS]; // Stores next bit to transmit
237    if (DATA_i == 0) { // @ bit 0, VPPM initiates in high state (d_PWM = .5)
238       PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,M0PWM0_PWIDTH);
239       GPIOPinWrite(GPIO_PORTB_BASE,GPIO_PIN_3,0x00);
240       DATA_MOD = 1;
241       CYC_i = 0; // resets PWM cycle counter
242
243       GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0xFF);
244    }
245    else if (DATA_i == 1) { // @ bit 1, VPPM initiates in low state (d_PWM = 0)
246       PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,0);
247       GPIOPinWrite(GPIO_PORTB_BASE,GPIO_PIN_3,0xFF);
248       DATA_MOD = 0;
249       CYC_i = 0; // resets PWM cycle counter
250
251       GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0x00);
252    }
253    DATA_POS++;
254    if (DATA_POS == DATA_SIZE) { // End of Package
255       DATA_POS = 0; STOP_FLAG=1; DATA_MOD=0;
256       GPIOPinWrite(GPIO_PORTB_BASE,GPIO_PIN_3,0x00);
257       GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0x00);
258       if (LOOP==0) { // Disables PWM outputs and interrupts
259          PWMOutputState(PWM0_BASE,PWM_OUT_0_BIT,0);
260          PWMOutputState(PWM0_BASE,PWM_OUT_1_BIT,0);
261          PWMIntDisable(PWM0_BASE, PWM_INT_GEN_0);
262          TimerIntDisable(TIMER0_BASE, TIMER_TIMA_TIMEOUT);
263       }
264    }
265    FIRST_PWM=1; // Flags first PWM of data period
266 }
267
```

```
268 // PWM Interrupt Handler
269 void PWM0Gen0IntHandler(void)
270 {
271     PWMGenIntClear(PWM0_BASE, PWM_GEN_0, PWM_INT_CNT_LOAD); // Clears Int
272
273     if (FIRST_PWM==1)
274     { // Outputs a pulse at first PWM cycle (for oscilloscope triggering)
275         FIRST_PWM=0;
276         GPIOPinWrite(GPIO_PORTB_BASE,GPIO_PIN_2,0xFF);
277         GPIOPinWrite(GPIO_PORTB_BASE,GPIO_PIN_2,0x00);
278     }
279
280     CYC_i++;  // High-frequency PWM cycles counter
281    // Counts the number of cycles the output must remain enabled.
282     if (DATA_MOD == 1 ) {
283         if (DATA_i == 0 && CYC_i == N_CYC_0) {
284             PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,0);
285             DATA_MOD = 0;
286             CYC_i = 0;
287             GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0x00);
288         }
289         else if (DATA_i == 1 && CYC_i == N_CYC_1) {
290             PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,0);
291             DATA_MOD = 0;
292             CYC_i = 0;
293             GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0x00);
294         }
295     }
296    // Counts the number of cycles the output must remain disabled.
297     if (DATA_MOD == 0 && CYC_i > 0) {
298         if (DATA_i == 1 && CYC_i == (M - N_CYC_1)) {
299             PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,M0PWM0_PWIDTH);
300             DATA_MOD = 1;
301             CYC_i = 0;
302             GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0xFF);
303         }
304     }
305    //N_CYC_0 is the ammount of high-frequency cycles the PWM will be ON while
       sending the bit '0' at the beggining of the data period.
306    //N_CYC_1 is the ammount of high-frequency cycles the PWM will be ON while
       sending the bit '1' at the end of the data period.
307 }
```

```
308
309 // GPIO Interrupt Handler
310 void GPIOFIntHandler(void)
311 {
312     uint32_t ui32Status;
313     uint32_t pinRead=0xff;
314
315     ui32Status = GPIOIntStatus(GPIO_PORTF_BASE, true); //Get interrupt status
316     GPIOIntClear(GPIO_PORTF_BASE, ui32Status); //Clear the asserted interrupt
317
318     if((ui32Status & GPIO_INT_PIN_4) == GPIO_INT_PIN_4) //Check if there was
            indeed button press @ PF4
319     {
320         pinRead = GPIOPinRead(GPIO_PORTF_BASE, GPIO_PIN_4); //Read pin value
321         if(pinRead == 0) //Check if button was pressed and unbounced
322         {
323             GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_2, 0xff); //Turn on the BLED
324
325             // Reset initial values for fs and D:
326             MOGEN0_PERIOD = (SysCtlClockGet()/MOGEN0_FREQ);
327             MOPWM0_PWIDTH = MOGEN0_PERIOD*MOPWM0_DUTY;
328
329             PWMGenPeriodSet(PWM0_BASE,PWM_GEN_0,MOGEN0_PERIOD); //Gen 0
                frequency/period set
330             PWMPulseWidthSet(PWM0_BASE,PWM_OUT_0,MOPWM0_PWIDTH); //MOPWM0 duty
                set
331             PWMDeadBandEnable(PWM0_BASE,PWM_GEN_0,0,0); //Config dead-band
                (rise, fall) on Module 0 Gen 0
332
333             UARTprintf("Programa reinicializado com fs = 500 kHz, D = 0.5, sem
                dead-time\n\r"); //Initialization message
334
335             GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_2, 0x00); //Turn off the BLED
336         }
337         SysCtlDelay((5000000/CLKTCK)/3); //Delay, in ns - DEBOUNCE
338     }
339 }
340
341
342
343
344
```

```
345
346 // UART Interrupt Handler
347 void UART0IntHandler(void) {
348     uint32_t ui32Status;
349     ui32Status = UARTIntStatus(UART0_BASE, true); //Get the interrupt status
350     UARTIntClear(UART0_BASE, ui32Status); //Clear the asserted interrupt
351     char var=0;
352
353     //Loop while there are characters in the receive FIFO
354     while(UARTCharsAvail(UART0_BASE) && DATA_SIZE_RECEIVED==0) {
355         GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_1, 0xff); //Turn on the RLED to
              show a character transfer is occuring
356         if (!aux) { // Detects code received
357             aux = UARTCharGet(UART0_BASE);
358         }
359         switch (aux) {
360         case 'Z': // Clears DATA_VPPM by replacing all cells with zeros
361             UARTCharGet(UART0_BASE);
362             it=0;
363             while(1) {
364                 if(it==DATA_SIZE) {
365                     break;
366                 }
367                 else {
368                     DATA_VPPM[it++] = '0';
369                 }
370             }
371             break;
372         case 'T': // Detects information package to be received
373             DATA_SIZE_RECEIVED=1;
374             STOP_FLAG=0;
375             PWMIntEnable(PWM0_BASE, PWM_INT_GEN_0); // Enable interrupts
376             TimerIntEnable(TIMER0_BASE, TIMER_TIMA_TIMEOUT);
377             break;
378         case 'M': // Receiving Multiplying factor in the format M000
379             for (i = 0; i < 3; ++i) {
380                 UART[i] = UARTCharGetNonBlocking(UART0_BASE);
381             }
382             M = ((UART[0] - '0')*100 + (UART[1] - '0')*10 + (UART[2] - '0'));
383             UART[2] = UART[1] = UART[0] = 0; // clears vars
384             aux = 0; i = 0; setM = 1;
385             break;
```

```
386         case 'D': { //Receiving duty cycle in the format D000, 000 is duty in
                % (00,0%)
387             for (i = 0; i < 3; ++i) {
388                 UART[i] = UARTCharGetNonBlocking(UART0_BASE);
389             }
390             VLC_DIM = ((UART[0] - '0')*100 + (UART[1] - '0')*10 + (UART[2] -
                    '0'))*0.001f; //Duty cycle conversion from % to absolute
391             if (VLC_DIM > DMAX)
392                 VLC_DIM = DMAX;
393             if (VLC_DIM < DMIN)
394                 VLC_DIM = DMIN;
395             UART[2] = UART[1] = UART[0] = 0; // clears vars
396             aux = 0; i = 0; setD = 1;
397             break;
398         }
399         }
400     }
401
402     // If 'T' was received, this condition reads the data to follow:
403     if (DATA_SIZE_RECEIVED==1) {
404         it=0;
405         it2=0;
406         DATA_SIZE_RECEIVED=0;
407         RECEIVED_FLAG = 0;
408         UARTCharGet(UART0_BASE);
409         while(1) { //Adds bit to DATA_VOOM until stop symbol is found ('s' or
                'S')
410             var = UARTCharGet(UART0_BASE);
411             UARTCharGet(UART0_BASE);
412             if(var=='S') { //hard-stop (stops transmission)
413                 LOOP=0;
414                 break;
415             }
416             else if (var=='s') { //soft-stop (loops transmission)
417                 LOOP=1;
418                 break;
419             }
420             else {
421                 DATA_VPPM[it++] = var-'0';
422             }
423         }
424     }
```

```
425     if (setM & setD) { //Only set M and D if both are required to change
426             //Time Variables for TIMER
427             TIMER0_PERIOD = MOGEN0_PERIOD*M;
428             TIMER0_FREQ  = MOGEN0_FREQ/(M);
429 
430             S_PERIOD_NS = 1000000000*(float)MOGEN0_PERIOD/SysCtlClockGet();
431             D_PERIOD_NS = 1000000000*(float)TIMER0_PERIOD/SysCtlClockGet();
432 
433             T_DIM_NORM = (VLC_DIM)*TIMER0_PERIOD - MOGEN0_PERIOD*0.5;
434             T_DIM_COMP = (1-VLC_DIM)*TIMER0_PERIOD - MOGEN0_PERIOD*0.5;
435 
436             N_CYC_TOT = TIMER0_PERIOD/MOGEN0_PERIOD;
437             N_CYC_0 = N_CYC_TOT*VLC_DIM + 0.5;
438             N_CYC_1 = N_CYC_TOT*VLC_DIM;
439 
440             TimerLoadSet(TIMER0_BASE, TIMER_A, TIMER0_PERIOD);
441             TimerEnable(TIMER0_BASE, TIMER_A);
442 
443             setM = setD = 0;
444             GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0xFF);
445             GPIOPinWrite(GPIO_PORTF_BASE,GPIO_PIN_3,0x00);
446         }
447     DATA_POS = 0; it=0; i=0; ii=0; aux = 0;
448     DATA_SIZE_RECEIVED=0;
449     GPIOPinWrite(GPIO_PORTF_BASE, GPIO_PIN_1, 0x00); //Turn off the RLED
450 }
```