Universidade Federal de Juiz de Fora
Programa de Pós-Graduação em
Engenharia Elétrica

Ruan Moreira Ferraz

ALTERNATIVES FOR HIGH PERFORMANCE LED DRIVING IN OFF-LINE APPLICATIONS

Tese de Doutorado

Juiz de Fora
2023

Ruan Moreira Ferraz

Alternatives for High Performance LED Driving in Off-line Applications

Thesis submitted to the Graduate Program in Electrical Engineering of the Federal University of Juiz de Fora as a partial requirement for obtaining a Doctor's degree in Electrical Engineering. Concentration area: Electronic Systems

Supervisor: Prof. Guilherme Márcio Soares, Dr. Eng.

Juiz de Fora
2023

Ficha catalográfica elaborada através do programa de geração
automática da Biblioteca Universitária da UFJF,
com os dados fornecidos pelo(a) autor(a)

Ferraz, Ruan Moreira .
Alternatives for High Performance LED Driving in Off-line Applications / Ruan Moreira Ferraz. -- 2023.
209 f. : il.

Orientador: Guilherme Márcio Soares
Tese (doutorado) - Universidade Federal de Juiz de Fora, Faculdade de Engenharia. Programa de Pós-Graduação em Engenharia Elétrica, 2023.

1. Off-line light-emitting diode (LED) drivers. 2. Active ripple compensation. 3. Capacitance reduction. 4. Multi-objective optimization. I. Soares, Guilherme Márcio, orient. II. Título.

FEDERAL UNIVERSITY OF JUIZ DE FORA

RESEARCH AND GRADUATE PROGRAMS OFFICE

Ruan Moreira Ferraz

Alternatives for High Performance LED Driving in Off-line Applications

Thesis submitted to the Graduate Program in Electrical Engineering
of the Federal University of Juiz de Fora as a partial requirement for obtaining
a Doctor's degree in Electrical Engineering. Concentration area: Electronic Systems

Approved on 18 of December of 2023.

EXAMINING BOARD

Prof. Dr. Guilherme Márcio Soares – Academic Advisor
Federal University of Juiz de Fora

Prof. Dr. Álysson Raniere Seidel
Federal University of Santa Maria

Prof. Dr. Edilson Mineiro Sá Junior
Federal Institute of Education, Science and Technology of Ceará

Prof. Dr. Janaína Gonçalves de Oliveira
Federal University of Juiz de Fora

Prof. Dr. Pedro Santos Almeida
Federal University of Juiz de Fora

Juiz de Fora, 12/18/2023.

Documento assinado eletronicamente por **Álysson Raniere Seidel**, **Usuário Externo**, em 18/12/2023, às 11:58, conforme horário oficial de Brasília, com fundamento no § 3º do art. 4º do Decreto nº 10.543, de 13 de novembro de 2020.

Documento assinado eletronicamente por **Guilherme Márcio Soares**, **Professor(a)**, em 18/12/2023, às 12:42, conforme horário oficial de Brasília, com fundamento no § 3º do art. 4º do Decreto nº 10.543, de 13 de novembro de 2020.

Documento assinado eletronicamente por **Edilson Mineiro Sá Junior**, **Usuário Externo**, em 19/12/2023, às 15:41, conforme horário oficial de Brasília, com fundamento no § 3º do art. 4º do Decreto nº 10.543, de 13 de novembro de 2020.

Documento assinado eletronicamente por **Janaina Goncalves de Oliveira**, **Professor(a)**, em 20/12/2023, às 15:22, conforme horário oficial de Brasília, com fundamento no § 3º do art. 4º do Decreto nº 10.543, de 13 de novembro de 2020.

Documento assinado eletronicamente por **Pedro Santos Almeida**, **Professor(a)**, em 22/12/2023, às 12:09, conforme horário oficial de Brasília, com fundamento no § 3º do art. 4º do Decreto nº 10.543, de 13 de novembro de 2020.

A autenticidade deste documento pode ser conferida no Portal do SEI-Ufjf (www2.ufjf.br/SEI) através do ícone Conferência de Documentos, informando o código verificador **1591950** e o código CRC **72F3C8DB**.

ACKNOWLEDGMENT

First of all, I thank God for being present in my life and giving me support to achieve my goals.

To my wife Daiana, for the huge companionship in every moment of my life, as well as all the care, affection, and understanding. To my parents, Airton and Aparecida, who are responsible for my moral formation and give me all the support possible in this journey. To my brother, Rodrigo, for being a great friend and companion. And to all my family who has always been on my side.

I especially thank my supervisor professor Guilherme Márcio Soares for always contributing to my professional growth. To professor Henrique A. C. Braga and professor Pedro S. Almeida for all the support and the opportunity to research and make science. To all professors of the electrical engineering course at the Federal University of Juiz de Fora who contributed to my education. Furthermore, I thank professor José Marcos Alonso, who even from a distance also contributed to this work.

To my colleagues from the Lighting Research Group (NIMO-UFJF) because this work has the contribution of everyone, especially Lucas Resende for helping me during the research. To my other friends for being present in difficult moments.

Finally, I thank CAPES for its financial support.

“A failure is not always a mistake.
It may simply be the best one can do under the circumstances.
The real mistake is to stop trying.”
(Burrhus F. Skinner)

RESUMO

Este trabalho visa contribuir na área de *drivers* de LED alimentados a partir da rede elétrica que apresentam elevado desempenho, ou seja, conversores que possuem elevada eficiência, baixo custo, alta confiabilidade, elevada densidade de potência e alto fator de potência. O trabalho apresenta alternativas para a obtenção destas características desejáveis. Para a obtenção de alternativas topológicas de elevada eficiência, conversores ressonantes são empregado para a redução das perdas de comutação. Neste sentido, uma metodologia de elevada acurácia para projeto de um conversor LLC ressonante foi proposta, de modo que o ponto de operação do conversor e a transmissão de ripple de baixa frequência possam ser definidos com erros significativamente menores do que os obtidos através de outras estratégias, como as que utilizam a FHA (*First Harmonic Approximation*). O trabalho também endereça alternativas para o aumento da confiabilidade e da densidade de potência em drivers de LED. Estas duas características estão fortemente vinculadas ao dimensionamento dos capacitores empregados para a filtragem da ondulação de baixa frequência da corrente de saída, que costumam ser volumosos e diretamente relacionados à confiabilidade do circuito. Neste sentido, é proposta uma alternativa para a compensação da ondulação de baixa frequência, chamada de ARC (do inglês, *Active Ripple Compensation*), de modo que seja possível minimizar as capacitâncias de filtragem. A técnica proposta realiza a compensação através da modulação deliberada da frequência de operação do conversor, que permite uma significativa redução da capacitância de filtragem associada a um aumento insignificante da THD da corrente de entrada. Os resultados experimentais obtidos a partir de um protótipo de 96 W comprovaram o desempenho da ARC baseada em frequência, uma vez que foi alcançada uma redução de 66,6% da capacitância com um aumento de apenas 0,9% na THD. Além disso, é proposta uma metodologia de projeto sistemático baseada em um problema de otimização multi-objetivo com restrições para conceber um driver de elevado desempenho. A estratégia proposta permite o projeto simultâneo dos elementos do circuito de potência e do controlador com a ARC baseada em frequência, além de otimizar vários parâmetros de desempenho. Os resultados experimentais obtidos a partir do conversor otimizado comprovaram as melhorias significativas nos parâmetros de desempenho, como a redução de 38% na taxa de falhas e o aumento de 111% na densidade de potência dos elementos passivos. O conversor proposto também possui uma eficiência de 90,96%, atingindo as características desejáveis para um driver de elevado desempenho.

Palavras-chave: Conversor ressonante LLC. *Driver* de LED alimentado a partir da rede elétrica. Modelagem matemática acurada. Compensação ativa da ondulação de baixa frequência. Redução de capacitância. Otimização multiobjetivo.

ABSTRACT

This doctoral thesis proposal is focused on the area of high-performance off-line LED drivers, in other words, converters that feature high efficiency, low cost, high reliability, high power density, and high power factor. The work presents alternatives for achieving these desirable characteristics. In order to obtain topological alternatives with high efficiency, this research uses resonant conversion in the second stage to reduce switching losses. In this sense, a high-accuracy methodology for designing a dc-dc LLC resonant converter has been proposed, so that the operation point of the converter and the low-frequency (LF) current ripple transmission can be defined with errors significantly lower than the ones obtained by other strategies, such as based on First Harmonic Approximation (FHA). In order to reduce the total cost of the topology, the work studies converters that integrate the power factor correction (PFC) stage with the power control (PC) stage, thus reducing the number of components that yields simplicity and low cost. The work also addresses alternatives for increasing the reliability and power density of LED drivers. These two characteristics are strongly linked to the sizing of the capacitors used to filter the low-frequency ripple of the output current, which are often large and directly related to the circuit reliability. In this regard, an alternative for Active Ripple Compensation (ARC) techniques is proposed to reduce the converter bulk capacitance. The proposed technique performs the compensation by deliberate modulation of the converter's switching frequency, which allows for a huge capacitance reduction with a negligible increase in the THD of the input current. Experimental results gathered from a 96-W laboratory prototype supplied from a 127-V 60-Hz grid attested to the superior performance of the frequency-based active ripple compensation since a capacitance reduction of 66.6% has been obtained with an increase of only 0.9% in the THD. In addition, a systematic design methodology based on a constrained multi-objective optimization problem is proposed for designing high-performance drivers. The proposed strategy enables the simultaneous design of the power circuit elements and the controller with frequency-based ARC, while optimizing various performance parameters. Experimental results from the optimized converter demonstrated the significant improvements in performance parameters, such as a 38.25% reduction in failure rate and a 111.69% increase in power density of passives elements. The proposed converter also achieved an efficiency of 90.96%, meeting the desirable characteristics for a high-performance driver.

Key-words: LLC resonant converter. Off-line light-emitting diode (LED) drivers. Accurate mathematical modeling. Active ripple compensation. Capacitance reduction. Multi-objective optimization.

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF ABBREVIATIONS

ABNT	Association of Technical Standards (Associação Brasileira de Normas Técnicas)
ac	alternating current
Al-Caps	Aluminium Electrolytic Capacitors
ARC	Active Ripple Compensation
BBLC	totem-pole bridgeless boost PFC integrating HB LC SRC
BCM	Boundary conduction Mode
CCM	Continuous Conduction Mode
dc	direct current
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FB	full-bridge
FHA	First Harmonic Approximation
FIT	Failures in Time
GaN	Gallium Nitride
HB	half-bridge
IBbLLC	PFC buck-boost integrating HB LLC converter
IBoLLC	PFC boost integrating HB LLC converter
IBuFly	Integrated buck flyback converter
IDBB	Integrated Double Buck-Boost Converter
IEA	International Energy Agency
InGaN	Indium gallium nitride
LED	Light-Emitting Diode
LF	low-frequency

LFR	low-frequency ripple
MPPF-Caps	Metallized Polypropylene Film Capacitors
NIMO	Núcleo de Iluminação Moderna
PC	Power Control
PF	Power Factor
PFC	Power Factor Correction
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RPI	Resonant Proportional-Integral
SiC	Silicon Carbide
SRC	Series Resonant Converter
THD	Total Harmonic Distortion
UFJF	Universidade Federal de Juiz de Fora
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

CONTENTS

1 INTRODUCTION

1.1 ENERGY-EFFICIENT LIGHTING

Lighting is a fundamental aspect of modern life, significantly impacting both individual well-being and workforce productivity. Artificial lighting extends the productive day and allows people to access places where there is no natural light, among other many indoor and outdoor lighting applications. As economies mature and populations expand, the global demand for lighting continues to rise, making lighting systems indispensable to modern society.

According to Lafitte & Garcia (2021), lighting systems consume about 15% of the produced global electricity, thus representing a considerable portion of the world's energy consumption. Therefore, the use of efficient technologies for lighting purposes is quite interesting, mainly by reducing the energy consumed.

Unlike incandescent and fluorescent lamps, Light-Emitting Diodes (LEDs) are not inherently white light sources. The emergence of InGaN-based LEDs has allowed for the generation of white light from these devices, which can now be used as a general-purpose light source. With this discovery, light-emitting diodes are increasingly becoming popular in lighting applications.

The luminous efficacy of the LEDs has improved considerably in recent years. According to Craford (2007), LED is the technology that presents the most evolution in luminous efficacy when compared to other light sources. Since 2010, the average efficacy of LEDs has improved by 6-8 lumens per watt (lm/W) each year (IEA, 2021). LEDs typically available in the market have an efficacy of over 100 lm/W. Currently, there are commercial LEDs that can achieve a luminous efficacy higher than 200 lm/W, but they are much more expensive, such as the LED LM301B EVO from Samsung Electronics (SAMSUNG SEMICONDUCTOR, INC, 2022).

The global trend in lighting sales is illustrated in Figure 1.1 from a study completed by the IEA (2021). Over 50% of buildings sector lighting markets globally are covered by LEDs. In addition, it is expected that all countries will sell only LEDs by 2025. Therefore, conventional lighting sources such as incandescent, fluorescent, and high-intensity discharge are being replaced by solid-state light-emitting diode technology, enabling energy savings with increased adoption.

Figure 1.2 shows the energy consumption and potential energy saving across 156 nations for efficient LED lighting. According to Lafitte & Garcia (2021), it is estimated that 194 TWh could be saved annually by 2030. This is equivalent to a financial savings of over 16 billion dollars as a result of reduced electricity bills, highlighting the importance of using efficient lighting systems.

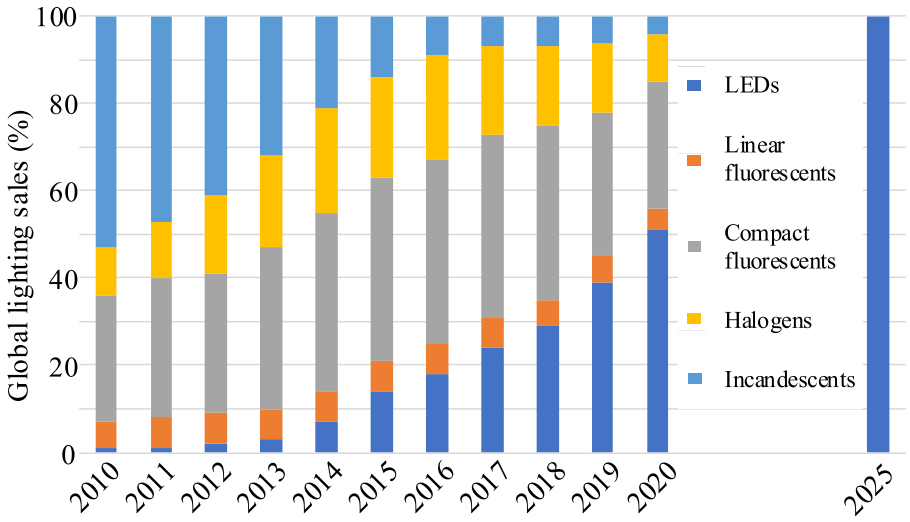


Figure 1.1 – Global lighting sales, historical and expected in 2025 (IEA, 2021).

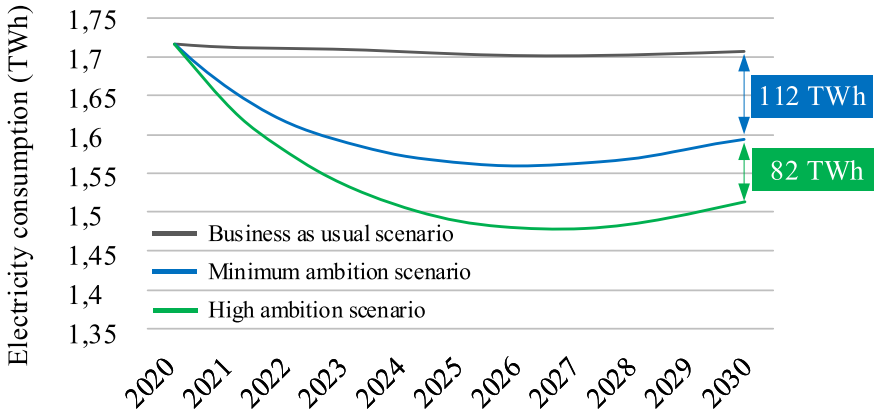


Figure 1.2 – Savings potential of lighting by 2030 (LAFITTE; GARCIA, 2021).

Besides the LEDs, the overall performance of an energy-efficient lighting system also depends on the driver, which is responsible for regulating the current flowing through the devices. Before exploring some characteristics of these two elements, converter and LED, it is important to define concepts concerning performance in off-line LED drivers.

1.2 HIGH-PERFORMANCE OFF-LINE LED DRIVERS

This section presents the concepts associated with high performance. Then, these concepts are applied to off-line LED drivers, and performance indexes are defined to determine a high-performance off-line LED driver.

1.2.1 **Concepts of high performance**

The term “performance” originated in Greece around 550 bc, emerging from the theatrical realm, where it referred to an actor, singer, or dancer who demonstrated exceptional skill and artistry (SCHECHNER, 2020). Years later, in the industrial revolution movement, the concept of performance was adapted to the industry (JURAN; GRYNA, 1980). High performance was used to refer to equipment that kept active and working for a period superior when compared to others. Therefore, the performance was given by comparison and extreme use without failures or maintenance (TORRES; MARTINS, 2021).

From the 1940s to the 1960s, business management models emerged and employees who exceeded their daily tasks were said to have “high performance”, referring to workers who had the capabilities or skills to perform their tasks with greater dexterity. However, when this concept of performance is addressed to people, it undergoes many influences, currently making it quite broad, ambiguous, and multifaceted (ALATAILAT; ELREHAIL; EMEAGWALI, 2019). Based on studies of Tuckman (1965), high performance begins to be seen under multiple meanings from the 1980s, such as evaluation, performance, efficiency, dexterity, acting, performing, etc.

Quality and process improvement were discussed in Deming (2018). This work uses the concept of high performance of machines, methods, and processes as learning and constant improvement. Thus, when proposing a performance, one aims to execute a work or activities above expectations. According to Fletcher (1995), high-performance is simply about achieving better than expected results in a sustainable way. Moreover, the literature provides a clear picture of performance for the purpose of measuring, raising organizational results, improving employees’ quality of life, and job satisfaction (GARCÍA-CHAS; NEIRA-FONTELA; VARELA-NEIRA, 2016; HUANG et al., 2016; JR, 2017). In addition, Torres e Martins (2021) shows that performance can be perceived as evaluation metrics, efficiency, skill, competence or soft skill.

In this context, this work considers high performance as producing better than expected results. It is important to highlight that the expected results depend on the application and must be measurable based on the performance parameters defined for the operation.

1.2.2 **Concept of high performance applied to off-line LED drivers**

As mentioned earlier, high performance is achieved when the results obtained are better than expected. Therefore, it is important to clarify what is expected of an off-line LED driver. In power electronic converters, the main quantities that determine the performance are the power losses, the volume, the weight, the failure rate, and the

system costs (KOLAR et al., 2010). The converter weight enables simple handling, installation, and maintenance of the system (EVERTS, 2014). Despite these advantages and the significant impact in the area of electric vehicles, the converter weight will not be considered in this work whose focus is on off-line LED drivers, which in the case of outdoor lighting applications, are usually installed on a robust pole. On the other hand, off-line LED drivers are typically connected to the low-voltage grid, which is often single-phase and unbalanced across the phases. Some standards such as NBR-16026:2012 (ABNT, 2012) and IEC-61000-3-2:2018 (IEC, 2018) establish input requirements for devices connected to the electricity grid to ensure low impact on power supply parameters. This makes the quality of the ac input power a critical factor in outdoor lighting applications. This parameter can be quantified using both the power factor (PF) and the amount of harmonic current injection into the grid, as well as the total harmonic distortion (THD) of the input current.

In this way, the present work investigates the high performance by relative quantities that are termed "performance indexes", being respectively the efficiency, power density, cost savings, reliability, and power quality. It is quite important to highlight that these performance indexes are mutually coupled, thus representing a trade-off between them, as illustrated in Figure 1.3. For example, high power densities generally imply high frequencies, which potentially lead to a reduction in efficiency, showing a trade-off between increasing switching losses and reducing the size of the passive elements. Transistors based on Gallium Nitride (GaN) or Silicon Carbide (SiC) enable ultra-high efficiencies, but are still expensive or have incompatible typical ratings (voltages, currents limits) for LED off-line applications.

Multifunctional chips and stage integration techniques both incorporate multifunctional parts and components, yielding circuits using fewer parts, thus reducing

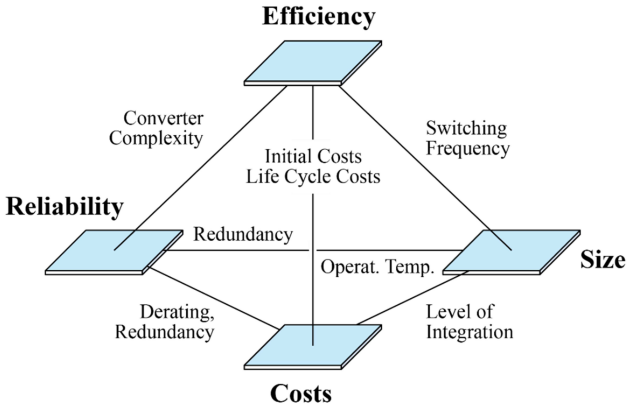


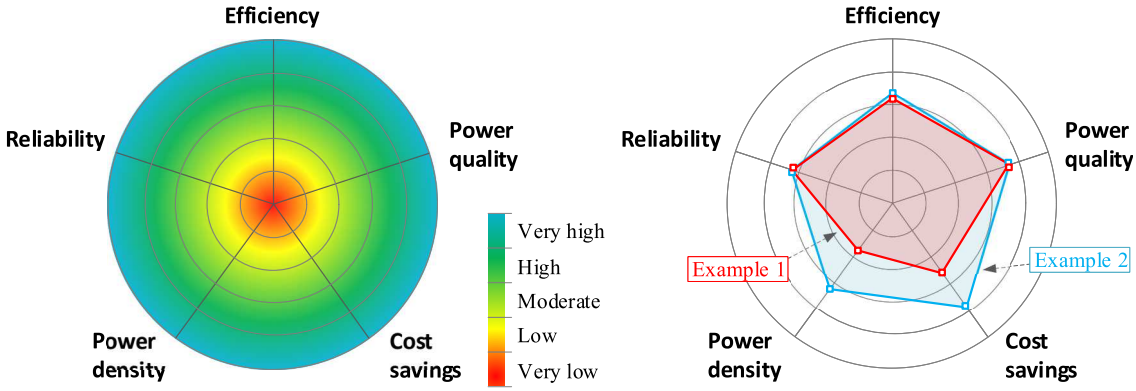
Figure 1.3 – Mutual coupling of performance indexes of power electronic converter systems (KOLAR, 2016).

size. However, depending on the level of integration, the converter can need more support devices (filters, monitoring, control, thermal management, and the like) or more complex components. Thus, the level of integration can require a trade-off analysis between size and cost. Another performance indicator defined is reliability, which is the ability of a system or component to perform its required functions under stated conditions for a specified period (SONG; WANG, 2012). In some cases, the reliability of the system is improved by using more components (redundancy), which can result in decreased performance of other attributes such as size and cost (SFAKIANAKIS; EVERTS; LOMONOVA, 2015).

Based on the discussion in this section, it is clear that performance parameters are strongly coupled. Often one performance parameter is improved at the cost of a significant deterioration in another. In the case of off-line LED drivers, achieving good results in all five performance indexes (efficiency, power density, cost savings, reliability, and power quality) is very important and challenging. In this context, high-performance off-line LED drivers are achieved when these trade-offs are improved. In other words, high-performance LED drivers can improve some performance indexes without a significant decrease in others.

In order to assess and compare different converters, these mutually coupled factors will be evaluated together using a spider (or radar) graph, which is suitable for comparing several different dimensions in a compact space. Figure 1.4a shows the performance analysis tool with a color scale, highlighting the qualitative levels that will be used in the evaluation.

This visual tool is ideal for displaying and comparing performance, as presented in several works (CITTANTI; VICO; BOJOI, 2022; SHARMA et al., 2022; CENTENARO et al., 2021; EVERTS, 2014; KOLAR, 2016). In this graph, each dimension gets its axis that represents a single performance index. The further away from the center, the better the performance of the respective metric. It's important to note that the area of the graph can not be used as an overall performance metric, as it depends on the scale of the axes. In other words, each performance index should be evaluated independently based on its respective axis. Figure 1.4b shows two examples of LED drivers from the perspective of the five performance indexes. As can be seen in this figure, the analysis tool allows for easy comparison of converters, whereby the Example 2 converter performs better in terms of power density and cost savings when compared to the Example 1 converter. From this tool, a high-performance off-line LED driver can be graphically identified when all five performance indexes score well.



(a) Performance analysis tool

(b) Example of performance evaluation

Figure 1.4 – Performance analysis tool for comparing off-line LED drivers.

1.3 DESIRABLE FEATURES FOR OFF-LINE LED DRIVERS

Given the concept of high performance, this section shows some desirable characteristics for LED drivers, highlighting the existing constraints for LED driving in off-line applications.

In general, the most common power source for lighting systems is the ac power grid. Therefore, off-line LED drivers are an interesting topic for investigation. Unfortunately, some problems resulting from ac-dc conversion can occur depending on the technique or topology used in the converter design. Many of them are associated with harmonic pollution of the mains and low PF that reduce the quality of distribution systems. In order to avoid these problems, the converters must comply with power quality requirements imposed by standards. Thus, these drivers are expected to have a power factor greater than 0.92 and reduced THD of the input current (ABNT, 2012). In addition, it is fundamental that LED drivers comply with the IEC-61000-3-2 standard, since lighting devices above 25 W, classified as Class C of this standard, must fulfill the emission limits for the harmonic content of the current (IEC, 2018). The maximum amplitude of the h-th order harmonic component of the input current established by the IEC-61000-3-2 standard is shown in Table 1.1.

The power quality requirements can be met by using a power factor correction stage, which is designed so that the current drained from the grid has a sinusoidal characteristic and is in phase with the voltage. On the other hand, the power control stage performs the dc-dc conversion to stabilize the current in the LEDs, maintaining the average and ripple value at desired levels.

Table 1.1 – Limits of harmonic emission of Class C equipment according to IEC-61000-3-2 standard.

Order	Maximum allowable current (normalized to the fundamental)
2	2 %
3	30·PF$_m$[1] %
5	10 %
7	7 %
9	5 %
11	3 %
$13 < h < 39$	3 %

Another important aspect in the design of LED drivers is the overall efficiency, which is an issue to be addressed in the design of such devices since it has a direct relation to the effective luminous efficacy of an LED lamp (ALMEIDA, 2014). In this sense, LED drivers can help save energy in lighting applications. In addition, a combination of energy-efficient lamps and drivers produces the best possible outcome in terms of lighting performance, achieving even greater energy savings. Therefore, it is recommended that the driver should have a high efficiency.

Solid-state lighting systems commonly work at low power levels, typically 25 W to 250 W, which makes it difficult to obtain high-efficiency converters for LED driving (ALMEIDA, 2014). Among work focused on improving the conversion efficiency of off-line LED drivers, one can highlight:

- Partial power reprocessing techniques through non-cascaded connections between the PFC and PC stages (CAMPONOGARA et al., 2013);
- Synthesis of PC stages with reduced power redundant processing (YU et al., 2011).
- Use of resonant conversion in some driver stages to reduce switching losses (SICHIROLLO; BUSO; SPIAZZI, 2012; ARIAS et al., 2012);
- Use of synchronous rectification at the output of converters with galvanic isolation at high frequency (ARIAS et al., 2013);
- Use of bridgeless rectifiers to reduce conduction losses in semiconductors (ALMEIDA et al., 2013b).

Among the different possibilities, one can highlight the load-resonant converters, since they enable soft-switching, thus improving the driver efficiency (LAZAR;

[1] Measured power factor.

MARTINELLI, 2001; WANG et al., 2016a; QU; WONG; TSE, 2015). Resonant converters are typically employed as dc-dc converters used in the power control stage of LED drivers because it is a good alternative for reducing the bulk capacitance connected at the output of the power factor correction (PFC) stage. Besides providing higher efficiency for the whole system, resonant converters may help to reduce the propagated low-frequency (LF) ripple to the output LED current (FERRAZ et al., 2021; ALMEIDA et al., 2013a; MELO et al., 2015b).

The subject of LF ripple is especially important in off-line LED power supplies since the pulsating single-phase power at the input produces a low-frequency voltage ripple at its output at a frequency twice that of the line frequency. This voltage ripple is propagated through the converter and reaches the load, producing a large current ripple in the LED string due to its inherent low dynamic resistance. These instantaneous power oscillations are typically filtered out by bulky electrolytic capacitors, which are known to reduce the circuit lifespan, or by using a bank of metalized film capacitors, which have a better lifespan but decrease the power density of the drivers (WANG; BLAABJERG, 2014; WANG et al., 2020). Therefore, in order to mitigate these problems and attenuate the output current ripple, reduced capacitance is also a desired aspect in the design of high-performance off-line LED drivers.

It is worth noting that the converter represents an appreciable portion of the total cost of a solid-state lighting system. To mitigate this problem, the converters should be simple and with a low number of components to increase the economic attractiveness of such lighting systems. Thus, there is a research trend toward reducing the cost of the LED driver. Some works have proposed the use of integrated topologies, which are based on the integration of the PFC and the PC stages in order to reduce the component count and the driver cost (SOARES et al., 2017; ALMEIDA et al., 2015b). The use of converters with reduced capacitance and integrated topologies contributes to achieving high-density power drivers, responding to the industrial market trend towards higher levels of integration and lower development costs.

Galvanic isolation is an often-recommended practice for isolating the LED load's safe voltages from the power grid (CASTRO et al., 2019). This requirement is commonly met using transformers or coupled inductors, ensuring no direct connection between the input and output, thereby mitigating the risk of electric shocks. Galvanic isolation becomes mandatory when the driver is not integrated within the LED. On the other hand, drivers with galvanic isolation have higher costs and size, which decreases the power density. Therefore, it is recommended to use isolated drivers from the perspective of electrical safety. However, if the designer has no safety issues and prefers a more economical solution with a higher power density, it is recommended to use non-isolated drivers.

Another feature that can be considered when designing a LED driver is its ability to operate with a wide input voltage range, or even universal compatibility to worldwide line voltages (90-264 V) (LUO et al., 2019). Figure 1.5 shows the line voltage and frequency used in each country of the world. As can be seen, the domestic line voltage in which the driver can operate varies dramatically worldwide. Therefore, universal input voltage operation is an important attribute for LED drivers since they can be used anywhere in the world. On the other hand, a wide input voltage range is a requirement that is difficult to meet while achieving both high power density and high efficiency (SANTIAGO-GONZALEZ et al., 2018).

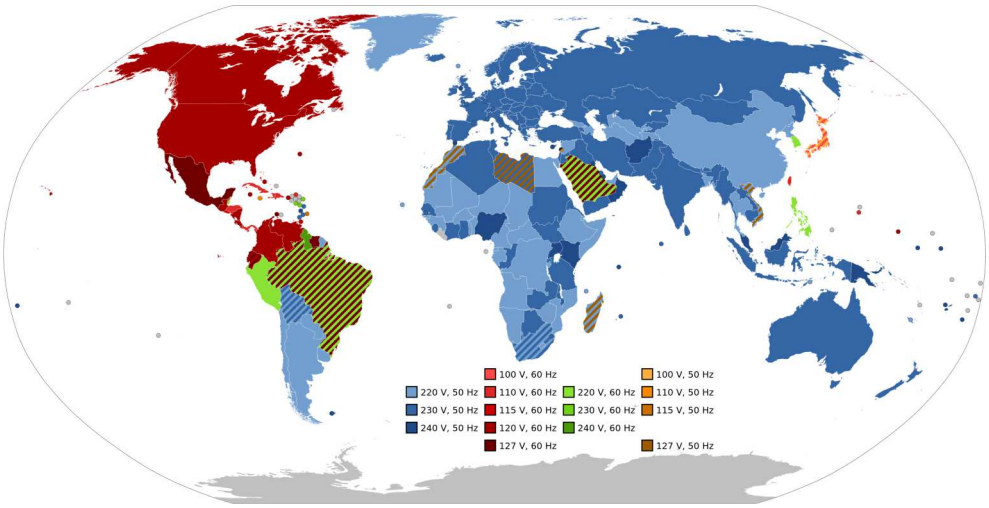


Figure 1.5 – Countries of the world, coloured according to their nominal power net voltage and frequency (SOMNUSDE, 2009).

In the context of desirable features in LED drivers, converters pursue enhanced efficiency, as well as improvements in power density, reliability, and lifetime. Furthermore, galvanic isolation and universal input operation can also be required in some applications at the cost of reducing power density and efficiency. As previously discussed, the performance parameters of off-line LED drivers are interconnected, and often, design conditions are arbitrarily chosen in most works. In order to address interconnected performance criteria, and mitigate the impact of arbitrary design choices, some recent studies have proposed design converters based on multi-objective optimization (RASHIDI et al., 2021; KOLAR, 2016; EVERTS, 2014).

1.4 LIGHT-EMITTING DIODES

Light-emitting diodes are devices that consist of two semiconductor layers, one of the P-type (anode) and one of the N-type (cathode), thus forming a P-N junction. When the P-N junction is direct polarized, a flow of electrons from the N to the P region

occurs (direction of the higher electric field potential), while an apparent movement of gaps from the P to the N region also takes place in a dual form (ALMEIDA, 2014). When the electron has enough energy to pass through the P-N junction, it moves from the conduction layer (highest energy level) to the valence layer (lowest energy level) by recombining with a gap. The recombination of the electron with the gap releases energy in the form of heat and light.

LEDs applied in lighting can be divided into two groups: high-brightness LEDs, which work at low power levels, and power LEDs, which operate at higher power levels with typically rated currents of 300 mA to 1.5 A. The power LEDs are best suited for outdoor applications, such as street lighting since they generally have higher luminous flux and efficacy than high-brightness LEDs (RODRIGUES et al., 2011).

In addition to high luminous efficacy and the ability to emit white light, LEDs have features such as high color rendering index, low operating temperature, small size, and long life that make them advantageous in lighting. Based on these features, light-emitting diodes are increasingly becoming the main source of artificial lighting, especially because of their potential of reducing energy consumption (SUN et al., 2014; LI et al., 2016; CHCH et al., 2010; LEE et al., 2015).

1.4.1 **Electrical Model**

The electrical model of the LEDs is useful in the design of the LED driver system and can be obtained similar to a diode because of the p-n junction structure (semiconductor devices). This model is given by the modified Shockley equation (1.1) proposed in Schubert, Gessmann e Kim (2005).

$$v_{LED}(i_{LED}) = \frac{n_i k T_j}{q_e} \ln\left(\frac{i_{LED}}{I_s}\right) + R_s i_{LED}, \tag{1.1}$$

in which:

n_i - Ideality factor;

k_B - Boltzmann's constant ($1{,}3806504 \cdot 10^{-23}$ J/K);

T_j - Junction temperature (in Kelvin);

q_e - Elementary charge of the electron ($1{,}602176487 \cdot 10^{-19}$ C);

I_s - Reverse bias saturation current;

R_s - LED series resistance.

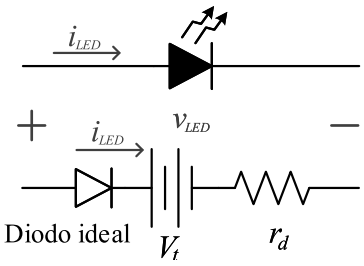


Figure 1.6 – Piecewise linear model of the LED.

The behavior of the LED is described with high accuracy by (1.1). However, it is often desirable to obtain a straightforward mathematical representation in order to simplify the design. In this sense, (1.1) can be reduced to a piecewise linear model useful for analyzing converter topologies for driving LEDs (SOARES, 2014). The straightforward model, given by (1.2), describes the LED as a constant voltage source connected in series with an ideal diode and a resistance, where V_t represents the threshold voltage and r_d the dynamic resistance of the LED. Figure 1.6 depicts this simplified model.

$$v_{LED} = V_t + i_{LED} r_d \tag{1.2}$$

The validation of the piecewise electrical model of the LED was experimentally verified in Almeida et al. (2011) for OSRAM LUW WPM-Golden Dragon LED. The comparison of the equivalent model (1.2) with the theoretical I-V characteristic curve of the LED obtained from (1.1), as well as the experimental results, are present in Figure 1.7. The equivalent model is determined based on the points measured around the operating current. The parameters of the LED under consideration were $r_d = 700$ mΩ and $V_t = 2.96$ V. It can be seen that the equivalent piecewise electrical model is adequate to represent the LED, once the operation is away from the knee region of the curve.

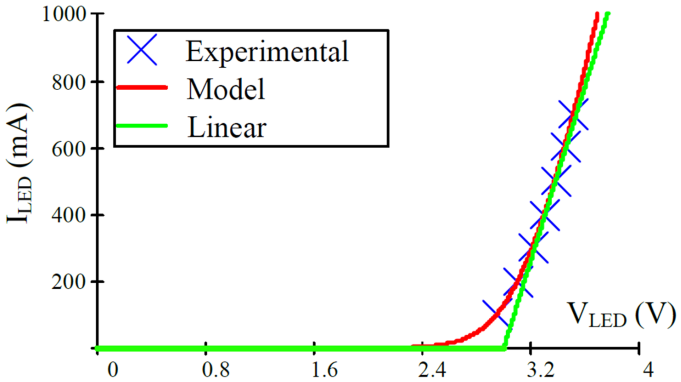


Figure 1.7 – Curve of the piecewise linearized model compared to the theoretical I-V characteristic curve (ALMEIDA et al., 2011).

1.4.2 **Influence of the temperature on the LEDs performance**

As mentioned earlier, some of the energy released during recombination is transformed into heat, directly affecting the performance of the LEDs. Hence, the proper thermal management of the device is one of the most fundamental requirements for driving LEDs that aims to ensure the operation of the LEDs at an appropriate temperature condition and according to the parameters set by the manufacturer.

It is important to highlight that the P-N junction temperature is related to the photometric characteristics of LEDs. The correlation between temperature and photometric performance of the devices has been studied in several works, which show the luminous flux and luminous efficacy decreasing as the P-N junction temperature increases (GARCIA et al., 2008; HUI; QIN, 2009; YAN et al., 2011; ALMEIDA et al., 2015a; CHEN; TAO; HUI, 2012). The analysis known as photoelectrothermal characterization was also addressed in Bender et al. (2013) and Almeida (2014). This model takes into account the interactions between photometric parameters (such as luminous flux, luminous efficacy, color temperature, chromaticity coordinates, and power spectral density), thermal aspects (dissipation, ambient temperature, and junction temperature), and electrical characteristics (current, the power dissipated and electrical parameters of the equivalent model).

The average current of the LEDs is related to the luminous flux and the luminous efficacy (ALMEIDA et al., 2015a). This relationship can be seen in the experiment presented in Almeida et al. (2015a) for a LED lamp consisting of 6 Philips Lumileds LXML-PWN1 LEDs. In this experiment, whose results are shown in Figure 1.8, the LEDs were allocated on a heatsink with a thermal resistance of 4.39 ^{o}C/W, and the ambient temperature was controlled at 25 ^{o}C. Note that for the heatsink employed, the luminous flux saturates around 700 mA, i.e., this current would be the maximum to ensure a good ratio between luminous flux and luminous efficacy.

Because of the relationship of luminous flux to average current and temperature, the thermal design can be optimized by sizing the LED module heatsink so that maximum flux is achieved for the desired average output current of the converter, as discussed in Hui et al. (2010).

1.4.3 **Influence of the current waveform on the LEDs performance**

Another factor that also significantly affects the photometric performance is the waveform of the current flowing through the LEDs. Figure 1.9 shows the typical waveform of the current in the LEDs when the converter is supplied from the mains, representing this magnitude in terms of the average value I_o and the low-frequency ripple (LFR) ΔI_o at twice the mains frequency (f_L).

Low-frequency current ripple effects on flux and luminous efficacy was addressed in Almeida et al. (2015a), Almeida, Soares e Braga (2013). According to the works aforementioned, an output ripple value of 50% ($\Delta I_o/I_o$) would be an acceptable limit when it is desired to increase the current ripple without causing harm to the photometric performance since for the worst-case obtained from the LEDs analyzed, the flux and efficiency decreased by only 3%.

Moreover, the current ripple can cause flickering effects, which could be noticeable to the human eye in some circumstances and can lead to human biological effects (LEHMAN; WILKINS, 2014). This effect is addressed in the following.

1.4.4 **Human biological effects of light flicker**

Light flicker can be defined as a rapid repetitive change in brightness and can become a hazard to health, provoking an increased incidence of headaches and even epileptic seizures (FISHER et al., 2005; BULLOUGH et al., 2012). According to

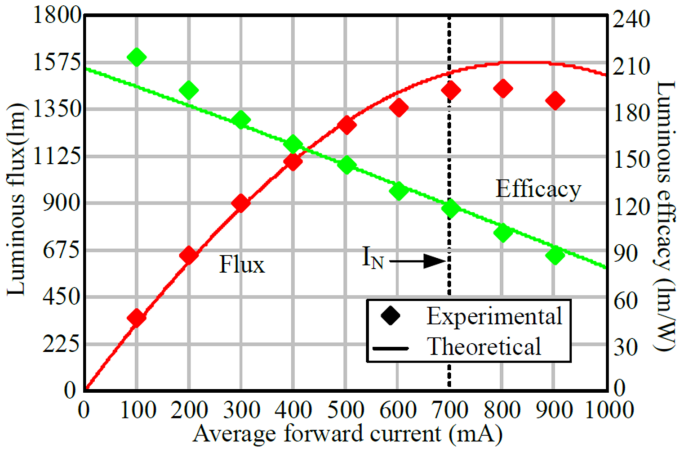


Figure 1.8 – Luminous flux and luminous efficacy of an LED Philips Lumileds LXML-PWN1 according to variations in the average forward current (ALMEIDA et al., 2015a).

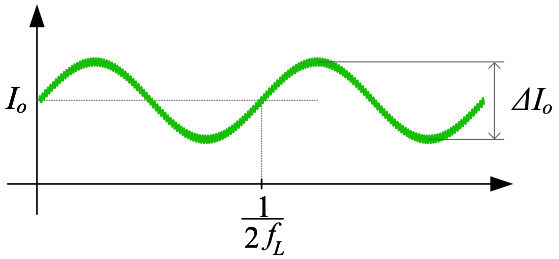


Figure 1.9 – Typical waveform of the current in the LEDs when the converter is supplied from the mains.

Lehman et al. (2011), the percent flicker $Mod\%$ is defined as

$$Mod\% = 100\frac{L_{max} - L_{min}}{L_{max} + L_{min}}, \tag{1.3}$$

where L_{max} and L_{min} represent the maximum and minimum measured light intensity from the lamp, respectively.

Some works evaluate the effect of this phenomenon on human health (LEHMAN; WILKINS, 2014; IEEE, 2015). Studies have shown that when the flicker frequency ($f_{flicker}$) is lower than 90 Hz, illuminance modulation is more sensitive since it can remain hazardous to humans with $Mod\%$ values lower than 0.9%. Furthermore, for $f_{flicker}$ higher than 90 Hz, the percent flicker can correspond to:

- low-risk level: $Mod\% < 0{,}08 f_{flicker}$;
- no-observable-effect level: $Mod\% < 0{,}033 f_{flicker}$.

Since the light emitted by the LED is proportional to the current, (1.3) can be rewritten in terms of the low-frequency ripple $\Delta I_{LED\%}$ (SOARES, 2017). Thus, the flicker levels concerning the ripple are:

- low-risk level: $\Delta I_{LED\%} < 0{,}16 f_{flicker}$;
- no-observable-effect level: $\Delta I_{LED\%} < 0{,}066 f_{flicker}$.

Normally, the flicker frequency will have a fundamental component at twice the ac line frequency, which is the low frequency of the LED current. Hence, if the mains frequency is 60 Hz ($f_{flicker} = 120$ Hz), the maximum acceptable ripple in the LED current would be 19.2% and 7.9% for low risk and no risk, respectively. Therefore, this undesirable LF ripple in the LED current is a limiting factor for solid-state lighting systems (ALMEIDA et al., 2013a; IEEE, 2015).

Since the current waveform can significantly affect the photometric performance of the LEDs and can cause stroboscopic and flickering effects, the LED must be properly driven by an electronic circuit. Therefore, this device must control the average value and ripple level of the LED current. Moreover, it is interesting that these goals are achieved with all five performance indexes (efficiency, power density, cost savings, reliability, and power quality) scoring well.

1.5 PROPOSALS AND ORGANIZATION OF THE WORK

Based on the discussions of the last sections, this work proposes some contributions in LED driving, focusing on high-performance off-line LED drivers with reduced storage capacitance and high efficiency.

Before presenting alternatives for high-performance LED driver, some features concerning capacitor technologies and converters with reduced capacitance are addressed in chapter 2. The off-line LED drivers based on resonant converters and their analysis procedures are also outlined in this chapter.

The capacitance reduction implies a large ripple at the bus voltage, which requires an accurate model of the resonant stage for proper converter design. In this sense, chapter 3 presents an analysis and a design methodology for a dc–dc LLC resonant converter applied to off-line LED driving. An investigation regarding the main design parameters that influence the LED low-frequency (LF) ripple has been carried out, showing that the design of the LLC resonant converter for off-line LED driving is a trade-off between the converter efficiency and the LF ripple transmission. Experimental results were taken from two 46-W laboratory prototypes considering two different design goals: one for LF ripple reduction and another aiming at the highest converter efficiency and better power quality.

Based on the requirements presented in chapter 1, about Active Ripple Compensation (ARC) techniques for minimizing the converter bulk capacitance, and taking into account the numerical model described in chapter 3, a novel frequency-based ARC technique is proposed in chapter 4 as an alternative to the conventional ARC methodology, in which the duty-cycle is modulated. This chapter presents a generalized analysis of ARC techniques applied to integrated off-line LED drivers where the input current harmonic content and the output ripple reduction have been theoretically predicted for each converter. These analyses show that the frequency-based ARC approach applied to resonant converters feature a better performance than the one used in hard-switching converters since it allows for a huge capacitance reduction with a small THD increase.

Chapter 5 presents a design example of an integrated off-line LED driver with frequency-based ARC. The topology chosen for the PC stage needs a higher modulation amplitude for capacitance reduction, thus resulting in higher input current distortion among the LLC converters evaluated in chapter 4. Therefore, this converter was chosen to show the higher influence of the frequency modulation on the input current of the integrated off-line LED drivers based on load-resonant converters. Experimental results gathered from a 96-W laboratory prototype supplied from a 127-V 60-Hz grid attested the superior performance of the frequency-based active ripple compensation since a capacitance reduction of 66.6% has been obtained with an increase of only 0.9% in the THD.

Based on the numerical model shown in chapter 3, and on the frequency-based ARC technique proposed in chapter 4, a systematic design methodology based on a constrained multi-objective optimization problem is proposed in chapter 6 for designing high-performance drivers. This chapter presents a case study of a PFC bridgeless boost

converter integrated with the LLC resonant converter. The passive elements and the controller are designed, while optimizing performance parameters according to the designer's requirements. Experimental results were taken from two laboratory prototypes, benchmark and optimized converter, attesting the significant improvements in performance parameters, and meeting the desirable characteristics for a high-performance driver.

Finally, chapter 7 presents the final considerations of this work and discusses some proposals for future works.

2 REVIEW OF THE TECHNICAL LITERATURE

The previous chapter has shown the importance of the study of LED driving, primarily regarding high-performance off-line LED drivers that aim for high efficiency, power density, reliability, ac input power quality, and low cost. Section 2.1 presents the main characteristics of capacitors: reliability, lifetime, and power density of the storage element. These aspects can be enhanced through capacitance reduction techniques, which are addressed in section 2.2. Regarding the search for increasing efficiency, section 2.3 explores the off-line LED drivers based on resonant converters. Furthermore, section 2.4 reviews the analysis methodologies for resonant converters. Finally, section 2.5 presents the partial conclusions of this chapter.

2.1 DC-LINK CAPACITORS

This section shows that the capacitor used in the off-line LED driver has a direct impact on three performance indexes: reliability, cost and power density. These parameters are greatly affected depending on the technology adopted and the capacitance value. Therefore, the study of this element is crucial to achieving a high-performance off-line LED diver.

In off-line LED power supplies (ac-dc converters), the pulsating single-phase power at the input produces a low-frequency voltage ripple at its output at twice the line frequency. This conversion between dc and ac electric power requires energy buffering to balance the instantaneous power difference between the two systems. Barth et al. (2019) presented a comparison of instantaneous power presented by single-phase ac at twice the line frequency and the average dc power over one power line cycle. Figure 2.1 shows these instantaneous power oscillations typically filtered out by electrolytic capacitors (WANG; BLAABJERG, 2014; WANG et al., 2020). The region highlighted in green color represents the energy stored in the capacitor at each half-line cycle. Similarly, the area in red indicates the energy released by the capacitor.

The energy that is being charged to or discharged from the decoupling capacitor during a half-line cycle can be calculated by integrating one of the colored areas in Figure 2.1, which yields (2.1) (HU et al., 2013). On the other hand, according to Barth et al. (2019), this energy also can be calculated by the average power P_{avg} and the line frequency f_L as described in (2.2).

$$E = \frac{1}{2}CV_{C\text{max}}^2 - \frac{1}{2}CV_{C\text{min}}^2, \tag{2.1}$$

$$E = \frac{P_{\text{avg}}}{2\pi f_L}. \tag{2.2}$$

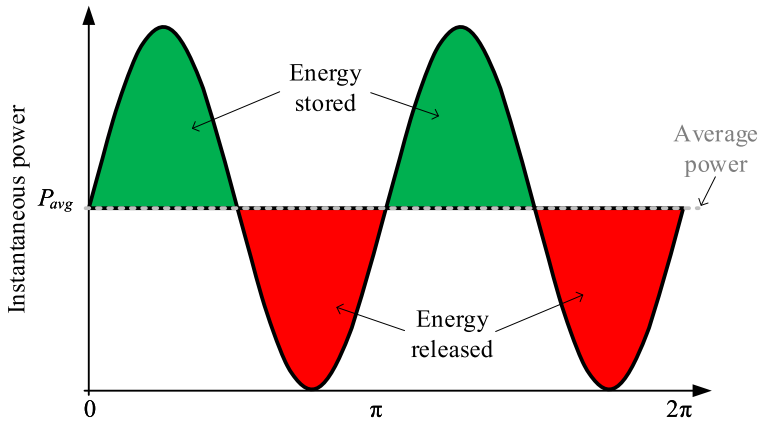


Figure 2.1 – Comparison of instantaneous power presented by single-phase ac at twice the line frequency and the average dc power over one power line cycle (BARTH et al., 2019).

In several applications, the capacitance value is designed from its voltage ripple ΔV_C. Thus, assuming V_C as the arithmetic average of $V_{C\max}$ and $V_{C\max}$ and combining (2.1) and (2.2), the equation typically used for capacitance design is given by

$$C = \frac{P_{\text{avg}}}{2\pi f_L V_C \Delta V_C}. \tag{2.3}$$

As can be noted, the required capacitance is obtained by the average voltage and maximum allowable voltage ripple. Therefore, for a given load power P_{avg}, the only way to change the capacitance value is by manipulating these two parameters. In this sense, it is possible to reduce the capacitance value by increasing V_C or (and) ΔV_C (WONG et al., 2016).

Capacitors are one of the most critical elements in an LED driver because this component can affect dramatically the reliability of the system according to the technology used. There are two types of capacitors typically employed for LED driving applications: the Aluminum Electrolytic Capacitors (Al-Caps) and Metallized Polypropylene Film Capacitors (MPPF-Caps). In this section, the characteristics of such technologies will be presented, highlighting the advantages and drawbacks of each one. It is worth mentioning that other capacitor technologies can be applied to LED drivers, such as Multilayer Ceramic Capacitors (MLC-Caps) and Aluminium Polymer Capacitors (AP-Caps). However, these technologies will not be discussed in this work since they are yet incipient, high-cost technologies. Although the cost of MLC-Caps and AP-Caps are declining, Al-Caps and MPPF-Caps remain the more widely used and cheaper.

2.1.1 **Reliability**

Generally, the failure modes of capacitors can be categorized into three different types: the early failures, which are premature defects related to the manufacturing process; the catastrophic failures (or random failures), which occur due to single-event overstress within the lifetime; and wear-out failures due to the long time degradation of capacitors (SOARES, 2017).

The predominant failure mechanisms for Al-Caps have been presented in Alwitt e Hills (1965), as well as in Chemi-con (2013). These works shows that dominant wear-out failure mechanisms are electrolyte vaporization and electrochemical reaction. On the other hand, for MPPF-Caps, the moisture corrosion and dielectric loss are the dominant wear-out failure mechanisms (SUN et al., 2013).

In order to search for a model to evaluate reliability, some works have proposed models for capacitors lifetime prediction. The most widely used empirical model derived from the Arrhenius equation is shown in (2.4), which describes the influence of temperature and voltage stress (WANG; BLAABJERG, 2014).

$$LT = L_{T0}\left(\frac{V_a}{V_r}\right)^{-n} \exp\left[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T}-\frac{1}{T_0}\right)\right], \tag{2.4}$$

in which LT is the lifetime estimation; L_{T0} is the base lifetime (under the testing condition); V_a is the applied voltage; V_r is the rated voltage; T and T_0 are the temperature in kelvin at use condition and test condition, respectively; E_a is the activation energy; K_B is Boltzmann's constant ($8.62{\cdot}10^{-5}$ eV/K); and n is the voltage stress exponent.

For electrolytic and film capacitors, a simplified model from (2.4) was discussed in Parler e Dubilier (2004), in which the activation energy was considered 0.94 eV, and is given by

$$LT = L_{T0}\left(\frac{V_a}{V_r}\right)^{-n} 2^{\frac{T_0-T}{10}}. \tag{2.5}$$

The value of exponent n is from around 7 to 9.4 for MPPF-Caps (POWER, 2008). For Al-Caps, the value of n is between 3 and 5 (ALBERTSEN, 2010). This shows that the lifetime is more impacted by voltage in Al-Caps when compared to MPPF-Caps.

It can be highlighted that the lifetime prediction model does not yet explicitly take into account the value of the capacitance. The conventional lifetime estimation was improved in Wang et al. (2019), which proposes a nonlinear accumulated damage model for the long-term estimation, considering the nonlinear process of equivalent series resistance (ESR) growth and capacitance reduction during the degradation. However, this analysis can not be generalized for different capacitance values and applications.

As previously mentioned, capacitors are susceptible to random failures even within their lifetime. These catastrophic events are typically described in terms of Failures in Time (FIT). According to Harms (2010), the estimated failure rate λ_f can be given by (2.6), which represents the number of failures for every million hours of operation.

$$\lambda_f = \lambda_b \pi_T \pi_V \pi_C \pi_Q \pi_E, \tag{2.6}$$

where:

λ_b - base lifetime, which assumes a different value for each capacitor technology and can be obtained in (HARMS, 2010).

π_T - temperature factor, defined in (2.7) for devices with ratings lower than 150 ^{o}C in which T_a is the capacitor ambient temperature.

π_V - voltage stress factor, defined in (2.8), which is a function of the rated voltage V_r and the maximum applied voltage $V_{C\max}$ (the ripple must be taken into account);

π_C - capacitance factor, calculated from the capacitance using (2.9). The values of the constants λ_b, E_a from (2.7) and k from (2.9) have different values for each capacitor technology. The values of these paramters for MPPF-Caps and for Al-Caps are shown in Table 2.1;

π_Q - quality factor, which is related to quality of the component (informed by the manufacturer). These values can be found in Harms (2010). the value of this factor is 3 for Non-Established Reliability capacitors;

π_E - environment factor, which also can be found in Harms (2010). For fixed ground environment, the value is 1.

$$\pi_T = \exp\left[\frac{-E_a}{K_B}\left(\frac{1}{T_a + 273} - \frac{1}{298}\right)\right], \tag{2.7}$$

$$\pi_V = \left[\left(\frac{V_{C\max}}{0.6V_r}\right)^5 + 1\right], \tag{2.8}$$

$$\pi_C = C^k. \tag{2.9}$$

Table 2.1 – Failure prediction model parameters for MPPF-Caps and Al-Caps.

Parameter	MPPF-Caps	Al-Caps
λ_b	0.00051	0.00012
E_a	0.15	0.35
k_1	0.09	0.23

Based on the equations aforementioned, the reliability of the capacitors is greatly impacted by the voltage (2.8) and the temperature (2.7). The oversizing of the element can improve the reliability of the capacitor, but this strategy leads to a higher cost and volume. Another important factor of capacitor reliability is its capacitance. As shown in (2.9), the number of failures in time (FIT) can be dramatically reduced with a capacitance reduction. This behavior has been illustrated in Soares (2017) by plotting the values of FIT as a function of capacitance for MPPF-Caps and Al-Caps, as shown in Figure 2.2, which was obtained considering a voltage derating of 10% ($V_{C\max}/V_r = 0.9$) and an ambient temperature of 80 ^{o}C.

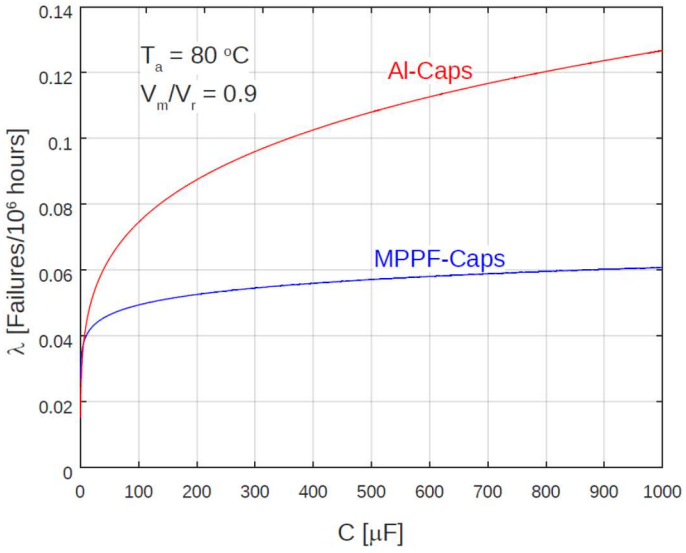


Figure 2.2 – Behavior of the FIT as a function of the capacitance for the MPPF-Caps and Al-Caps (SOARES, 2017).

2.1.2 **Power density**

Another important topic that should be addressed in capacitors is power density. Along with the magnetic elements, storage capacitors are the crucial elements when the power density of the circuit is investigated. Sometimes, the application can limit the range of possible technologies, mainly in cases where the available space is limited, such as LED bulbs.

The power density of some capacitor technologies has been discussed in März et al. (2010). This work showed that the power density of the capacitor depends mostly on the relative permittivity and the operating field strength of the dielectric material. Figure 2.3 shows the energy storage density of some dielectrics. MPPF-Caps, which are based on polypropylene dielectric, can reach an energy storage density of 0.2 J/cm^3 whereas Al-Caps, which are based on aluminum oxide (Al_2O_3), can achieve 2 J/cm^3. Therefore, Al-Caps have a high-performance dielectric that allows for an energy storage density about ten times higher than that of MPPF-Caps.

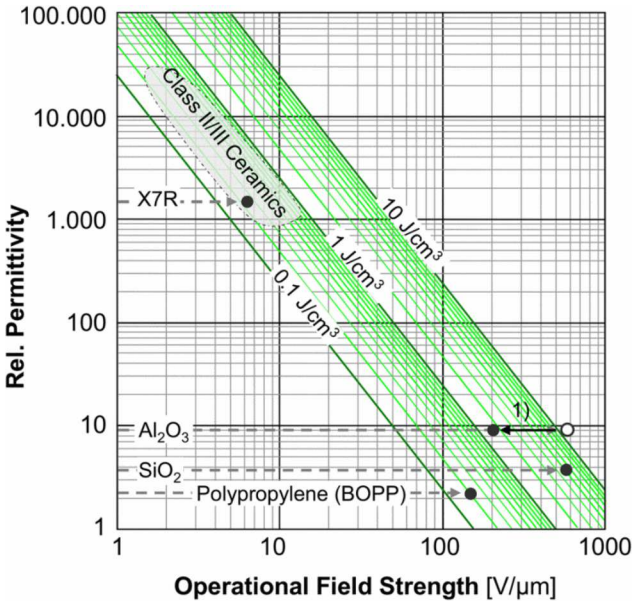


Figure 2.3 – Energy storage density for several dielectric materials (MäRZ et al., 2010).

Raggl, Nussbaumer e Kolar (2010), Heldwein e Kolar (2007), Barruel, Schanen e Retiere (2004) investigated passive component volume calculations in order to achieve volume, size, and cost reduction. According to Raggl, Nussbaumer e Kolar (2010), the capacitor volume scales with the stored energy plus a constant offset factor, which is also dependent on the voltage, and can be written as:

$$\text{vol}_C = k_{c1} C V_r^2 + k_{c2}(V_r), \tag{2.10}$$

where the factor k_{c1} describes the proportionality of the capacitor volume and the stored energy, and k_{c2} is a voltage dependent factor. These factors can be calculated from manufacturer's data for different capacitance values, and voltage ratings V_r.

The boxed volume was calculated from the dimensions obtained in the datasheet for the following capacitor series: LGN (NICHICON, 2011a), UCY (NICHICON, 2011b), F611 (KEMET, 2021), and MKP1848C (VISHAY, 2022). Figure 2.4

shows the boxed volume function of these capacitors according to the capacitance values for the Al-Caps and MPPF-Caps together with the constant factors k_{c1} and k_{c2}, which were evaluated for a voltage rating of 250 V (figure 2.4a) and 500 V (figure 2.4b). As can be noted in the picture, the volume of the film technology is considerably larger than the volume of capacitors that use aluminum oxide as the dielectric material. Moreover, the volume of the capacitors grows as the voltage rating increases.

Since the capacitors contribute to cost, size and failure of power electronic

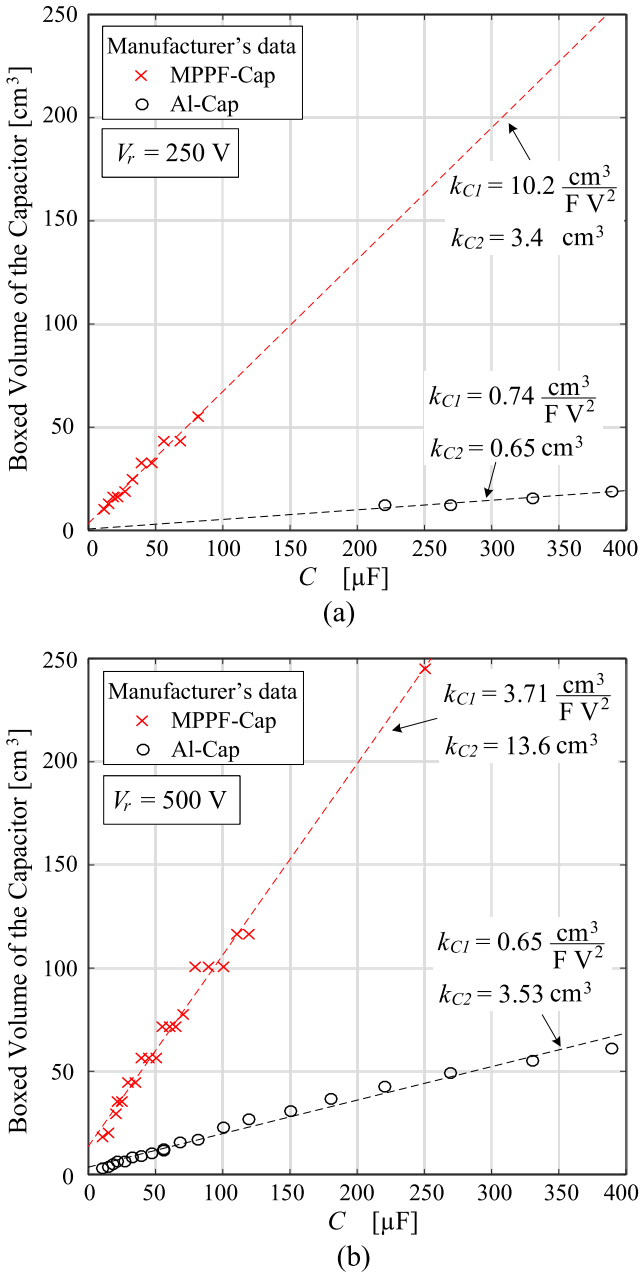


Figure 2.4 – Boxed volume of the capacitor according to the capacitance values for the Al-Caps and MPPF-Caps. Voltage rating of (a) 250 V and (b) 500 V.

converters on a considerable scale (PELLETIER et al., 2009), research efforts have been devoted to either the optimal design of dc-link capacitor (WANG; CHUNG; LIU, 2014) or to the reduction of the dc-link requirement (WANG; LISERRE; BLAABJERG, 2013).

2.2 OFF-LINE LED DRIVERS WITH REDUCED CAPACITANCE

This section investigates off-line converters with reduced capacitance since this class of converters tends to achieve better performance in terms of reliability, cost savings and power density. Thus, the investigation of off-line converters with reduced capacitance can provide interesting insights for conceiving a high-performance off-line LED driver.

Active single-stage off-line solutions are often used in off-line LED drivers because of their low cost and simplicity (LAMAR et al., 2017; CHENG et al., 2019; LAMAR et al., 2009; HWU; YAU; LEE, 2011). However, these converters usually require a high capacitance and a universal input solution can be difficult to be achieved (CASTRO et al., 2019). In order to attenuate the low-frequency ripple, multi-stage converters have been used as off-line LED drivers.

2.2.1 **Multi-stage converters**

In general, the capacitance reduction is performed by a second or more stage that compensates the LF ripple of the bus voltage in order to attain a desirable LF ripple in the LED current. The use of two-stage LED drivers based on cascade connection has been extensively related in the literature. These topologies are composed of a power control (PC) stage connected at the output of the power factor correction (PFC) stage and can be defined as converters with independent stages (FERRAZ et al., 2021; PERVAIZ; KUMAR; AFRIDI, 2018; WANG et al., 2016b; CASTRO et al., 2019) or with integrated stages (BRAND et al., 2021; ABDELMESSIH et al., 2020; ALMEIDA; SOARES; BRAGA, 2013; ALONSO et al., 2012; GACIO et al., 2011; ALMEIDA et al., 2015b).

Figure 2.5 shows the difference between the aforementioned approaches. The strategy that relies on independent converters (Figure 2.5a) requires two control loops, one for each stage that is designed for only one function, increasing flexibility for some applications. Regarding the losses, there is not a major difference between the efficiency of non-integrated and integrated converters if the PFC and the PC stages are designed with the same switching frequency (FRAYTAG et al., 2015). The integrated strategy illustrated in Figure 2.5b, in which the PFC and PC stages are integrated into a single-active-switch topology, has only one control loop. This removal of one control variable,

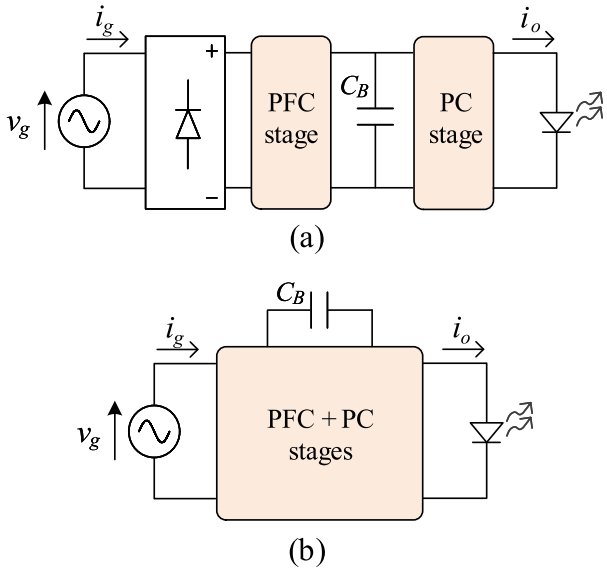


Figure 2.5 – Two-stage converters: (a) with independent stages; (b) with integrated stages.

i.e. of one degree of freedom of the converter, reduces design flexibility. On the other hand, the complexity of the control and the total number of components is reduced, thus reducing the cost.

Other converters that can be considered within the multi-stage category are bidirectional dc–dc converters in parallel with the LEDs (FANG et al., 2019; HE; RUAN; ZHANG, 2017; YANG et al., 2014; WANG et al., 2012) or the ones based on multi-output ripple cancellation (CAMPONOGARA et al., 2015; SHAN et al., 2019; VALIPOUR; REZAZADEH; ZOLGHADRI, 2016; DONG et al., 2018; CAMPONOGARA et al., 2013). The first strategy is shown in Figure 2.6a, where the bidirectional converter handles the pulsating power of C_B consequently reducing its size - trading capacitance for voltage. It can be noted that, unlike the two-stage converters based on cascade connection, the parallel converter with a capacitor does not process all the power. A similar principle is applied in the multi-output voltage ripple cancellation solution shown in Figure 2.6b. In this strategy, in order to reduce its size and value, a certain voltage ripple is allowed on C_B to be compensated by the dc-dc converter, which delivers its output voltage out of phase with the ac portion of the output voltage of the PFC stage. Since part of the energy delivered to the load must be processed by both stages, the efficiency of the theses multi-stage solutions can be improved in some cases. For example, an efficiency of 91% and 94% were reported in Camponogara et al. (2015) and Camponogara et al. (2013), respectively. Therefore, converters with reduced energy processing often achieve high efficiency at the cost of complex control, high component count, and low bandwidth on the output current feedback loop.

As already mentioned, the use of a two-stage driver based on cascade connec-

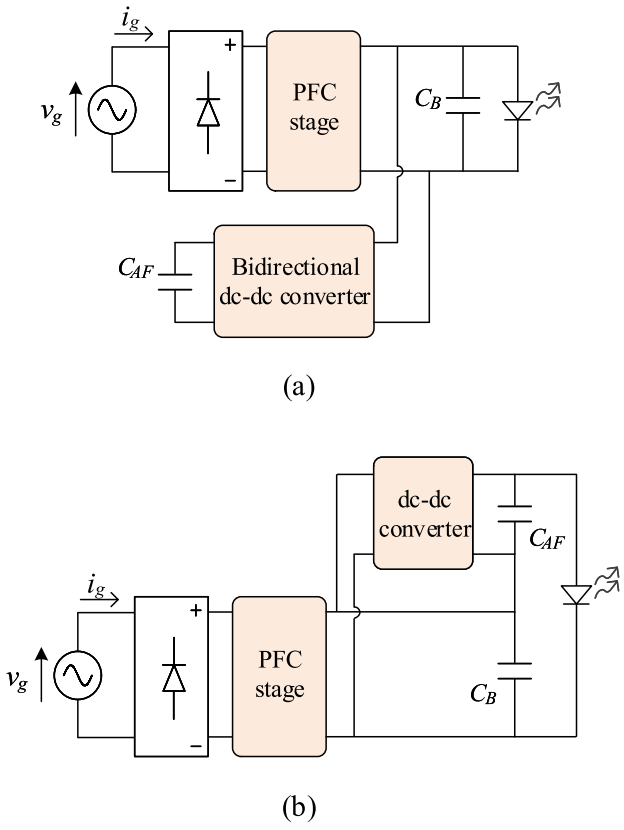


Figure 2.6 – Multi-stage solutions with reduced energy processing: (a) bidirectional dc–dc converter ; (b) multi-output voltage ripple cancellation (CASTRO et al., 2019).

tion allows for the use of lower capacitances (see Figure 2.5). In addition, integrated converters reduce control complexity and the number of components, thus reducing system cost. One of the drawbacks of the cascade connection of two basic topologies is that the overall efficiency of the drivers is limited and rarely is greater than 90% (ALMEIDA; SOARES; BRAGA, 2013; ALONSO et al., 2012).

In order to overcome this problem, the use of resonant converters can be emphasized. Some works have proposed off-line LED drivers based on resonant converters, which are typically employed as the PC stage (ALMEIDA et al., 2013a; MA et al., 2016; WANG et al., 2018; WANG et al., 2015a). All of these works reported an overall efficiency higher than 90%. Since this class of drivers is an important research topic, resonant converters will be discussed in further detail in Section 2.3.

Regarding the capacitance reduction, Alonso et al. (2012) shows that the output current ripple can be attenuated by reducing the ripple in the bus voltage or by reducing the voltage ripple transformation factor, i.e. the low-frequency ripple transmission. The reduction of the ripple in the bus can be done by increasing the filtering capacitance or by increasing the bus voltage (ALONSO et al., 2012). Alternatively, the LED current

ripple can be reduced by choosing a PC stage with a lower ripple transmission.

Alonso et al. (2012) evaluated the natural voltage ripple transmission on a buck, forward, buck-boost, and flyback converters operating in CCM or DCM as PC stage, showing that the second stage attenuates the low-frequency ripple indeed. The analysis of the low-frequency ripple transferred from the bus voltage to the LED current also has been investigated in Brand et al. (2021) for a buck, boost, and buck-boost converter operating in DCM. Since resonant converters can improve the overall efficiency, the analysis of the LF ripple transmission in resonant converters has been addressed in some works (FERRAZ et al., 2021; MELO et al., 2015b; ALMEIDA et al., 2013a; MELO et al., 2015c; MELO et al., 2015a), which show that resonant converters are a good alternative for reducing the bulk capacitance.

2.2.2 **Harmonic current injection**

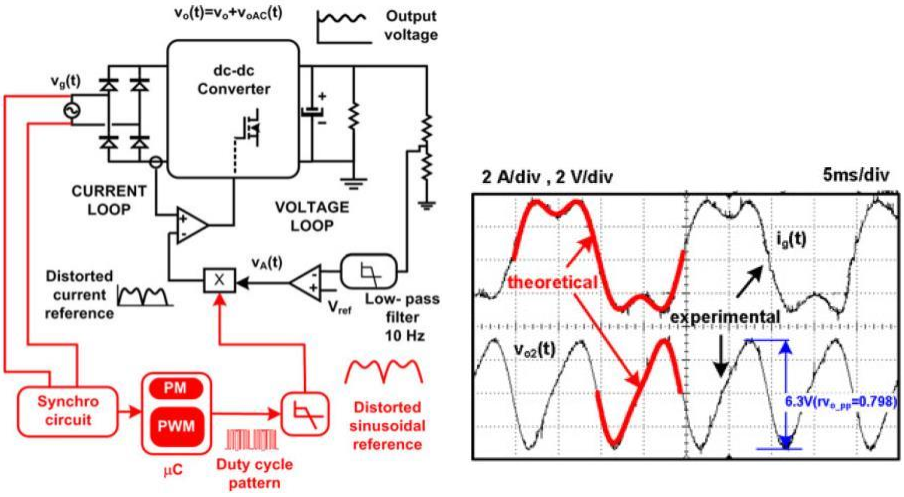
As mentioned in section 2.1, the power imbalance between the input and output of the converter causes an output ripple in the PFC pre-regulators. Considering a unity power factor PFC pre-regulator, the instantaneous input power can be described by (2.11), in which ω_L is the angular frequency of the line, V_G and I_G are the RMS values of the line voltage, and current, respectively.

$$P_g(t) = v_g(t)i_g(t) = V_G I_G - V_G I_G \cos(2\omega_L t). \tag{2.11}$$

Thus, the input power has an average value and an ac oscillating portion, which is the main cause of the low-frequency ripple in off-line converters (SOARES, 2017). In order to reduce the amplitude of the ac portion, and therefore reduce the output current ripple, some works have proposed a harmonic current injection method (WONG et al., 2016). Those techniques rely on the deliberated distortion of the input current by injecting harmonic components. Some works included a certain amount of third (GU et al., 2009; WONG et al., 2016) and fifth (WANG et al., 2010; RUAN et al., 2011) harmonics by modifying the standard control loop of a current-mode controlled PFC converter in order to provide a non-sinusoidal reference for the input current.

A similar strategy has been evaluated in Lamar et al. (2012), which takes into account the harmonic injection limits imposed by the IEC-61000-3-2 standard (IEC, 2018) to generate the reference for the input current, and thus achieve better FP at the cost of lower ripple reduction. Figure 2.7 shows the circuit proposed in Lamar et al. (2012) (Figure 2.7a) and its experimental result (Figure 2.7b). In this case, a 20.2% of output voltage ripple reduction was obtained (from 8 to 6.3 V). As can be observed, this approach is a trade-off between the increase in the THD of the input current and the reduction of the output low-frequency ripple. In addition, two control loops are

needed and the complexity of the control structure is increased when compared to the conventional current-control mode.



(a) (b)

Figure 2.7 – (a) Off-line converter with harmonic injection and (b) its experimental result: Input current and output voltage ripple for a Class C design (LAMAR et al., 2012).

In Luz et al. (2018), the resonant proportional integral (RPI) controller has been applied to reduce the bus capacitance value of the Integrated Double Buck-Boost Converter (IDBB). This controller has an infinite theoretical gain at 120 Hz, implying a low current error compared to the ac portion of the current reference. Another compensation method, called active ripple compensation (ARC) technique, has also been proposed in Soares et al. (2017), Soares, Alonso e Braga (2018), Soares et al. (2018) and applied to integrated off-line LED drivers. This approach allows for current ripple reduction by means of a proper modulation of the converter duty-cycle, which will be discussed in further detail in section 4.1. In general, capacitance reduction occurs because an active compensation technique mitigates the transmission of low-frequency ripple, thus allowing for a higher voltage ripple in the bus. Therefore, a higher voltage ripple implies the use of a lower capacitance value.

It is important to highlight that the modulation of the control variable generates distortions in the input current in integrated off-line converters since they use only one control signal to drive two stages. On the other hand, this worsening of the ac input power quality does not occur in converters with independent stages, but they are more expensive. Therefore, converters with capacitance reduction techniques exhibit a trade-off between cost increase and power quality degradation. Figure 2.8 shows the comparison of the typical performance of LED drivers with and without compensation techniques for capacitance reduction, highlighting their impact on integrated and non-integrated converters.

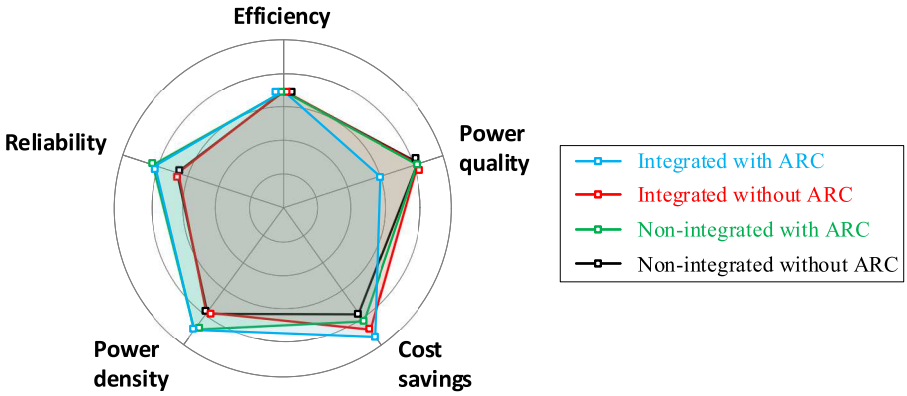


Figure 2.8 – Typical performance analysis of non-integrated and integrated hard-switching converters with and without compensation techniques for capacitance reduction.

2.3 OFF-LINE LED DRIVER BASED ON RESONANT CONVERTERS

The previous sections introduced converters with reduced capacitance and how their characteristics and elements are correlated with four performance indexes: reliability, power density, cost savings and power quality. It is worth mentioning that the high-performance LED drivers also aim for high overall efficiency. Thus, this section investigates LED drivers based on resonant converters for efficiency improvement.

In general, the semiconductor losses are dominant in total losses under hard-switching applications at higher frequencies (LIDOW et al., 2019). Since switches are not ideal, there are two main types of losses in power semiconductors: conduction and switching losses. Figure 2.9a shows a typical hard-switching current, and voltage waveforms. In the conduction range of the switch, the power semiconductor presents a non-zero voltage between its terminals, thus resulting in conduction losses. On the other hand, during on-off transitions (time intervals represented by t_{on} and t_{off}), the device is subjected to both voltage and current at the same time, causing switching losses. The values of t_{on} and t_{off} depend on the device and practically do not change with the switching frequency modifications. However, on-off transitions occur more often with increasing switching frequency, i.e., greater switching frequencies result in higher switching losses. Thus, such losses may be more relevant than conduction losses when the switching frequency is very high (PAULA et al., 2018).

High efficiency and operation at high frequencies, which increase the power density of the converter, can be achieved by employing resonant converters. In these circuits, switching occurs when the voltage and/or current is theoretically zero (called soft-switching). Thus, simultaneous voltage and current transitions are avoided, mitigating switching losses. Soft-switching is classified according to the way the transitions are performed: zero voltage switching (ZVS), which is shown in Figure 2.9b or zero cur-

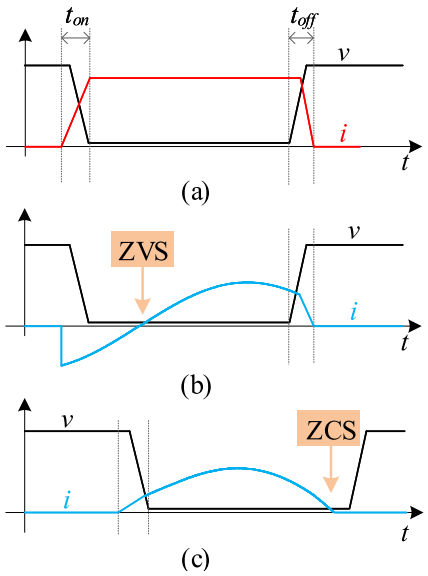


Figure 2.9 – Example of operation waveforms in semiconductors. (a) hard-switching in PWM converters; soft-switching in resonant converters: (b) ZVS and (c) ZCS.

rent switching (ZCS), which is illustrated in Figure 2.9c (ERICKSON; MAKSIMOVIC, 2007).

Therefore, by means of soft-switching, resonant converters can reduce the switching losses since switching devices turn on and off at zero or nearly zero voltage or current. This feature also reduces the electromagnetic interference of the converter, which requires a lower EMI filter. Furthermore, the improved efficiency allows the use of higher frequencies in order to achieve high-power-density converters.

2.3.1 **The basic structure of resonant converters as a PC stage**

The main types of resonant converters are resonant switch, resonant load, and resonant dc link. In this paper, the resonant load converters are evaluated since they do not require any type of active clamping circuit or auxiliary static switches to enable the soft switching of the main circuit switches. Therefore, they are the simplest resonant converter structures (ALMEIDA, 2014) and are typically used as a PC stage in off-line LED drivers (see Figure 2.5). The soft-switching is achieved by means of a high-frequency inverter circuit associated with a resonant filter (also known as a resonant tank) and a high-frequency rectifier, as illustrated in Figure 2.10.

Regarding high-frequency inverters, their typical voltage-supplied topologies for employing resonant converters are shown in Figure 2.11. The push-pull inverter (Figure 2.11a) has a peak voltage on the MOSFETs equal to twice the input voltage and therefore is used in applications where the dc input voltage is low (typically 12 to 24 V) and the current high, up to 150 A (RYAN et al., 1998; CHU; LI, 2009). Therefore,

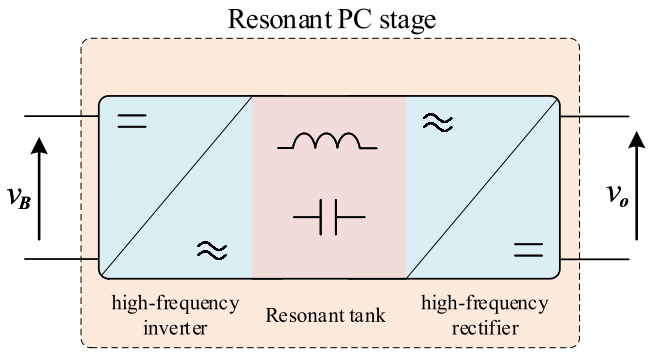


Figure 2.10 – The basic structure of the resonant converter as a PC stage in off-line LED drivers.

a push-pull inverter is not feasible for a PC stage of LED driving applications since the bus voltage (output of the PFC stage) is usually high. The full-bridge topology shown in Figure 2.11b is widely employed at high power levels and can be applied to LED drivers (FANG et al., 2012). This topology has a higher component count, despite the peak voltage on the MOSFETs being equal to half the input voltage. Figures 2.11c and 2.11d show half-bridge topologies that are simple and have a low component count. They are widely used as a PC stage for LED drivers (MELO et al., 2015b; LAZAR; MARTINELLI, 2001). The half-bridge inverter with an asymmetrical bus has the lowest number of components, though the peak voltage on the MOSFETs is equal to the input voltage.

As already mentioned, resonant converters use a resonant tank connected to the output of the high-frequency inverter. The filters are usually designed for resonance to be close to the switching frequency of the inverters, in order to obtain a quasi-sinusoidal current in the tank and enable the soft switching, reducing losses and improving an overall efficiency even at high frequencies. Current papers report several popular types of resonant converters. The topologies commonly used in the resonant tank are LC series, LC parallel, LCC series-parallel, and LLC series-parallel which are depicted in Figures 2.12a, 2.12b, 2.12c, and 2.12d, respectively. The choice of the circuit for each case relates to the characteristics of the load and the input voltage, which is dependent on the PFC circuit.

Regarding the high-frequency rectifiers, the full-bridge topology is widely used in converters without galvanic isolation thanks to its simplicity. However, this topology has a lower efficiency because there are always two diodes conducting at any instant of operation. Another more efficient structure, which is widely used in converters with galvanic isolation, is the rectifier with two diodes from a high-frequency transformer with a center tap.

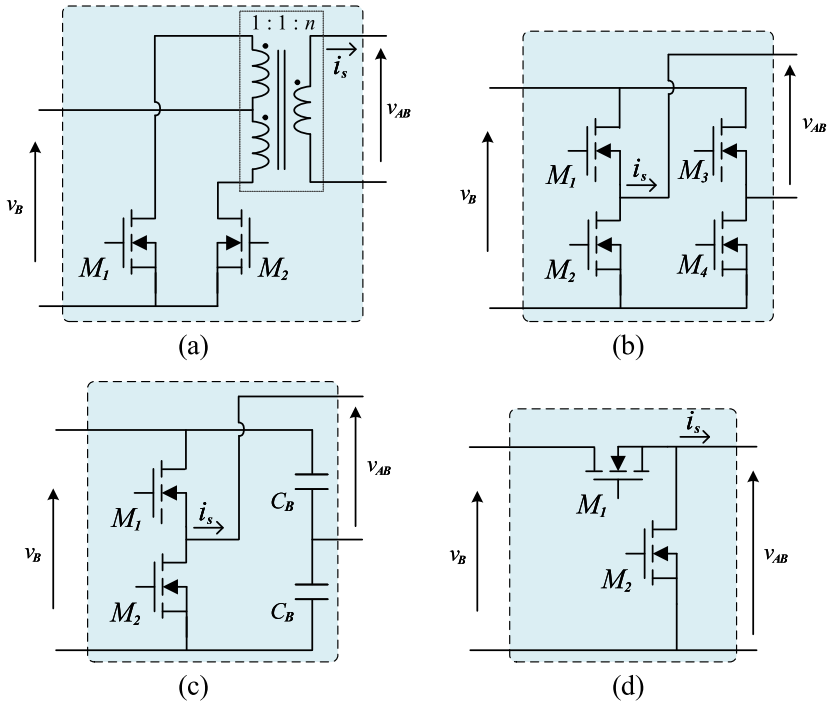


Figure 2.11 – High-frequency inverter topologies for resonant converter applications: (a) push-pull inverter; (b) full-bridge inverter; (c) half-bridge inverter with an symmetrical bus; (d) half-bridge inverter with an asymmetrical bus.

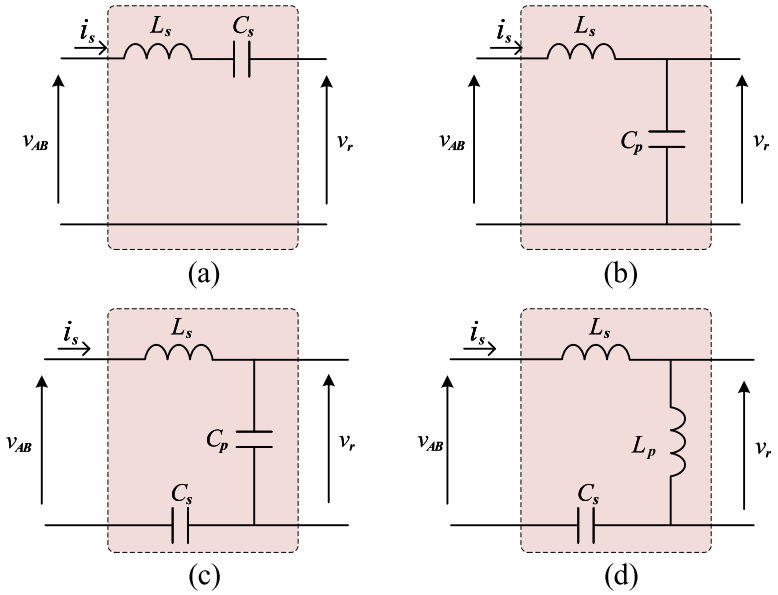


Figure 2.12 – Some resonant tank topologies: (a) LC series, (b) LC parallel, (c) LCC series-parallel e (d) LLC series-parallel.

2.3.2 **Resonant two-stage converters with independent stages**

When galvanic isolation is required, this is usually performed by the second stage of the converter. Therefore, non-isolated PFC topologies can be used as PFC stages. Among the main topologies applied to single-phase voltage-mode controlled power factor pre-regulators, the boost PFC pre-regulator operating in DCM mode is a common choice for this role, particularly for its high efficiency (MA et al., 2018a; Kim et al., 2013). Regarding the PC stage, the LLC resonant converters are quite popular in industrial electronics and LED driving applications, owing to the advantages of high efficiency, high power density, galvanic isolation, wide output ranges, low voltage stress, and high operation frequency (ZENG et al., 2020; XIE et al., 2007). Therefore, the most common topology in the literature is the two-stage Boost-LLC converter (WANG et al., 2015b; ZHANG; JIANG; WU, 2017; FERRAZ et al., 2021; MA et al., 2018b).

There are several methods of controlling the output current in resonant converters, which can be used in the PC stage according to the application, the inverter topology, and the converter design specifications, such as the input voltage range, load, frequency, etc. As already mentioned, for the case of off-line converters with independent stages (Figure 2.5), the control schemes used in resonant converters only affect the behavior of the PC stage, which can be analyzed individually.

The control scheme typically used in resonant converters with the half-bridge inverter is the pulse frequency modulation (PFM) (BEIRANVAND et al., 2011; BEIRANVAND et al., 2012; FANG et al., 2013; FENG; LEE; MATTAVELLI, 2014; FANG et al., 2018; IVENSKY; BRONSHTEIN; ABRAMOVITZ, 2011; LIU et al., 2017; XIE et al., 2007; FANG et al., 2012; MENKE et al., 2020; FERRAZ et al., 2021). Figure 2.13 shows the waveforms of the PFM scheme and its control loop. The waveform applied at the input of the resonant tank (v_{AB}) is square with D=0.5 and the output voltage regulation is obtained by modulating the switching frequency. This control scheme is the most widely used due to its simplicity and low cost (CHENG et al., 2015; ZHANG et al., 2020). The analog implementation of this control loop can be easily achieved using a resonant controller, such as L6599, which inserts a fixed deadtime between the turn-off of one switch and the turn-on of the other in order to guarantee soft-switching and enables high-frequency operation (MA et al., 2016).

In the case of resonant converters, the circuit gain reduces as long as the amplitude of the switching frequency increases. On the other hand, the resonant converter is designed to operate near the resonant frequency under the full-load condition in order to achieve the best efficiency. Since the gain of the converter becomes flat as frequency increases, the PFM control has difficulty operating with dimming. In other words, when the LED dimming ratio becomes high, it comes to the light-load condition with a very high switching frequency, which increases dramatically the switching

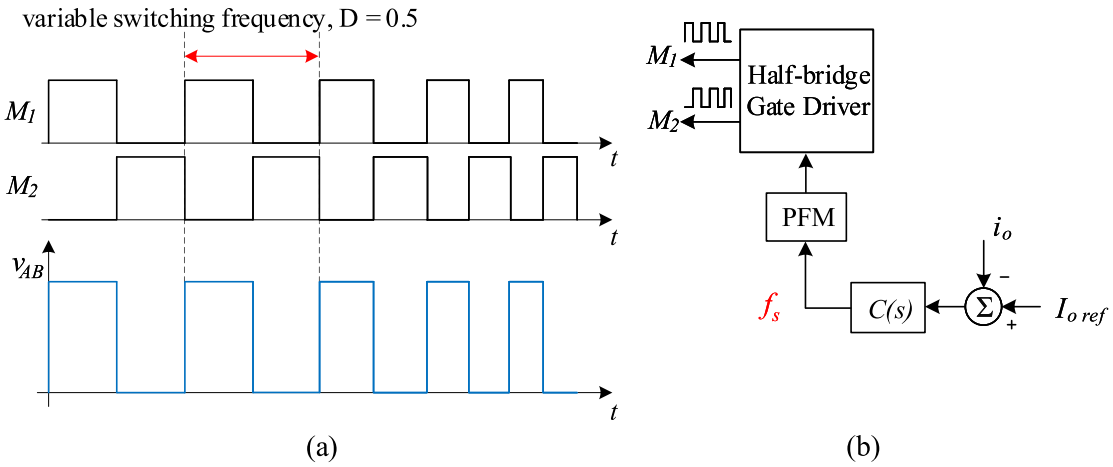


Figure 2.13 – (a) Pulse frequency modulation (PFM) and its (b) control loop.

loss, reducing the efficiency. Feng, Lee e Mattavelli (2014) showed that, for the LLC converter, only 15% full load dimming was achieved when the switching frequency has increased ten times. This case is depicted in Figure 2.14. It is important to highlight that this problem also occurs for applications with a wide range of bus voltage variations. Therefore, the switching frequency range can increase, i.e. efficiency can be lower, for resonant converters operating in wide input- and/or output-voltage range with the PFM approach.

Some works have used burst-mode control to improve the light-load efficiency (ZHAO et al., 2022; FEI; LI; LEE, 2018; FENG; LEE; MATTAVELLI, 2014; FENG; LEE; MATTAVELLI, 2013; DWELLEY, 2001). The concept of burst mode is to switch the converter between ON and OFF mode. During the burst-ON, the LLC converter operates at the peak-efficiency condition. While during the burst-OFF time, the LLC converter is not operating, and the output power is zero (ZHAO et al., 2022). Thus, by

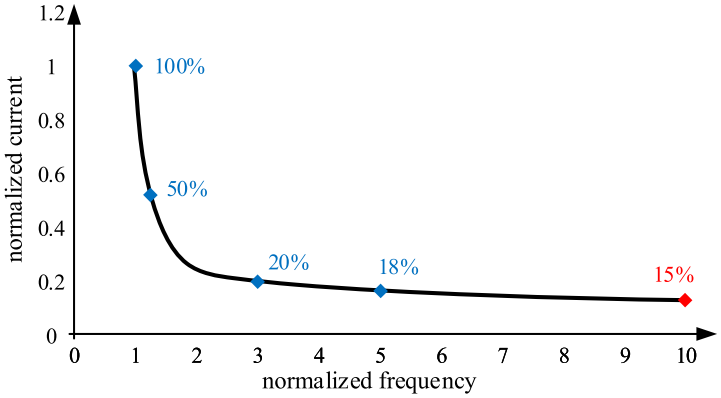


Figure 2.14 – Gain of LLC converter with frequency controlled analog dimming (FENG; LEE; MATTAVELLI, 2014).

periodically blocking the switch-gate driving signals M1 and M2, as shown in Figure 2.15, the average output power can be controlled to regulate the output voltage with high efficiency at low output current levels.

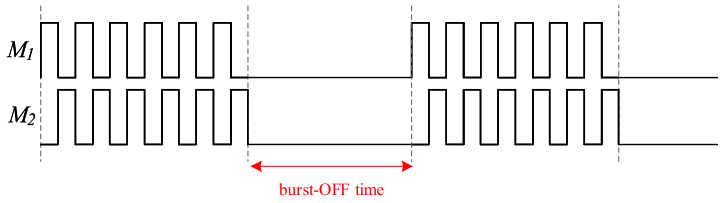


Figure 2.15 – Burst-mode control.

The reduction of the frequency range by decreasing magnetizing inductance was investigated in Fang et al. (2013) and Jovanović e Irving (2016). These works have shown that, with reduced magnetizing inductance, the frequency range is reduced when the converter behaves more like a parallel resonant converter. By using this approach, the gain curve features a higher voltage peak and the converter operates close to it (series-parallel frequency). In addition, Jovanović e Irving (2016) uses the full-bridge inverter in order to further reduce the frequency range, as shown in Figure 2.16. The full-bridge (FB) LLC converter presents a higher gain range when compared to the half-bridge (HB) LLC converter.

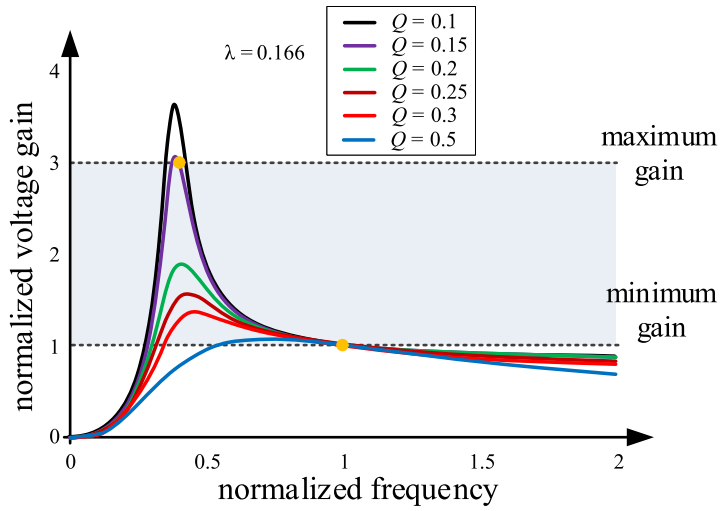


Figure 2.16 – FB LLC converter operating in high gain range (JOVANOVIć; IRVING, 2016).

An additional bus voltage control loop can also be used to reduce the frequency range. In this way, both the wide variation of the input voltage and the dimming are compensated by the PFC stage. This alternative allows for a lower frequency range at the cost of increasing the complexity of the control system.

Another control scheme found in the literature is asymmetrical pulse width modulation (APWM), which is shown in Figure 2.17. In this case, the switching frequency is fixed and the output regulation is performed by modulating the duty cycle, thus applying an asymmetric square voltage to the input of the resonant tank. As a result of this asymmetric waveform, the resonant topology has a transformer magnetizing current with an average value that is not zero. This implies that the conduction losses in the transformer are higher than in traditionally half-bridge converters controlled by PFM modulation. Therefore, an accurate design of the magnetic element must be performed in order to avoid the core saturation (ARIAS et al., 2012).

The asymmetrical half-bridge converter (AHBC) has been used as the second stage in off-line LED drivers since ZVS can be obtained. Arias et al. (2013) has shown that it is possible to design a feed-forward loop optimized for canceling this low-frequency ripple, while the closed-loop control assures stability and output voltage regulation due to variations in the characteristics of the LEDs, which are determined by their warming-up. This strategy has been simplified and implemented in a digital feed-forward loop (ARIAS et al., 2015). An optimized design guideline was also proposed for the zeta AHB (ZAHB) converter with a similar feed-forward loop in Arias et al. (2018).

Kim, Park e Moon (2012) applies the APWM control scheme during hold-up time for LLC resonant converter, proposing a mixed PFM and APWM control scheme in order to narrow the switching-frequency variation range and achieve high power density. As shown in Figure 2.18a, when the bus voltage is lower than a reference value, the modulation method is changed from PFM to APWM. Figure 2.18b shows that the switching frequency variation range of this approach is lower when compared to the PFM.

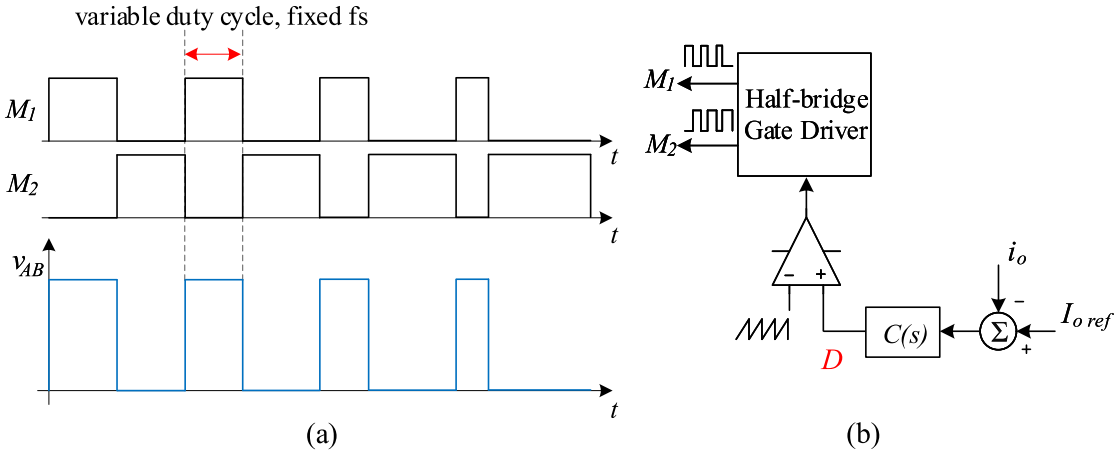


Figure 2.17 – (a) Asymmetrical pulse width modulation (APWM) and its (b) control loop.

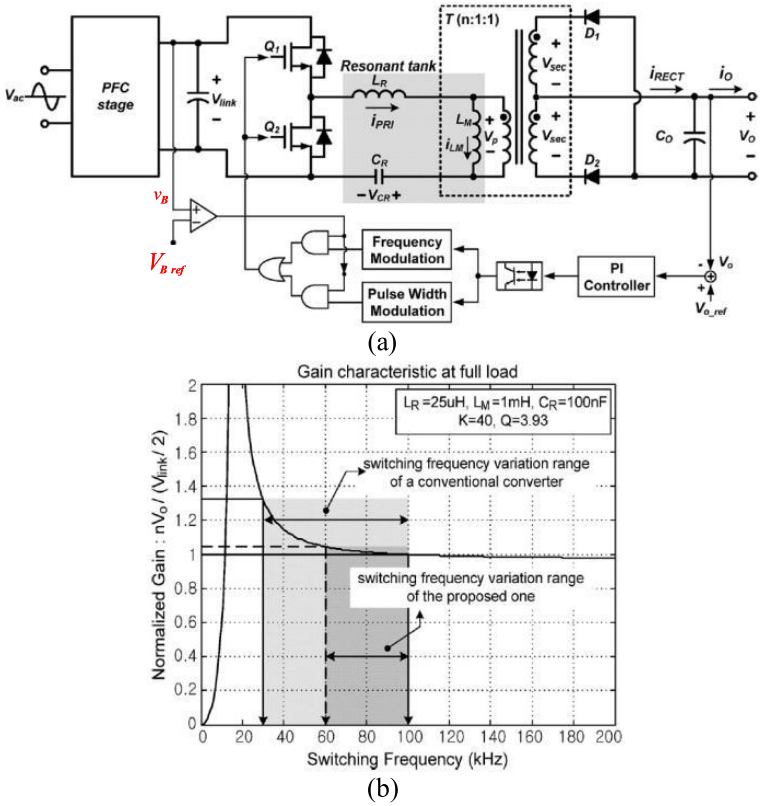


Figure 2.18 – (a) LLC resonant converter with a mixed PFM and APWM control scheme; (b) Gain characteristic of an LLC resonant converter (KIM; PARK; MOON, 2012).

According to the applications, an additional degree of freedom can be required to meet the design specifications. In several applications, both the duty cycle and the switching frequency can be used simultaneously as control variables, as illustrated in Figure 2.19. Thus, the same APWM characteristics are present in v_{AB}, but also with a variation in frequency. Kim, Moon e Moon (2017) proposes this hybrid control scheme for the current balancing of the two-channel LED driver. The total output current is controlled with the frequency modulation, and the duty cycle control is added to obtain the current balancing of each LED channel. As an advantage of the configuration of multi-channel LED drivers, failures in any one string do not affect the other strings. However, the cost and complexity of the driver are increased.

Some work has investigated phase shift modulation (PSM), which can be employed in full-bridge inverters shown in Figure 2.11 (KIM et al., 2016). Each branch of the inverter operates with D=0.5 and with a variable switching frequency. This method uses phase-shifted gate signals between switch legs to generate the resonant tank input voltage, which has a symmetrical waveform with three levels, by setting the effective duty ratio Def as illustrated in Figure 2.20. Since the switching loss can increase under light-load conditions because the switching frequency can conside-

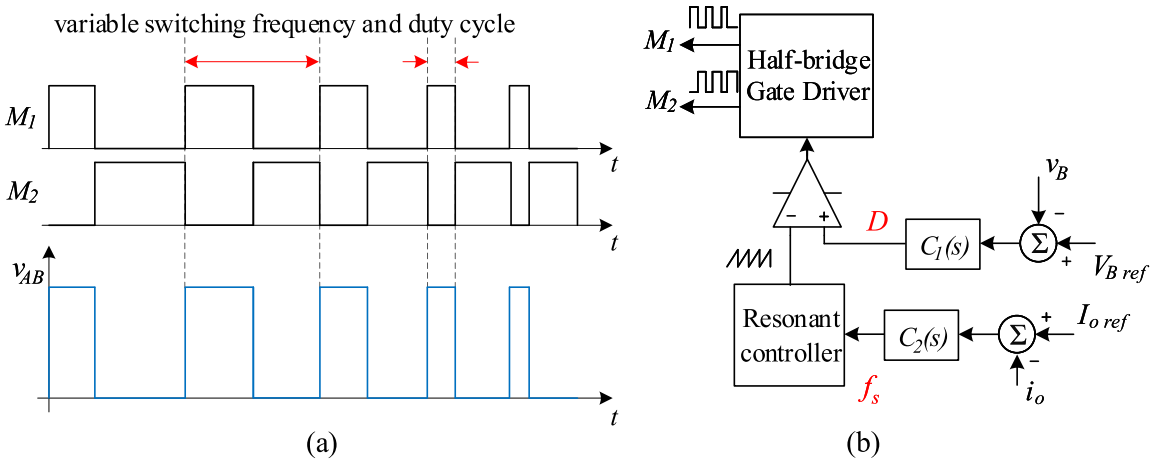


Figure 2.19 – (a) Hybrid control scheme: PFM and APWM; (b) control loops for hybrid control scheme.

rably increase, the phase-shift control was adopted for the FB LLC converter under light-load conditions in Kim et al. (2016), limiting the switching frequency range. In addition, this work evaluates the core loss in magnetic components and designs D_{ef} for the highest efficiency. Besides, PSM has also been used to suppress inrush current during the start-up process (YANG et al., 2016). In other words, during the transient starting process in the LLC converter, the resonant current spike was attenuated by the PSM control. A loss model for an LLC converter with phase-shifted is also discussed in Mumtahina e Wolfs (2018). Based on this model, a cost function was evaluated and returned to the optimization engine in order to minimize the losses. In time-domain analysis, according to different resonant conditions in one switching cycle, LLC can be divided into several stages and its operation can be summarized as different operation

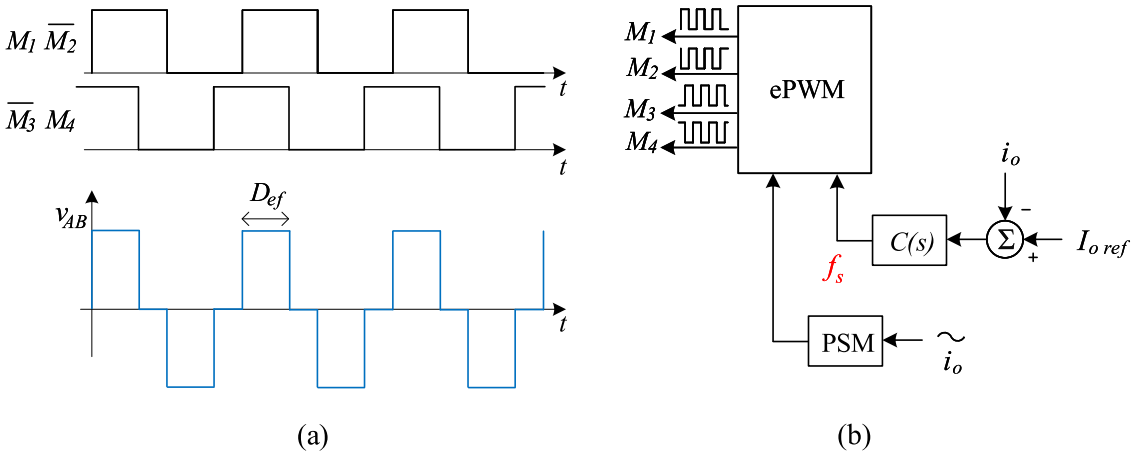


Figure 2.20 – (a) Phase shift modulation used in resonant converters applied to full-bridge inverter and its (b) control loop.

stage trajectories (OSTs). In Xiao et al. (2021), the influence of PSM control was analyzed for each operating mode of the converter and an optimization method was proposed in order to improve the efficiency.

Also in control approaches, some works have focused on the analysis and design of the LLC resonant converter with magnetic control, also called variable inductor control (WEI et al., 2020b; WEI; LUO; MANTOOTH, 2019). As depicted in Figure 2.21, this control scheme has a voltage-controlled current source, which generates a dc bias magnetic flux density inside the magnetic core, thus the material magnetic permeability is adjusted, allowing for the modification of the inductance of the main winding. Therefore, the output voltage is regulated by adjusting the variable inductor value. Since the control variable is the series inductance of the resonant tank, a constant switching frequency and duty cycle can be implemented for the switches, which simplifies the design of the magnetic components. On the other hand, this approach increases the control complexity.

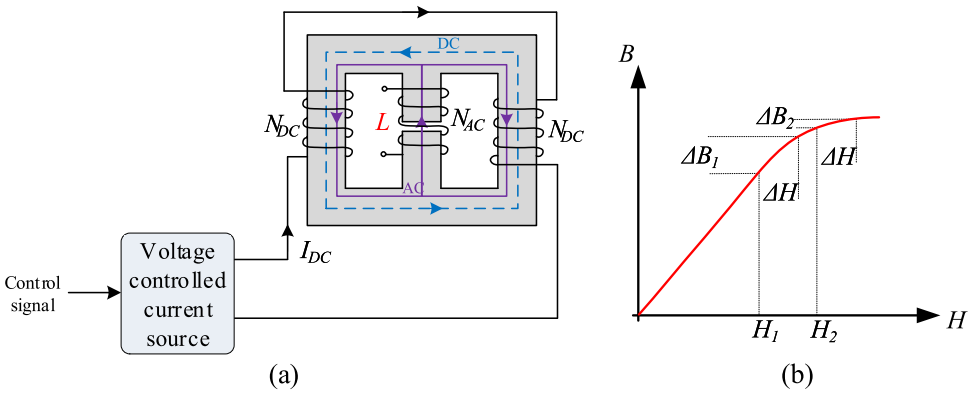


Figure 2.21 – Variable inductor control. (a) Structure; (b) Principle of operation.

2.3.3 **Integrated resonant two-stage converters**

In order to reduce the component count and the driver cost, some works have proposed the use of integrated topologies, which are based on the integration of the PFC and the PC stages (Figure 2.5b). Unlike the off-line LED drivers with independent stages investigated in the previous section, the control schemes used in resonant converters affect the behavior of the PFC stage in LED drivers with integrated stages since both stages share the same switches. In other words, this topology uses only one control signal to drive two converters. Therefore, the topology and control scheme must be taken into consideration when designing the LED driver according to the application.

From the most common topology of off-line LED drivers based on resonant

converters, Lai e Shyu (2007) and Chen, Li e Chen (2012) investigated the converter obtained by integrating a boost PFC pre-regulator and a half-bridge LLC resonant converter, which operates with PFM. This circuit is shown in the Figure 2.22a. The PFC boost operating in DCM to meet the requirements of the IEC 61000-3-2 Class C standard. Since the ZVS operation for the switches can be achieved, this converter has higher efficiency when compared to conventional hard-switching dc-dc converters.

In order to further improve system efficiency, the number of semiconductors in the rectifier can be minimized, and the power losses can be reduced. Thus, a bridgeless off-line converter, which was obtained by integrating a totem-pole bridgeless boost PFC and an HB LLC resonant with PFM control, has been evaluated in Ma et al. (2016), Cheng et al. (2015), Zhang et al. (2020). As can be noted in Figure 2.22b, this topology exhibits simplicity, lower cost, and higher efficiency than the circuit presented in Lai e Shyu (2007) and Chen, Li e Chen (2012).

On the other hand, considering the PFM control in the aforementioned works, the PFC stage operates with a duty cycle of 0.5 and, therefore, the bus voltage has to be at least twice the peak value of the input voltage. Hence, it poses some difficulties to operate in universal-input voltage condition with the 650 V/700 V voltage rating power devices.

The bridgeless structure also was obtained in a converter that integrates a dual buck-boost PFC converter with coupled inductors and an HB LLC resonant converter

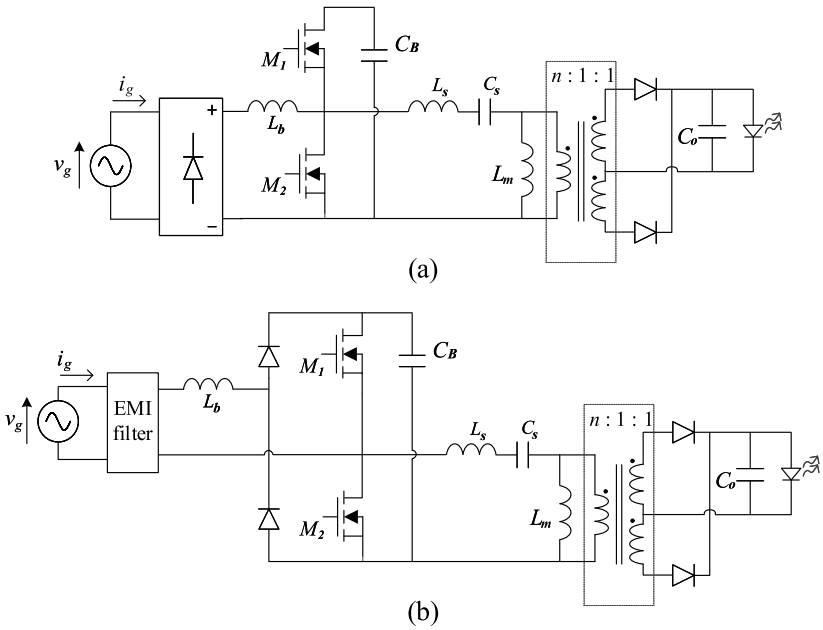


Figure 2.22 – (a) Conventional PFC boost integrating HB LLC converter with PFM control (CHEN; LI; CHEN, 2012); (b) Totem-pole bridgeless PFC boost integrating HB LLC converter with PFM control (ZHANG et al., 2020).

was proposed in Cheng, Cheng e Chung (2014). Two buck-boost circuits operating in DCM were also presented as a PFC stage in Wang et al. (2018), which integrates this PFC and CLCL resonant converter operating with the switching frequency lower than the resonant frequency. Thus, both the ZVS and ZCS characteristics are achieved in the MOSFETs and the secondary-side diodes, respectively, so that the switching loss can be significantly reduced. However, this bridgeless PFC circuit also yields a high bus voltage (the sum of output voltages of the two buck-boost circuits), which is difficult to operate with a high input voltage.

In order to reduce the bus voltage with a duty cycle of 0.5, it is usual to use PFC stage topologies with step-up/step-down characteristics such as the buck-boost or single-ended primary-inductor converter (SEPIC). Chang et al. (2011) proposed an off-line converter consisting of a combination of buck-boost and LLC resonant converter, as shown in Figure 2.23a. In this work, low efficiency of 86% was obtained, mainly because the resonant stage was not well exploited and operates significantly above the resonant frequency with a wide frequency range (60 $\sim$ 250 kHz). In addition, a buck-boost stage is too affected by electromagnetic interference effects, thus a large EMI filter is needed (LI; CHEN, 2012). In contrast, the SEPIC converter has an inductor on the input side, which reduces current ripple and provides inherent input current filtering capability. Therefore, a small EMI filter is required. By integrating a SEPIC PFC and an HB LLC resonant converter, Wang et al. (2017) achieved a converter, presented in Figure 2.23b, with low bus voltage and high efficiency of 92% at full load since primary-side switches operate in ZVS while the secondary-side diodes operate in ZCS mode. In these two topologies, the voltage stress of one of the switches is much higher than the input line voltage peak. As can be seen in Figure 2.23, compared to the two-stage converter with independent stages, the converters require extra diodes but eliminate one switch and one controller.

A low bus voltage has also been obtained in converters operating at high-input-voltage conditions by using interleaved converters as PFC stage (WANG et al., 2013; WANG et al., 2015a; WANG et al., 2019). In these structures, the input voltage is divided and forms two circuits with two half-bridge switches and corresponding diodes, as can be seen in Figure 2.24. A bus voltage of around 1.2 times the peak input voltage has been achieved. The converters based on an interleaved buck-boost PFC have a totally symmetric structure so that the voltage and the current stress caused by the switch integration can be shared completely (WANG et al., 2015a; WANG et al., 2019). However, one boost circuit or buck-boost requires one individual inductor and, in practical use, deviations of the inductor values inevitably occur. Therefore, the two boost circuits (Figure 2.24a) or buck-boost circuits (Figure 2.24b) cannot equally share the input power. In addition, these converters have two inductors, which increased the

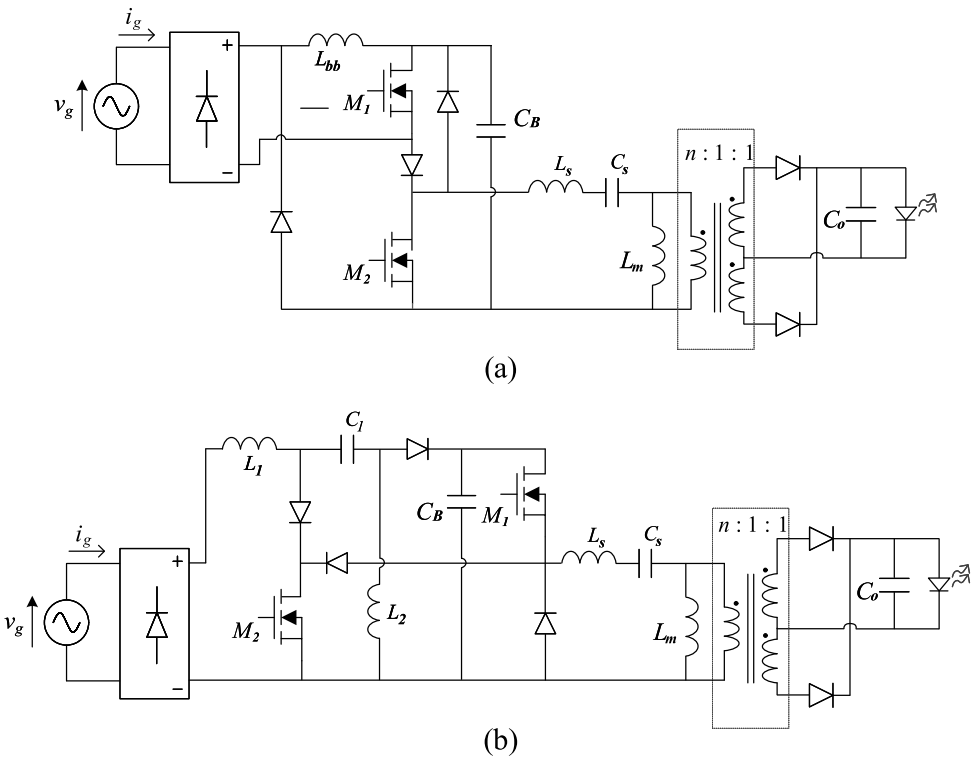


Figure 2.23 – (a) PFC buck-boost integrating HB LLC converter with PFM control (CHANG et al., 2011); (b) PFC SEPIC integrating HB LLC converter with PFM control (WANG et al., 2017).

cost of the system.

The number of inductors of the PFC stage was reduced in Wang et al. (2015b) and Zawawi, Iqbal e Jamil (2016), as can be observed in Figure 2.24c. Two boost circuits that share a single inductor are formed by integrating the switches of an HB LLC resonant converter. Thus, the two switches can equally share the current and voltage stresses since the two boost circuits always work under the same condition as they share one inductor. Moreover, the PFC stage naturally operates in boundary conduction mode (BCM) and performs well under a high input voltage even though the PFM control scheme is used.

The topology formed by the integration between a totem-pole bridgeless PFC boost and a non-isolated HB series resonant with asymmetrical bus, shown in Figure 2.25, has been proposed for high input voltage applications in Almeida et al. (2015b). Since the PFC stage is composed of a boost converter, the APWM control scheme has been used to be feasible in employing a duty cycle lower than 0.5. Thus, the switching frequency is constant and the output current is controlled by the duty cycle modulation (<0.5), which reduces the PFC stage gain and consequently the bus voltage. On the other hand, since this converter uses a bridgeless structure and operates with a variable

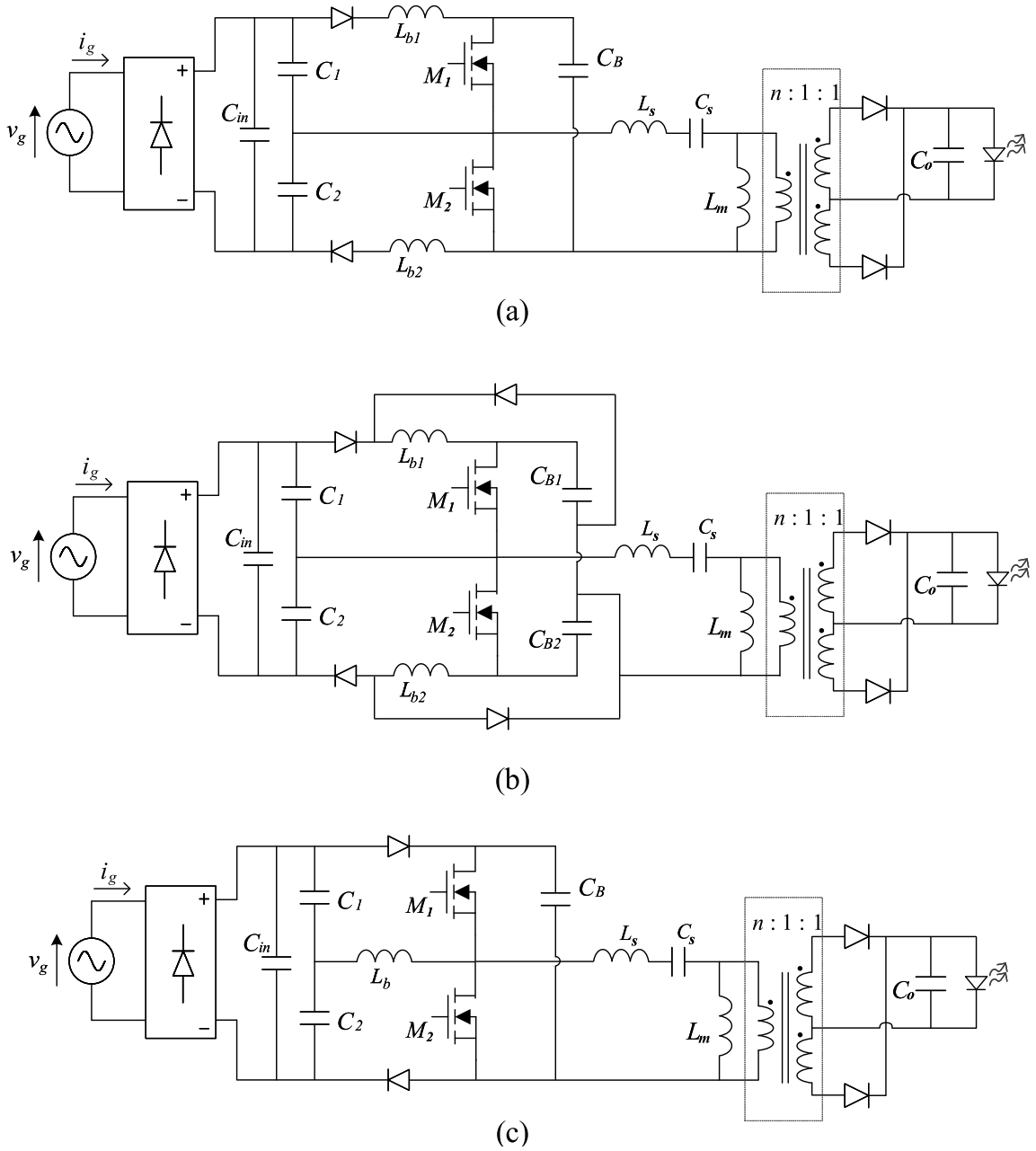


Figure 2.24 – (a) Interleaved boost PFC integrating HB LLC converter with PFM control (WANG et al., 2013); (b) Interleaved buck-boost PFC integrating HB LLC converter with PFM control (WANG et al., 2015a); (c) Two BCM boost PFC integrating HB LLC converter with PFM control (WANG et al., 2015b).

duty cycle as the control parameter, an additional synchronism circuit is required in order to achieve power factor correction, thus increasing the complexity of the control and driving of MOSFETs.

In order to achieve a converter that performs well under universal-input voltage, a PFM-APWM control has been proposed in (MA et al., 2017; MA et al., 2018a; YI

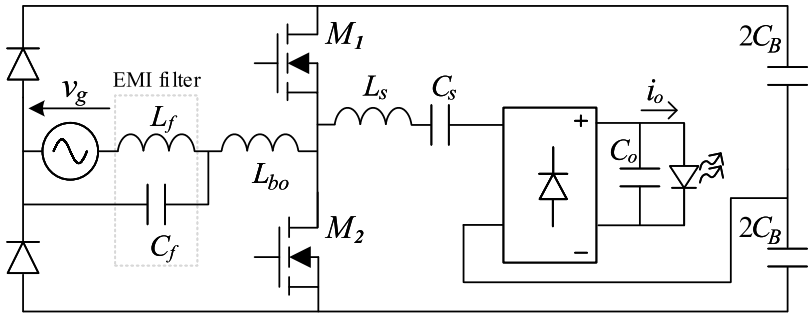


Figure 2.25 – Integration between a totem-pole bridgeless boost PFC and a half-bridge LC series resonant for LED driving (ALMEIDA et al., 2015b).

et al., 2021). The hybrid control of the aforementioned works is composed of two closed loops, one is the PFM-based output voltage feedback loop, which regulates the output power, and the other is the APWM-based bus voltage feedback loop. By setting the suitable maximum bus voltage as a reference and by limiting the duty cycle value to 0.5, the bus voltage control loop is not activated under low input voltage conditions, therefore, only the PFM loop is used. For high input voltage, the bus voltage feedback loop regulates the bus voltage at the desired value by decreasing the duty cycle. In this case, the converter will enter into the APWM operation mode. In other words, both control loops work simultaneously at high input voltages, keeping the bus voltage constant at the reference value for this condition. Ma et al. (2018a) applied this technique to the conventional PFC boost integrating HB LLC converter (topology illustrated in Figure 2.22a) and a maximum voltage of 500 V under universal input voltage condition was achieved, as can be seen in Figure 2.26. In order to increase the power capacity of the off-line converter, Yi et al. (2021) investigated an integrated off-line LED driver obtained by integrating an interleaved boost PFC and a full-bridge LLC resonant, which operates with an output power of 300 W.

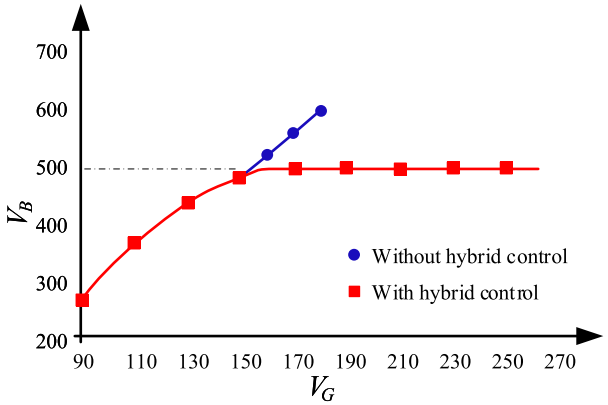


Figure 2.26 – Average bus voltage with and without the hybrid PFM-APWM control (MA et al., 2018a).

Magnetic control has also been applied to the most common topology of LED drivers based on resonant converters (WEI et al., 2020a; WEI et al., 2020), which as already mentioned, is the boost-type PFC integrating LLC resonant. As a PFC stage, a conventional boost was employed in (WEI et al., 2020) while a totem-pole bridgeless topology was used in (WEI et al., 2020a) to increase the overall efficiency of the converter. In both works, the boost inductor is treated as the control variable, which only influences the dc-link voltage and the PFC stage, whereas the operation of the LLC resonant converter remains unchanged. Thus, a constant duty cycle and switching frequency were implemented for the primary switches. The LLC resonant converter was designed to operate at the series resonant frequency in order to achieve a maximum efficiency operation since there is no reverse recovery problem for the secondary rectifier in this condition. However, Wei et al. (2020a) showed that despite the magnetic control, the DCM operating condition does not depend on the boost inductor but on the duty cycle that is kept constant at 0.5. Therefore, magnetically controlled off-line LED drivers with integrated stages have the same drawback of high bus voltage, which makes operation at high input voltages difficult.

Table 2.2 gives a brief characteristics comparison of recently reported off-line topologies based on resonant converters. Low bus voltage was achieved in converters that used the buck-boost type or interleaved topologies as PFC stage, as well as converters with hybrid APWM-PFM control. In addition, the topologies exhibit a wide bus voltage range and the ratio between the maximum and minimum bus voltage may exceed three, resulting in difficulties for designing the resonant converters for the PC stage (YI et al., 2021). In summary, a review of the presented integrated two-stage soft-switched off-line converters shows their common shortcoming: they are difficult to perform well under the universal-input voltage.

2.4 ANALYSIS PROCEDURES FOR THE RESONANT CONVERTER

There are mainly three analysis methodologies for the resonant converters: 1) frequency domain analysis or first harmonic approximation (FHA); 2) frequency domain analysis with time-domain correction ; and 3) time-domain analysis. Figure 2.27 includes a pie chart that shows the distribution of analysis methodologies for the resonant converters among papers evaluated in this thesis.

The majority of the works are based on the first harmonic approximation (FHA), which presents closed-form expressions for the gain and phase relationships, allowing for a quick and straightforward analysis of the converter (MA et al., 2018a; KAZIMIERCZUK; CZARKOWSKI, 2012). There are two considerations that limit the range of application of the FHA. The first one is that the current through the resonant tank is considered purely sinusoidal, even though the resonant tank is excited by a square

Table 2.2 – Integrated Off-line Topologies Based on Resonant Converters

Control scheme	**Topologies**	**Advantagens**	**Drawbacks**
PFM	boost PFC-HB LLC [1]	• high efficiency; • low cost; • low complexity;	• high and wide bus voltage range;
	Totem-pole PFC-HB LLC [2]	• Features of [1]; • bridgeless structure, higher efficiency; • lower cost than [1];	
	dual buck-boost PFC-HB LLC [3]	• high efficiency; • bridgeless structure;	• features of [1] and [2] ; • two inductors of the PFC stage may not equally share the input power;
	dual buck-boost PFC-HB CLCL [4]	• features of [3]; • lower frequency range than [3];	
	buck-boost PFC-HB LLC [5]	• high efficiency; • reduced bus voltage.	• wide bus voltage range; • unbalanced current stress on switches; • two inductors of the PFC stage may not equally share the input power;
	SEPIC PFC - HB LLC [6]		• wide bus voltage range; • high voltage stress of one of the switches;
	SEPIC PFC-class-E [7]		
	interleaved buck-boost PFC - HB LLC [8]	• features of [5] and [6]; • symmetric structure (stress on switches);	• wide bus voltage range; • two inductors of the PFC stage may not equally share the input power;
	interleaved buck-boost PFC - HB CLCL [9];	• features of [8]; • Dimming.	
	interleaved boost PFC - HB LLC [10];	• features of [5] and [6];	• features of [8] and [9]; • two inductors of the PFC stage may not equally share the input power;
	two BCM boost PFC - HB LLC [11]	• features of [5] and [6]; • symmetric structure (stress on switches);	• wide bus voltage range;
APWM	Totem-pole PFC - HB LC [12]	• bridgeless structure; • reduced bus voltage;	• without galvanic isolation; • additional synchronism circuit for PFC;
PFM/ APWM	boost PFC-HB LLC [13]	• reduced bus voltage; • universal-input voltage;	• wide bus voltage range; • wide frequency range (50-216kHz);
	interleaved boost PFC-HB LLC [14];	• features of [13];	
magnetic control	Boost PFC-HB LLC [15]	• low bus voltage range; • constant duty cycle and switching frequency;	• features of [1] and [2];
	Totem-pole PFC-HB LLC [16]		

wave voltage. The second simplification is that the rectifier, the output filter and the load are represented by an equivalent ac-side resistance. Therefore, this technique usu-

ally provides good design results only when the converter is operating at the resonant frequency and/or the load is purely resistive. Moreover, it can lead to significant errors when the circuit operates with a wide input voltage range.

In the analysis methodology based on FHA with time-domain correction, the accuracy is slightly improved when compared with FHA approach. However, assumptions are still made, which will decrease its accuracy when compared with the practical results. For the time-domain analysis, no extra assumptions have been made when analyzing the resonant converter, and therefore, the theoretical analysis is closer to the practical results. The main disadvantage of time-domain analysis is its complexity, which involves sophisticated software to solve nonlinear equations.

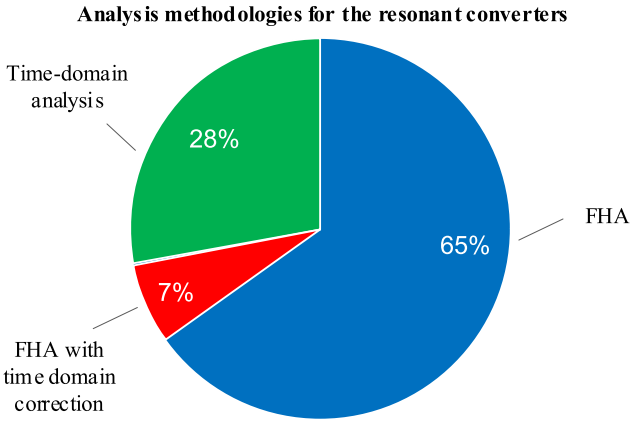


Figure 2.27 – Analysis methodologies of the papers evaluated in this thesis.

2.5 SUMMARY OF THE CHAPTER

This chapter discussed the concepts related to improving LED drivers performance indexes, highlighting their mutual coupling. The improvement alternatives for some performance indexes were evaluated, as well as their negative effects on others, thus forming a necessary basis for proposing high-performance off-line LED drivers.

Main capacitor technologies were investigated, focusing on metallized-film and electrolytic technology. Capacitors are one of the most critical elements in an LED driver and their reliability is affected by voltage, temperature and value of the capacitance, whose reduction greatly improves the lifespan of the driver, as well as power density. In addition, lower capacitance values are commercially available in both technologies and the decision of which technology must be adopted depends on the application. For example, if the designer pursues a longer lifespan, the metallized-film is the best choice, however, if a cheaper and compact LED driver is desired, the electrolytic capacitor technology is more suitable.

Some techniques that allow for the reduction of the filtering capacitances in off-line LED drivers were addressed in this chapter. They are based on alternative topologies, on design procedures or on control techniques. Regarding the alternatives based on control methods, most of them rely on the reduction of the instantaneous power unbalance between the input and the output of the converter, by a large-signal modulation of the duty cycle. Although this technique usually provides good results in terms of capacitance reduction, it implies the increment of the input current distortion.

From the perspective of improving the overall efficiency of the converter, resonant converters are a great alternative for the PC stage of LED drivers since they enable soft-switching. A review of the control schemes and topologies of this converter class has also been performed in this chapter. In an integrated off-line LED driver based on a resonant converter, the combination of topology and control scheme can be chosen according to application requirements, especially the input voltage. However, all of them are difficult to perform well under universal-input voltage mainly for the following reasons: 1) the control schemes used in resonant converters affect the behavior of the PFC stage since both stages share the same switches; 2) a quick and straightforward analysis based on FHA lead to significant errors and the use of an accurate model is required when the circuit operates with a wide input voltage range; 3) resonant converters are nonlinear and the ripple transmission must be accurately evaluated according to the operating point, as will be shown in chapter 3.

3 A NOVEL DESIGN APPROACH FOR LLC RESONANT CONVERTERS IN OFF-LINE LED DRIVING APPLICATIONS

The previous chapter presented a literature review of topologies for off-line LED drivers based on resonant converters as an alternative to achieve high efficiency. Among the resonant converter topologies used as a PC stage, the LLC converter is the most popular, owing to the advantages of high efficiency, high power density, galvanic isolation, wide output ranges, low voltage stress, and high operation frequency. Studies on those topologies are mainly based on the first harmonic approximation (FHA), which presents closed-form expressions for the gain and phase relationships, allowing for a quick and straightforward analysis of the converter. Although this technique has been widely used and usually provides good design results when the converter is operating at the resonant frequency, it can lead to significant errors for LED loads. Moreover, the LF ripple transmission is also calculated inaccurately through the FHA, making it impossible for the proper sizing of the bus capacitance.

In this context, this chapter proposes the design methodology for an LLC resonant converter used as a second stage (*i.e.*, the PC stage) in off-line LED drivers, considering the LF ripple transmission. It is important to highlight that the proposed design methodology allows the proper sizing of the bus capacitance for any design parameters and conditions. Moreover, the converter design can be accomplished accurately with the proposed approach because of the developed mathematical model, which is able to accurately predict the average level and the LF ripple of the output current, even if the converter is designed to operate far from the resonant frequency, a situation that is advantageous in some circumstances. In addition, this chapter shows how the LF ripple is transferred from the bus to the output current and which are converter parameters that have a major influence on this transference. Thus, design guidelines for this topology are proposed considering a trade-off between the LF ripple transmission and the rms current in the resonant tank, which is related to the converter efficiency. This chapter focuses on the LF ripple transmission and for reasons of simplicity, efficiency estimation is not included in this study. However, the efficiency will be calculated in Chapter 6.

The remainder of this chapter is organized as follows. Section 3.1 presents the mathematical description of the LLC resonant converter as a PC stage in off-line LED drivers. Section 3.2 addresses the dc static gain analysis and how the LF ripple is transferred from the bus to the output current. Section 3.3 presents the design methodology based on a numerical analysis focused on the LF ripple transmission of the LLC resonant converter. Section 3.4 addresses design examples based on the proposed numerical analysis. Section 3.5 presents the experimental results obtained from a 46-W laboratory prototype. Finally, the conclusions are detailed in Section 3.6.

3.1 MATHEMATICAL MODEL OF THE LLC CONVERTER

Figure 3.1 shows the LLC resonant converter applied as the second stage in an off-line LED driver. This topology is composed by a half-bridge inverter associated with a resonant LLC filter (L_s, C_s and L_m) and a center tap full-wave rectifier. The converter operates in an open loop with a voltage v_B at its input, which is modeled as a dc power source with a superimposed ac component representing the output voltage of the PFC stage.

The input voltage v_B is described by (3.1), in which V_{B0} is the average bus voltage. The usual LF ripple in off-line LED drivers that comes from the front-end ac-dc conversion stage is represented by a sinusoidal voltage source of amplitude V_{B1} and angular frequency ω_L.

$$v_B(t) = V_{B0} + V_{B1} sin(\omega_L t). \tag{3.1}$$

The input voltage of the resonant tank $v_{HB}(t)$ is generated by the half-bridge inverter, being applied to the LLC resonant tank, which can be written as

$$v_{HB}(t) = \frac{v_B(t)}{2}(\text{sgn}[\sin(\omega_s t)] + 1), \tag{3.2}$$

where $sgn()$ is the sign function, defined as (3.3), and ω_s is the angular switching frequency.

$$\text{sgn}(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ -1, & \text{if } x < 0 \end{cases} \tag{3.3}$$

The output voltage of the converter ($v_o(t)$) can be expressed by the classical piecewise-linear model of the LED string:

$$v_o(t) = r_d i_o(t) + V_t, \tag{3.4}$$

in which V_t and r_d are the threshold voltage and the dynamic resistance of the LED lamp. By analyzing the output node of the converter, the current flowing through the

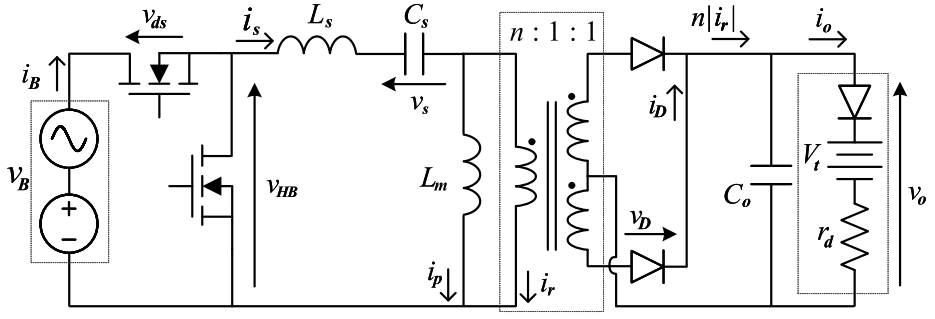


Figure 3.1 – LLC resonant converter as a PC stage of an off-line LED driver.

LED lamp $i_o(t)$ can be written as

$$i_o(t) = n|i_s(t) - i_p(t)| - C_o\frac{\mathrm{d}v_o(t)}{\mathrm{d}t}, \tag{3.5}$$

in which i_s is the current of the inductor L_s, i_p is the magnetizing current and C_o is the output capacitance.

The primary voltage of the transformer ($v_r(t)$) can be written as shown in (3.6).

$$v_r(t) = nv_o(t)\mathrm{sgn}[i_s(t) - i_p(t)], \tag{3.6}$$

in which n is the transformer turns ratio.

As can be seen in Figure 3.1, the LLC resonant converter has four storage elements (L_s, C_s, L_m and C_o) , so that the equation system describing the behavior of the converter is given by the following set of state-space equations:

$$\begin{cases} \dfrac{\mathrm{d}i_s(t)}{\mathrm{d}t} &= \dfrac{1}{L_s}(v_{HB}(t) - v_r(t) - v_s(t)) \\ \dfrac{\mathrm{d}v_s(t)}{\mathrm{d}t} &= \dfrac{1}{C_s}i_s(t) \\ \dfrac{\mathrm{d}i_p(t)}{\mathrm{d}t} &= \dfrac{1}{L_m}v_r(t) \\ \dfrac{\mathrm{d}v_o(t)}{\mathrm{d}t} &= \dfrac{1}{C_o}\left(n|i_s(t) - i_p(t)| - \dfrac{v_o(t) - V_t}{r_d}\right) \end{cases} \tag{3.7}$$

In order to analyze the converter, the mathematical model presented in (3.7) must be solved by employing a numerical integration technique in this non-linear set of differential equations. In this chapter, the behavior of the converter is obtained in a similar way as presented in Ferraz et al. (2018), which uses the composite trapezoidal approximation (LEVY, 2010) together with the *fsolve* function of the MATLAB optimization Toolbox. The detailed procedure for solving the equation (3.7) can also be found in Ferraz (2019). It is important to highlight that in this model, the LED load is not modeled as an equivalent resistive load. This consideration is quite important for the subsequent analyses, mainly those regarding the converter LF ripple transmission, which differs significantly for resistive and LED loads, as will be shown in next sections.

3.2 ANALYSIS OF THE LLC CONVERTER

By using the mathematical model presented in Section 3.1, which will be named as accurate model, an accurate analysis of the LLC converter operating as an LED driver can be developed. First, a dc static gain analysis will be presented in order to compare the accuracy of the FHA and the accurate model in terms of error in the average output current of the converter. Thereafter, the LF gain analysis will show

how the LF ripple is transferred from the bus to the output current and which are converter parameters that have a major influence on this transference. This study will serve as a ground for the choice of the converter parameters.

In order to produce more generalized results, some parameters of the converter were normalized as follows:

- $M = V_o/V_{B0}$ is the dc static gain;
- $Q = \pi^2\sqrt{L_s/C_s}/(8n^2R_o)$ is the normalized ac-side load resistance, in which $R_o = r_d + V_t/I_o$ is the resistance of the LED lamp, at the point of operation;
- $\lambda = L_s/L_m$ is the inductance ratio;
- $\Omega_n = \omega_s\sqrt{L_sC_s}$ is the normalized switching frequency;
- $\omega_{sp} = 1/\sqrt{(L_m + L_s)C_s}$ is the series-parallel resonance frequency;
- $\Gamma = r_d/R_o$ is the normalized dynamic resistance of the LED string. This parameter expresses the ratio between the percentage voltage ripple and the percentage current ripple in the LED luminaire.

The analysis in this chapter is carried out by altering the design parameters and evaluating several converters operating under different operating conditions using the accurate model. The parameter V_{B0} is fixed at 250 V. It is known that experimental results from these different converters are the best parameter for comparison with the accurate model. However, building many prototypes would be necessary to obtain these results. In this work, as a quick and simple alternative, the accurate model was compared with simulation results obtained from the software LTspice, incorporating more realistic models of electronic components. It is important to note that experimental results will be obtained from two laboratory prototypes to validate the accuracy of the model.

3.2.1 **dc Static Gain Analysis**

Figure 3.2a shows the comparison between the dc static gain curve when employing the accurate model and the FHA approach. Furthermore, simulation results obtained from the software LTspice are also presented, employing MOSFET R6020PNJ and diode RFV02V585, which are suitable for the power levels considered in the scope of this work. On the other hand, Figure 3.2b shows the resonant tank current phase angle ϕ for both models.

As can be seen in the figure, for a certain gain M, there is a difference between the accurate model, which is close to simulation results, and FHA approach regarding

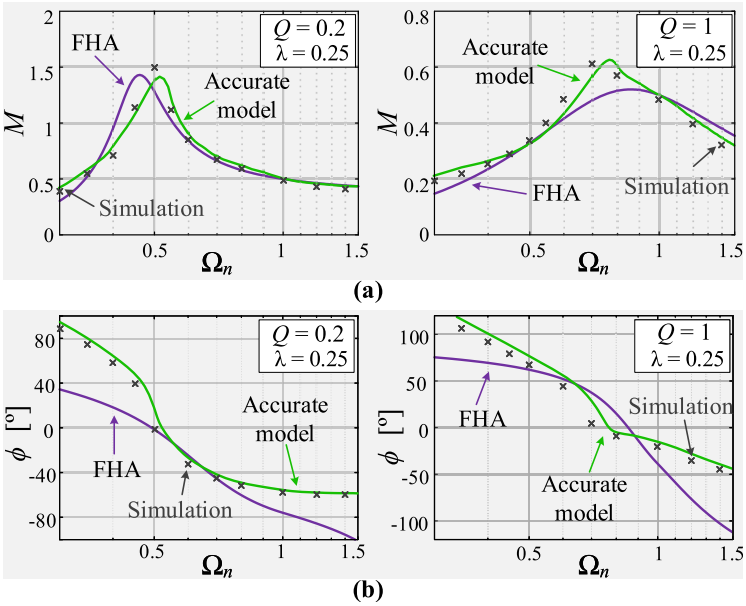


Figure 3.2 – Comparison among FHA, accurate model and simulation results by LTspice. (a) dc static gain curves; (b) phase angle between the current through the resonant tank and the input voltage.

the normalized frequency. This difference occurs owing to the simplifications employed in the FHA model, which lead to an error in the output voltage, and consequently, an error in the average output current. Furthermore, the error regarding the resonant tank current phase indicates that the FHA model can incorrectly predict the zero voltage switching region (ZVS). In order to quantify the dc static gain error related to the FHA approach, a case with $r_d = 8.128\ \Omega$, $V_t = 86.4$ V, $n = 1$ and $\lambda = 0.25$ was investigated considering $Q = 0.2$ and $Q = 1$. This analysis is presented in Figure 3.3a (output voltage error) and 3.3b (LED current error). The voltage and current errors are calculated according to (3.8).

$$\begin{cases} e_{V_o} = \dfrac{|V_o - V_{o,des}|}{V_{o,des}} \\ e_{I_o} = \dfrac{|I_o - I_{o,des}|}{I_{o,des}} \end{cases} \tag{3.8}$$

in which $V_{o,des}$ is the desired average output voltage and $I_{o,des}$ is the desired average output current.

By analyzing the errors of the FHA approach, it can be observed that the voltage error is acceptable. For a purely resistive load, the current error would be the same as the voltage error and, therefore, the first harmonic approximation can be used without major consequences. However, for an LED ($\Gamma < 1$) the current error can achieve very high values depending on the chosen normalized frequency and quality factor. Some works have used the FHA for designing LED drivers. However, in the

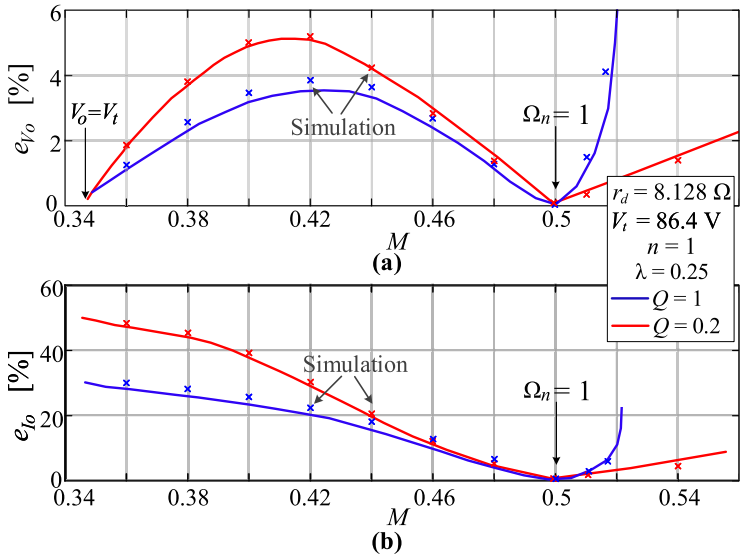


Figure 3.3 – Errors presented by the LLC simulation designed by FHA. (a) average output voltage error; and (b) average output current error in LED lamp.

majority of them, the quality factor was high and/or the normalized frequency was unitary, neglecting the aforementioned errors. Therefore, the dc static analysis shows that the FHA alone is suitable for designing resonant converters only for the cases in which the chosen normalized frequency is nearly unity or the quality factor Q is high. On the other hand, the mathematical model presented in this work can be used for designing such converters regardless of the values of those parameters, ensuring a good design accuracy.

3.2.2 **Low-frequency Gain Analysis**

This section presents the analysis of the main factors that have influence on the LF current ripple transmission of the LLC resonant converter operating in the ZVS region. The parameter V_{B1} is fixed at 10 V. In other words, the bus voltage ripple is 20 V ($\Delta V_B = 2V_{B1}$).

Figure 3.4a presents the behavior of the converter LF ripple gain $\Delta I_o/\Delta V_B$ according to variations in the normalized dynamic resistance of the LED lamp for a constant output power P_o = 45.2 W and several values of Ω_n. The results show that the LF gain of the converter decreases as the normalized dynamic resistance grows. The curves of Figure 3.4a show that as the load tends to a pure resistor (*i.e.*, $\Gamma \approx 1$), the impact of the normalized frequency becomes negligible. However, for small values of Γ, *i.e.* for LED lamps with low dynamic resistance, the LF ripple transmission has a strong dependence on the value of Ω_n.

Figure 3.4b shows the LF ripple transmission for different inductance ratios of the converter supplying an LED lamp with r_d = 8.13 Ω and V_t = 86.4 V (Γ = 0.045).

The figure shows that the LF current ripple transmission does not depend significantly on the inductance ratio (λ).

The LF LED current ripple attenuation and the rms current in the resonant tank according to variations in the normalized switching frequency are presented in Figure 3.5. In this case, the turns ratio of the ideal transformer was adjusted to have the same dc static gain in all operating points, so that the load is at nominal power at every operating point. The results show that the maximum LF current ripple transmission occurs when $\Omega_n = 1$. Thus, the LF gain of the converter decreases as the normalized switching frequency distances from unity. On the other hand, the rms value of the filter current increases as the normalized switching frequency grows. In other words, the converter manages more reactive power the farther it operates from the series-parallel resonance frequency, ω_{sp} (see Figure 3.5), which will produce an efficiency and power quality decrease. Therefore, there is a trade-off between ripple transmission attenuation and efficiency decrease in the design process. This conclusion is an important contribution of this work for LED loads, since it helps designers to choose the right design directives for its application considering the trade-off between conduction losses, which are related to the rms current of the resonant tank, and the LF ripple transmission, which defines the bulk capacitance in off-line LED drivers.

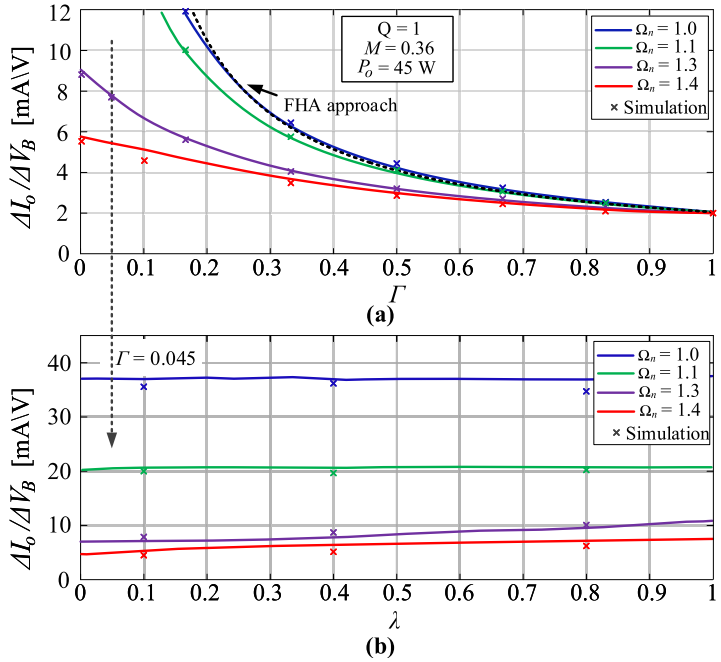


Figure 3.4 – LF gain of the LLC LED driver. (a) converter supplying different LED lamp at 45.2 W; (b) LF gain for different inductance ratio λ supplying LED example with $\Gamma = 0.045$.

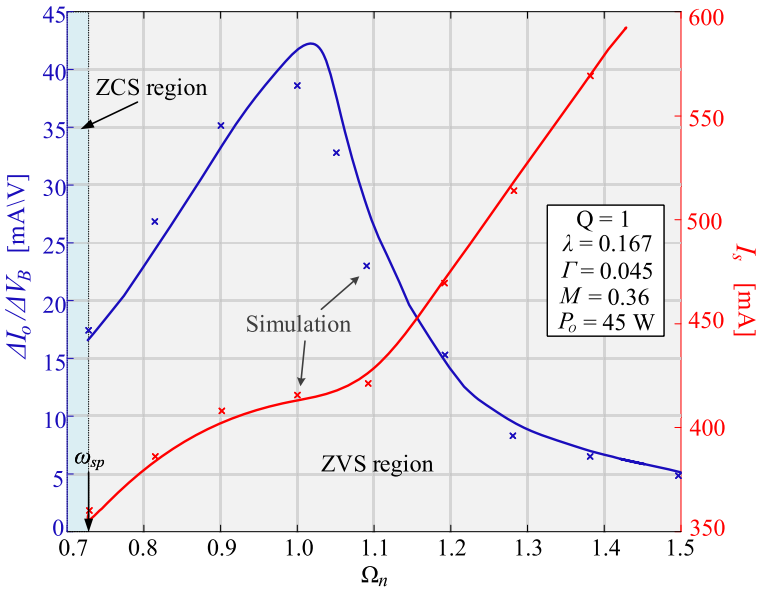


Figure 3.5 – LF gain of the LLC LED driver and the rms current in the resonant tank for different normalized switching frequency

3.3 DESIGN METHODOLOGY

This section presents a design methodology for LLC resonant converters employed as a PC stage in an off-line LED driver. The proposal is based on the analysis presented in Section 3.2 and, therefore, takes into account the trade-off between ripple transmission and resonant tank rms current. The design procedure derived from this work was devised so that the advantages of both FHA approach and accurate model can be used together. Therefore, the methodology consists in calculating the LLC converter elements through the FHA approach by supposing an approximated value of the switching frequency and then, by using the accurate model, the correct value for f_s is calculated, *i.e.*, the one which ensures that the LLC converter will operate with the desired dc gain. In addition, the maximum value of the bus voltage ripple that provides the LF ripple criterion in the LED current is properly predicted, thus allowing the sizing of the bus capacitance in off-line LED drivers.

The step-by-step procedure for designing the converter is presented in the flowchart of Figure 3.6. As can be seen, the procedure is described as an iterative process composed of seven steps, which are explained in the following.

Step 1: The appropriate choices of the converter parameters aiming at higher LF current ripple attenuation or higher efficiency must be done in this step. Here the designer must take into account the trade-off discussed in Section 3.2. If a low LF gain and ZVS operation is desired, the normalized frequency must be larger than one, as shown in Figure 3.5. On the other hand, if a higher efficiency is pursued, the

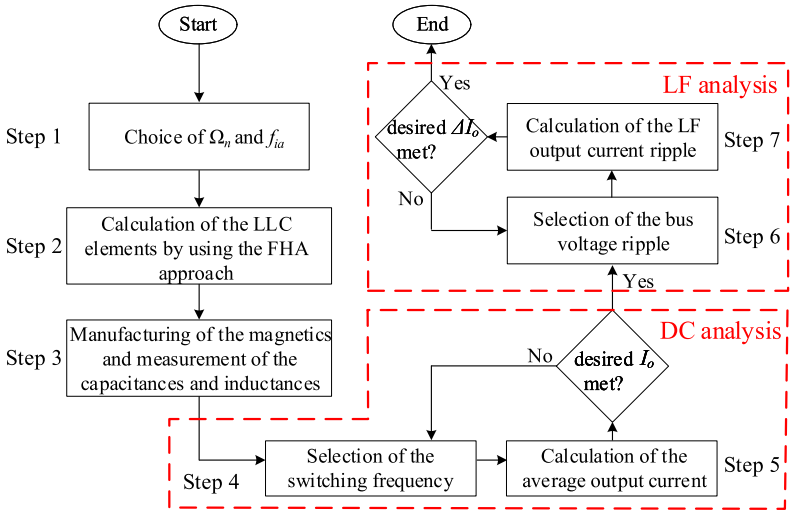


Figure 3.6 – Design steps flowchart of the LLC LED driver

normalized frequency must be chosen close to one, as shown in Figure 3.5. The load characteristics must also be defined in this step. Regarding the switching frequency, the designer must select an initial approximation for this parameter f_{ia}, which will be corrected in Step 4 by using the accurate model.

Step 2: Calculation of the L_s, C_s, L_p, n and C_o by using the FHA and considering an approximated value of the correct switching frequency, as explained earlier.

Step 3: The prototype components are built and their real values are employed for calculating the correct switching frequency by means of the accurate model.

Step 4: Calculation of the correct switching frequency by using the accurate model and a search method based on a linear approximation, as given by (3.9).

$$r_k = r_{k-1} + e_{k-1}\left|\frac{r_{k-1} - r_{k-2}}{f(r_{k-1}) - f(r_{k-2})}\right|, \tag{3.9}$$

in which r is the switching frequency, $f(r)$ is the average output current, k is the index of the k^{th} sample of the search method and e is the error between current and desired value.

Step 5: Calculation of the average output current using the accurate model.

Step 6: Calculation of the correct bus voltage ripple by using the accurate model and the search method explained in (3.9). In this case, r is the bus voltage ripple and $f(r)$ is the LF output current ripple.

Step 7: Evaluation of the LF output current ripple in order to be compared with the desired value. This evaluation was obtained from the accurate model, according to Melo et al. (2015a), as presented in the following

$$\Delta I_o = I_{o,max} - I_{o,min}, \tag{3.10}$$

in which $I_{o,max}$ is the LEDs average current at the higher input voltage ($V_{B0} + V_{B1}$) and $I_{o,min}$ is the average output current at the lower input voltage ($V_{B0} - V_{B1}$).

3.4 DESIGN EXAMPLE

By using the approach to design LLC converter shown in previous section, design examples for off-line LED driving applications considering different design directives can be carried out. First, an evaluation of the LLC converter will be presented in order to validate the proposed design methodology. Thereafter, a case study of an off-line LED driver will show how the bus capacitance can be reduced when the LLC converter operates far from the resonant frequency.

3.4.1 **Evaluation of the LLC Converter**

In order to validate the proposed methodology, this section presents two design examples of LLC resonant converters applied to LED driving considering different design directives. Aiming at a fair comparison, both designs have the same LED operating point and were designed to operate under ZVS conditions (inductive tank characteristic). The first one, which will be named DE1, operates above the series resonant frequency ($\Omega_n = 1.65$), thus presenting a higher LF LEDs current ripple attenuation and lower parametric sensitivity. However, the efficiency is expected to be lower in this design, since the resonant tank current will have a higher rms value. On the other hand, the second design example, which will be named DE2, operates at the series resonant frequency ($\Omega_n = 1$), thus obtaining greater efficiency and better power quality. The disadvantage of this second design is that it has a lower LF current ripple attenuation and higher parametric sensitivity. Table 3.1 shows the design parameters of the converters, which are used in Step 1 of the proposed methodology.

The load is composed by 32 Luxeon Rebel LEDs connected in series and is described in terms of V_t and r_d, which are also shown in Table 3.1. The criterion for choosing the output current ripple was based on IEEE (2015), which showed that an output current ripple of 19% has a low risk to cause human biological effects at 120 Hz, which is the case of off-line LED drivers supplied by a 60-Hz mains voltage.

Since the input data is completely defined, the design of the converter's elements is done by FHA approach, by following the procedure outlined in Simone et al. (2006) and considering a design switching frequency. Firstly the turns ratio n is calculated to have the desired dc static gain. Thereafter, the series inductor, the series capacitor and the parallel inductor are calculated, according to Ma et al. (2018a).

The output capacitor can be obtained by evaluating the current through the output node of the converter (3.11). Thus, by solving (3.11) for C_o, the output capacitor

Table 3.1 – Design Parameters.

Symbol	Description	Value
V_{B0}	Half-bridge input average voltage	250 V
ω_L	Angular frequency of the v_B	2π120 rad/s
Q	Quality factor of the resonant tank	0.8
λ	Inductance ratio	0.167
V_t	Nominal threshold voltage of the LEDs	86.4 V
r_d	Dynamic resistance of the LED lamp	8.128 Ω
I_o	Average output current	500 mA
V_o	Average output voltage	90.464 V
P_o	Output power	45.232 W
ΔI_o	Maximum LF LEDs current ripple	95 mA
ΔI_{oHF}	High frequency LEDs current ripple	20 mA

can be calculated by means of (3.12).

$$\Delta I_{oHF} = \frac{4I_o}{3}\left|\frac{1}{1+\mathrm{j}2\omega_s C_o r_d}\right|, \tag{3.11}$$

$$C_o = \frac{1}{2\omega_s r_d}\sqrt{\left(\frac{4I_o}{3\Delta I_{oHF}}\right)^2 - 1}. \tag{3.12}$$

Based on the procedure outlined in Step 2 of the proposed methodology, the design results shown in Table 3.2 were obtained. As can be noted the initial approximation for the switching frequency f_{ia} for the DE1 is higher than the one selected for the DE2. This choice was done for the sake of a fair comparison, because the switching frequency adjustment of DE1 performed in Step 4 will be higher, thus making this parameter similar for both design examples. It is worth mentioning that the adjustment performed in Step 4 for DE2 is small, since the converter is devised to operate near resonance. Higher switching frequencies approximately 100 kHz will be explored in Chapter 6, as they are more compatible with the LLC resonant converter.

The next step of the proposed design methodology is the manufacturing of the prototype components, whose values are given in Table 3.3 for both design examples.

Table 3.2 – FHA Design Results.

Symbol	Design example 1 (DE1)	Design example 2 (DE2)
	Input parameters	
Ω_n	1.65	1
f_{ia}	85 kHz	78.6 kHz
	Elements calculated by FHA	
L_s	361.4 μH	354.2 μH
C_s	30.17 nF	9.05 nF
L_m	1.89 mH	2.72 mH
n	0.93	1.38
C_o	3.84 μF	4.16 μF

Table 3.3 – Main Parameters of Design Example Prototypes

Item	Value
	Semiconductor elements
Half-bridge switches	SPP08N80C3 (800V / 0.65Ω)
Output rectifier diodes	MUR460
	Design Example 1 (DE1 - $\Omega_n = 1.65$)
Resonant inductor L_r	312.6 μH / NEE 30-15-7 / 38 turns gap = 0.16 mm / 2x26 AWG
Resonant capacitor C_s	35 nF polypropylene capacitor (2x15 nF B32693/UD)
Output capacitor C_o	3.3 μF/ 250 V polypropylene capacitor (335K250U)
Conduction losses R_s	2.75 Ω
LLC Transformer	NEE 42-21-15 / 85:91:91 turns gap = 0.32 mm / 2x26 AWG
Turns ratio n	0.93
Self-inductance L_p	2.35 mH
Leakage inductance L_d	2.4 μH
	Design Example 2 (DE2 - $\Omega_n = 1$)
Resonant inductor L_r	440 μH / NEE 30-15-7 / 45 turns gap = 0.16 mm / 2x26 AWG
Resonant capacitor C_s	9.3 nF polyester capacitor (2x4.7 nF P692XN21)
Output capacitor C_o	3.3 μF/ 250 V polypropylene capacitor (335K250U)
Conduction losses R_s	3.74 Ω
LLC Transformer	NEE 42-21-15 / 64:46:46 turns gap = 0.16 mm / 2x26 AWG
Turns ratio n	1.39
Self-inductance L_p	2.76 mH
Leakage inductance L_d	3.1 μH

From this table it is possible to see that the same semiconductor elements were used for both prototypes.

It is important to highlight that the series inductance L_s can be calculated as the sum of the leakage inductance of the LLC transformer L_d and the inductance of the resonant inductor L_r, as shown in (3.13). On the other hand, the magnetizing inductance L_m can be calculated by subtracting the leakage inductance L_d from the self-inductance L_p, as described by (3.14).

$$L_s = L_d + L_r. \tag{3.13}$$

$$L_m = L_p - L_d. \tag{3.14}$$

By considering the values of the converter elements and following the procedure outlined in steps 4 and 5 (see Figure 3.6), the switching frequency can be calculated. Similarly, by using the procedures described in steps 6 and 7, the maximum value of the bus ripple that ensures the low-frequency ripple criterion can be determined. The results of these parameters for both design examples are shown in Table 3.4.

Table 3.4 – Results of the proposed designed methodology

Description	DE1 (Ω_n=1.65)	DE2 (Ω_n=1)
Switching frequency f_s	78.6 kHz	76 kHz
Maximum bus ripple ΔV_B	17.94 V	2.8 V

3.4.2 **Case Study: An off-line LED driver based on the LLC Converter**

This section presents a case study of a two-stage off-line LED driver with independent stages in order to show how the bus capacitance is affected by the design directive of the LLC resonant converter. In this example, the PFC stage is composed of a boost converter operating in DCM mode, which is a common choice for this role (MA et al., 2018a). The topology of this two-stage Boost-LLC converter can be seen in Kim et al. (2013).

The design of the PFC stage can be carried out as presented in Almeida et al. (2015b). According to this work, the bus capacitance can be written as shown in (3.15).

$$C_B = \frac{\Delta Q_{CB}}{\Delta V_B}, \tag{3.15}$$

where ΔQ_{CB} is the amount of charge injected in (or extracted from) the bus capacitance during each quarter of line cycle.

Considering that the input is a 127-V/60-Hz mains and using the design parameters of the LLC converter listed in Table 5.1 and 3.4, the bus capacitance can be calculated as 49.2 μF for DE1 and 351.7 μF for DE2. It is important to highlight that, the normalized switching frequency has a great influence on the LF ripple transmission and, consequently, on the value of the bus capacitance. In this case, when the LLC converter operates far from the resonant frequency (DE1 - Ω_n=1.65), a reduction of 86% in the required filtering capacitance was allowed when compared with the conventional DE2 approach (Ω_n=1).

3.5 EXPERIMENTAL RESULTS

This section presents the experimental results for the designs examples of LLC resonant converter applied to LED driving and for a case study of the two-stage off-line LED driver discussed in Section 3.4.2.

3.5.1 **LLC resonant converter applied to LED driving**

In order to validate the proposed design methodology, the prototypes of the design examples 1 and 2 were built, whose boards are shown in Figure 3.7.

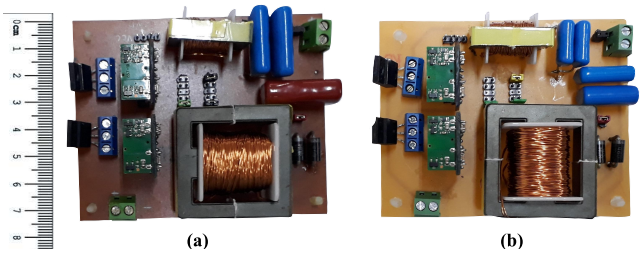


Figure 3.7 – Photographs of prototypes. (a) design with $\Omega_n = 1.65$ (DE1); and (b) design with $\Omega_n = 1$ (DE2).

Figure 3.8 presents experimental waveforms of the semiconductor elements and resonant tank for $\Omega_n = 1.65$ (a) and $\Omega_n = 1$ (b). As can be seen in Figure 3.8a, the converter of DE1 operates above series resonant frequency and under ZVS.

Figure 3.9a presents experimental waveforms obtained for the design with $\Omega_n = 1.65$ operating with a bus voltage ripple $\Delta V_B = 18.1$ V. The LF output current ripple obtained from this experiments was 93.5 mA, which is close to the 95 mA predicted by the algorithm. Meanwhile, Figure 3.9b presents experimental waveforms obtained for the design with $\Omega_n = 1$. In this case, the LF output current ripple obtained was very similar, 100.2 mA, but with a much lower bus voltage ripple, $\Delta V_B = 2.8$ V, which requires a much higher bulk capacitance at the output of the PFC stage. The designed capacitance values and the measured efficiency for each case are emphasized in the

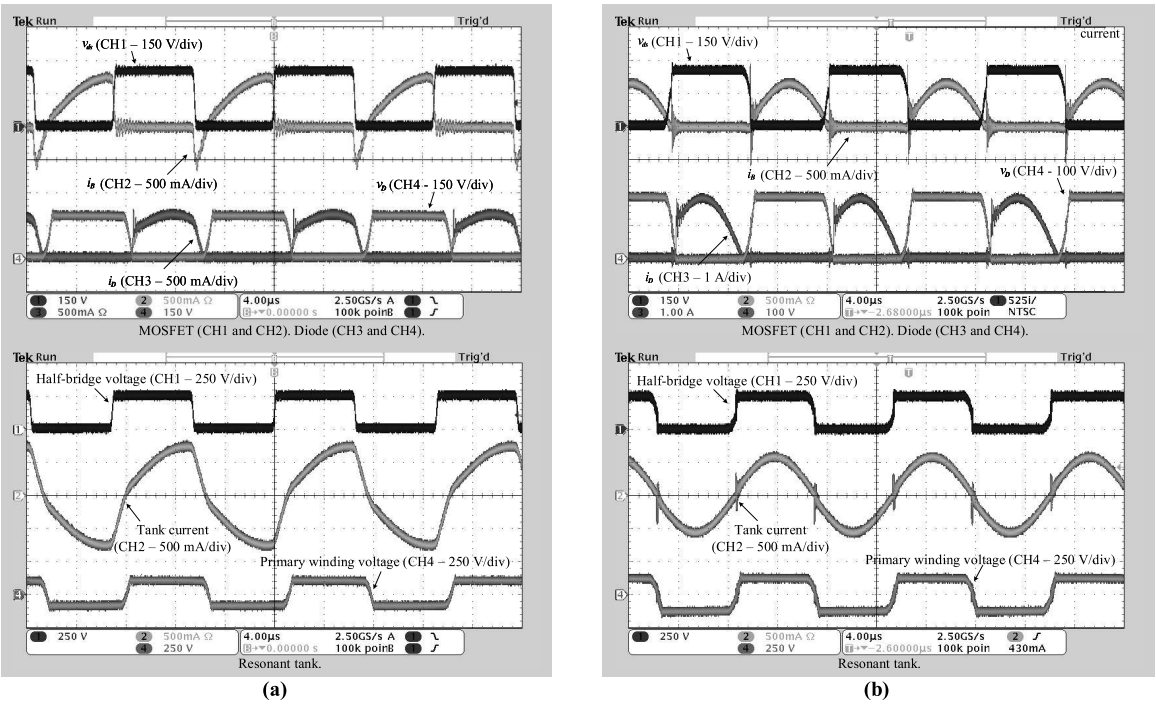


Figure 3.8 – Experimental waveforms in the semiconductor elements and resonant tank. Horiz. scale: 4 μs/div. (a) Design with $\Omega_n = 1.65$ (DE1); and (b) Design with $\Omega_n = 1$ (DE2).

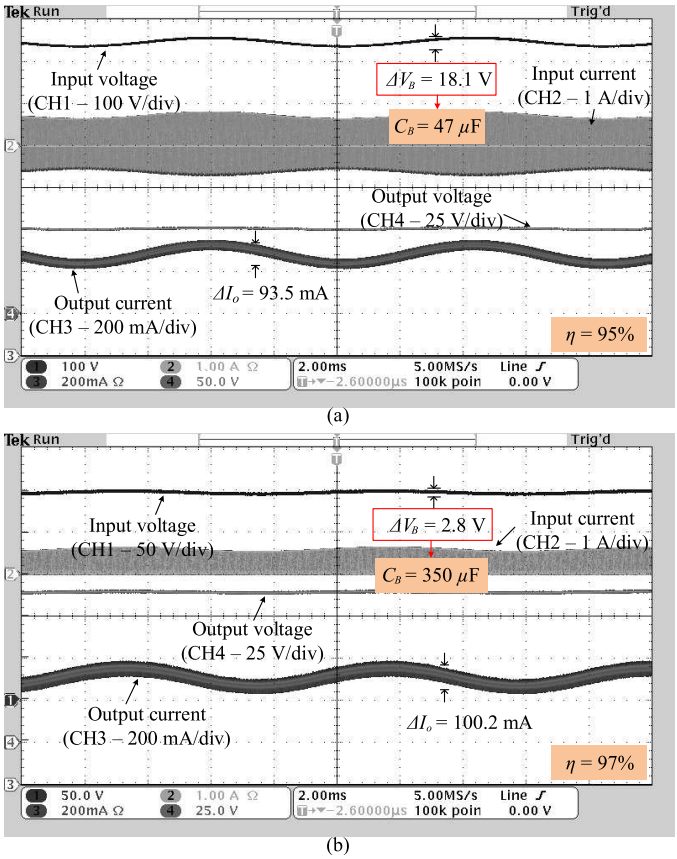


Figure 3.9 – Experimental waveforms obtained for the LLC LED driver. Horiz. scale: 2 ms/div. (a) Design with $\Omega_n = 1.65$ (DE1); and (b) Design with $\Omega_n = 1$ (DE2).

figures.

In order to show that the difference in LF ripple gain between the design examples arises because of the LED load, Figure 3.10 presents the experimental results for a resistive load whose power is the same of the analyzed LED load. As can be seen, the LF ripple is the same for both design examples, *i.e.*, it does not depend on Ω_n, as stated in Section 3.2 (see Figure 3.5). This result attests the importance of this study, since this difference in the LF ripple transmission between LED and resistive loads was not reported elsewhere. Furthermore, it can be noted that the LF gain and the dc gain are nearly the same for the resistive load, which does not occur when the converters feed an LED load, as shown in Figure 3.9.

By using a Yokogawa WT230 digital power meter, the losses distribution for both prototypes were measured. The results, presented in Table 3.5, show that the losses are concentrated in the series resonant tank and are greater in the design example 1 ($\Omega_n = 1.65$). This result can be explained by the rms value of the current through the resonant tank, which was 549 mA for the design with $\Omega_n = 1.65$ and 403 mA for design with $\Omega_n = 1$. The measured efficiency was 95.2% for DE1. On the other hand, the measured efficiency of DE2, which operates very close to the series resonant frequency,

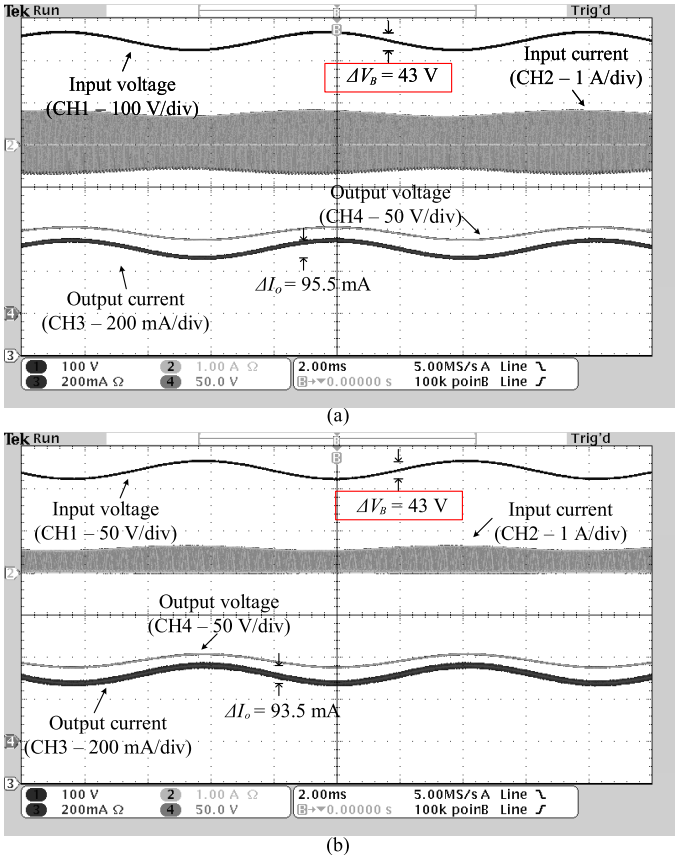


Figure 3.10 – Experimental waveforms obtained for the LLC supplying a 181 Ω resistive load. Horiz. scale: 2 ms/div. (a) Design with $\Omega_n = 1.65$ (DE1); and (b) Design with $\Omega_n = 1$ (DE2).

was 97.2%.

Figure 3.11 presents the behavior of the efficiency of both prototypes as a function of the switching frequency (Figure 3.11a) and the bus voltage (Figure 3.11b). The results show that the efficiency of the circuit in DE1 is lower than DE2 even for different values of switching frequency and bus voltage. As can be noted in Figure 3.11a, the efficiency reduces with increasing switching frequency, as expected since the converter manages more reactive power the farther it operates from the series-parallel resonance frequency (see Figure 3.5). On the other hand, Figure 3.11b shows that the efficiency

Table 3.5 – Loss Breakdown

Component	Ω_n=1.65 (DE1)	Ω_n=1 (DE2)
Half-bridge switches	0.2 W	0.1 W
Resonant inductor	0.9 W	0.4 W
Resonant capacitor	0.5 W	0.3 W
LLC transformer	0.1 W	0.1 W
Output rectifier diodes	0.4 W	0.3 W
Output Capacitor	0.1 W	0.1 W
Total	2.2 W	1.3 W

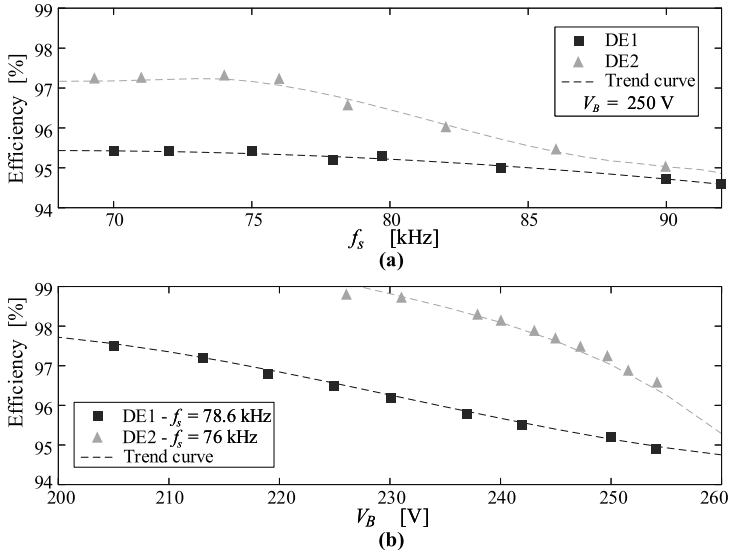


Figure 3.11 – Behavior of the efficiency of both prototypes as a function of the (a) switching frequency and (b) the bus voltage.

increases as the bus voltage decreases. In addition, it is important to highlight that the DE1 converter efficiency is less sensitive to voltage and frequency variations when compared with the conventional DE2 approach (Ω_n=1).

Table 3.6 highlights the trade-off between a LF gain and the efficiency in the design process. As supposed in the theoretical analysis, the design with $\Omega_n = 1.65$ presents a lower LF gain, thus allowing the use of lower capacitances in the PFC pre-regulator. On the other hand, the circuit with $\Omega_n = 1$ is more efficient and has a better power quality.

Table 3.6 – Comparative Experimental Results of the LLC converters.

Description	Ω_n=1.65 (DE1)	Ω_n=1 (DE2)
Switching frequency f_s	78.6 kHz	76 kHz
dc gain I_o/V_B	1.96 mA/V	2.04 mA/V
LF gain $\Delta I_o/\Delta V_B$	5.17 mA/V	35.79 mA/V
Resonant tank rms current	549 mA	403 mA
Efficiency	95.2%	97.2%

3.5.2 **Two-stage off-line LED driver based on the LLC Converter**

In order to validate the influence of the design directive on the bus capacitance value, the prototype of the two-stages boost-LLC converter addressed in section 3.4.2. The boost PFC, shown in Figure 3.13, operates in DCM mode to ensure low THD and a high PF. Table 3.7 shows the value of the prototype components of PFC stage. DE1 and DE2 were used as the PC stage of this converter.

In this case study, the measured efficiency of the PFC stage was 96.2%. The-

Table 3.7 – Main Parameters of the PFC boost prototype

Item	Value
EMI filter	DM: L_{DM} = 1,19 mH and C_f =330 nF
Diode Bridge	GBU4J (600V/ 4A)
Boost inductor	470,97 μH / NEE 30-15-7 / 66 turns gap = 0,32 mm / 24 AWG
MOSFET	SPP08N80C3 (800 V/ 0,65 Ω)
Diode	MUR460 (600 V/ 4 A)
Bus capacitor C_B	47 μF/ 450 V electrolytic capacitor (450PX47MEFC)

refore, the overall efficiency of the two-stage off-line LED driver with $\Omega_n = 1.65$ and $\Omega_n = 1$ were 91.5% and 93.5% respectively. Regarding power quality, the measured total harmonic distortion (THD) of the input current was 23% for DE1 and 23.1% for DE2. Furthermore, the harmonic content of the input current complies with the IEC-61000-3-2:2018 standard in both cases, as shown in the Figure 3.12.

Figure 3.14a presents experimental waveforms obtained for the two-stage off-line LED driver based on the LLC converter with $\Omega_n = 1.65$ (DE1) compared with the PC stage with $\Omega_n = 1$ (Figure 3.14b), and also with the conventional approach (DE2) with a bus capacitance of 350 μF (Figure 3.14c). The bus voltage low-frequency ripple obtained in DE1 experiment was 13.1 V, slightly below the one foreseen in the theoretical analysis. The LF output current ripple was 80 mA, which produces a flicker level that has a low risk to human health (IEEE, 2015). In addition, Figure 3.14b depics a larger ripple when the LLC converter operates at the series resonant frequency with the same bus capacitance of 47 μF, being necessary an additional value of 303 μF (Figure 3.14c) to decrease the output current ripple to a similar level of the one obtained when the DE1 is chosen.

From these experimental results, both two-stage off-line prototypes were investigated by the performance analysis tool, as shown in Figure 3.15. Since the same circuit is used as the PFC stage, both converters exhibit similar ac input power quality. However, DE1 performs far better in terms of reliability and power density because it uses a lower bus capacitance value than DE2. On the other hand, the circuit of DE2 is more efficient because the LLC converter operates under resonance frequency.

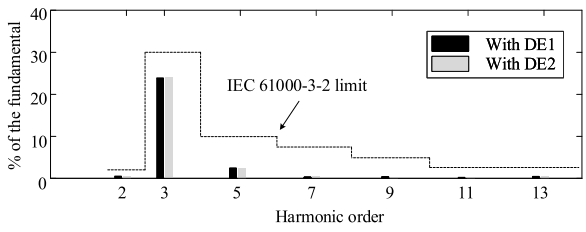


Figure 3.12 – Harmonic content of the input current of the prototypes compared with IEC limits.

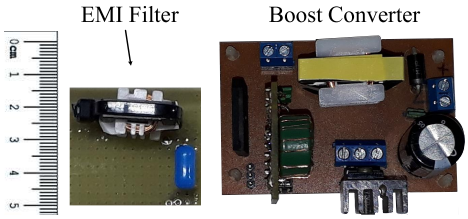
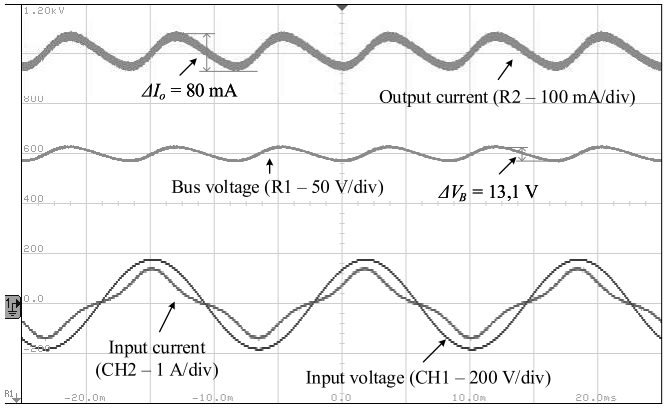
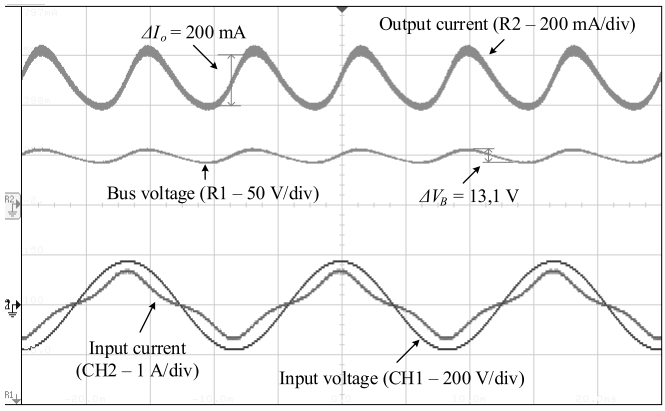


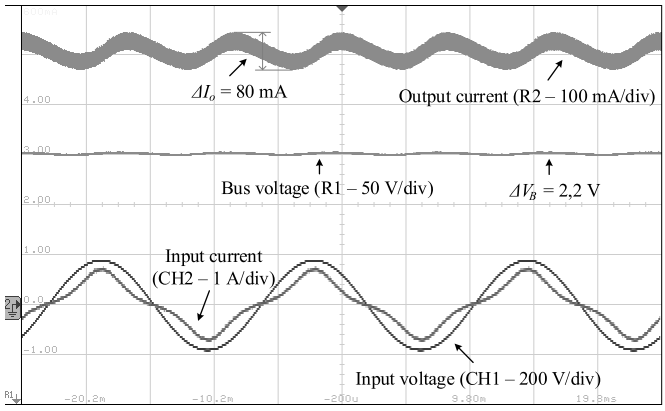
Figure 3.13 – Photograph of EMI filter and PFC boost prototype



(a) C_B = 47 µF with DE1



(b) C_B = 47 µF with DE2



(c) C_B = 350 µF with DE2

Figure 3.14 – Experimental waveforms obtained for the two-stage off-line LED driver based on the LLC converter. **(a)** $C_B = 47\ \mu$F with $\Omega_n = 1.65$; **(b)** $C_B = 47\ \mu$F with $\Omega_n = 1$; **(c)** $C_B = 350\ \mu$F with $\Omega_n = 1$; Horiz. scale: 5 ms/div.

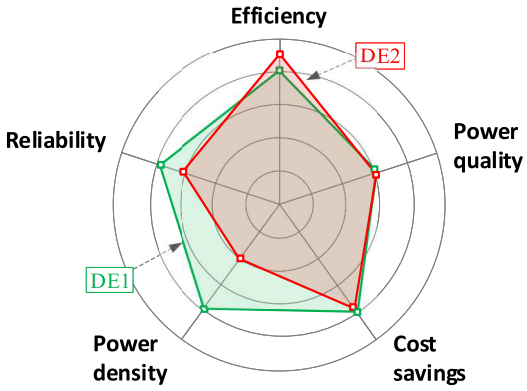


Figure 3.15 – Performance analysis of two-stage LED drivers based on DE1 and DE2.

3.6 SUMMARY OF THE CHAPTER

This chapter presented an accurate model for analyzing resonant converters operating in ZVS region applied to LED driving, considering the low-frequency current ripple transmission. The accurate model was used for devising a design methodology that was able to ensure the desired average output current and also to predict the low-frequency current ripple transmission with very small errors. Therefore, the maximum value of the bus ripple that ensures the low-frequency ripple criterion was determined, thus allowing the proper sizing of the bus capacitance for any design parameters and conditions. The analyses showed that the normalized switching frequency (Ω_n) has a great impact on the LF current ripple transmission and must be properly chosen in order to mitigate the low-frequency current ripple in the LED lamp.

Furthermore, two application examples were also detailed, highlighting the trade-off between the LF gain and efficiency. In addition, a two-stage off-line LED driver was discussed, emphasizing the impact of LF gain in designing the bus capacitance. The experiment showed that the bus capacitance reduction of 86% can be achieved by choosing $\Omega_n = 1.65$. Moreover, this choice implies an efficiency reduction of 2% in relation to the design with $\Omega_n = 1$. Therefore, the selection of Ω_n (lower LF LEDs current ripple or higher efficiency) must be a designer criterion for LLC resonant converters applied to off-line LED drivers.

This chapter has generated insights and mathematical tools capable of evaluating and designing resonant converters with a wide variation of design parameters. Although there is a trade-off between the LF gain (capacitance) and efficiency, both high efficiency and low capacitance are desirable features in high-performance LED drivers. Thus, this work will conceive a LED driver with a resonant stage to achieve high efficiency and employs a control technique (proposed in the next chapter) for capacitance reduction.

4 FREQUENCY-BASED ARC TECHNIQUE TO REDUCE BULK CAPACITANCE IN INTEGRATED OFF-LINE LED DRIVERS

The previous chapter addressed the design methodology for an LLC resonant converter, focusing on the LF ripple transmission and allowing the proper sizing of the bus capacitance for any design parameters and conditions. The converter design can be accomplished accurately because of the developed mathematical model, which allows for the converter operation with a wide variation of switching frequency, input voltage, and output power.

In order to increase the power density and the lifespan of LED drivers, several studies have proposed Active Ripple Compensation (ARC) techniques for minimizing the converter bulk capacitance. However, a common side-effect of the ARC method is the increase in the Total Harmonic Distortion (THD) of the converter input current, as shown in Figure 4.15. In this context, this work proposes an alternative that allows for output ripple compensation with a lesser negative impact on THD: the switching frequency modulation, which can be applied to resonant power control stages, thus improving the overall LED driver efficiency by employing soft-switching. Furthermore, this paper presents a more complete and generalized analysis of the active ripple compensation technique based on this large-signal modulation of the control variable in integrated off-line converters. In this way, as will be shown, the strategy of the switching frequency modulation has several advantages and can be used to design LED drivers with high efficiency and very low capacitance.

4.1 ACTIVE RIPPLE COMPENSATION TECHNIQUES

This section presents the study of the ARC technique based on the large-signal modulation of the control variable in integrated off-line LED drivers, comparing duty-cycle versus switching frequency modulation, as illustrated in Figure 4.1. The analysis carried out in this chapter considers that the driver is based on integrated topologies whose first stage (PFC) operates in discontinuous conduction mode (DCM), since it allows the converter to achieve a high power factor without using a loop for controlling the input current. As mentioned in section 2.2.2, the capacitance reduction is achieved when the bus voltage ripple is higher. This increase in low frequency ripple does not impact the LED current because the ripple compensation technique reduces the ripple transmission. Figure 4.1 shows that the modulation of the control variable can generate distortions in the input current since integrated off-line LED drivers use only one control signal to drive two stages.

The effectiveness of the ARC technique when applied to integrated converters is related with the frequency response characteristic of such converters. As shown in

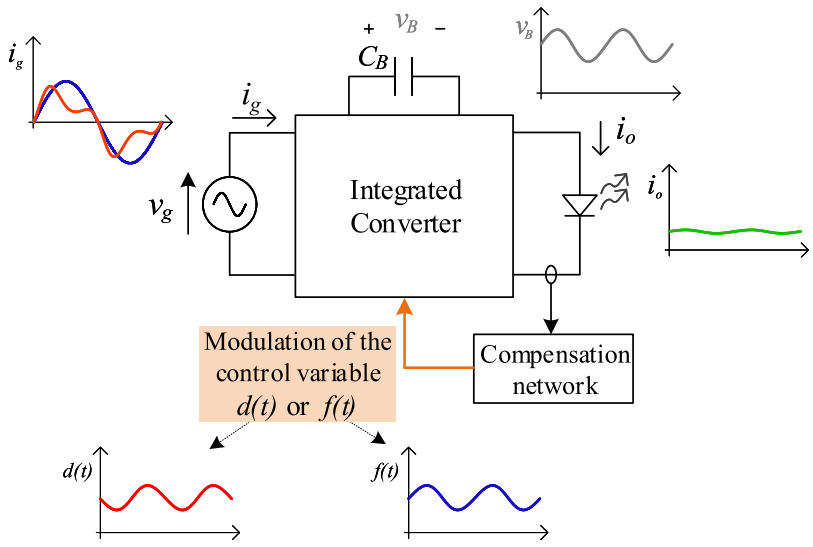


Figure 4.1 – Simplified diagram of an integrated off-line LED driver with a low-frequency large-signal modulation of the duty cycle or switching frequency.

Wu e Chen (1999), the output-to-control transfer function of an integrated converter depends only on the output stage. In addition, the operating principles of each stage are preserved although they share switches. Therefore, both stages can be discussed separately in order to simplify the analysis. First, the PFC stage with duty cycle or frequency modulation will be considered to calculate the THD. Thereafter, the values of the ARC parameters required to reduce the LF ripple in the LED current will be evaluated in the PC stage.

The line voltage can be defined by its RMS value V_G and angular frequency ω_L, as described by (4.1). In off-line converters, it is well-known that the main variables (*e.g.*, the output current) oscillate at twice the line frequency. Similarly to what was presented in Soares, Alonso e Braga (2018), an extra control parcel at twice the line frequency has been added, thus allowing it to influence the large-signal behavior of the converter. In this way, the duty cycle and the switching frequency functions used in the analysis of this section may well be represented by (4.2) and (4.3) respectively.

$$v_g(t) = \sqrt{2}V_G \sin(\omega_L t). \tag{4.1}$$

$$d(t) = d_0[1 + k_d \sin(2\omega_L t + \varphi_d)], \tag{4.2}$$

where d_0 is the dc component, k_d the relative amplitude and φ_d is the modulation phase of duty cycle modulation.

$$f(t) = f_0[1 + k_f \sin(2\omega_L t + \varphi_f)], \tag{4.3}$$

in which f_0 is the dc component and k_f the relative amplitude and φ_f is the modulation phase of switching frequency modulation.

4.1.1 PFC Stage Analysis

The analysis outlined in this subsection aims to present the main topologies applied to a single-phase voltage-mode controlled power factor pre-regulators, addressing the ARC characteristics regarding each one. It is important to highlight that although uncommon, the analysis of the ARC technique presented here also considers PFC pre-regulators with variable frequency, thus allowing a comparison with duty cycle modulation. The PFC pre-regulators that operate in DCM behave like voltage-followers, which allows them to achieve a high power factor at their input. However, depending on the converter, it is not possible to have an ideal sinusoidal current at the converter input, being that non-sinusoidal current condition the case of buck and boost-type topologies. On the other hand, the buck-boost type topologies can achieve a unity power factor when operating in DCM.

Some considerations are made to simplify the analysis as follows. All input current harmonics are suppressed by the EMI filter. The modulations of duty cycle and of switching frequency are not introduced simultaneously. The dc-linked capacitor (*i.e.*, output capacitor of the PFC stage) is large enough so that the bus voltage $v_B(t)$ can be treated as a constant value, and therefore does not interfere in the THD analysis of the converter with ARC technique.

The harmonic content of the input current can be obtained by using the Fourier series. The amplitude of the h-th order harmonic component of the converter input current can be calculated by (4.4). In this work, the THD of the input current was chosen to evaluate the power quality of the converter, as shown in (4.5).

$$I_h = \frac{2}{T_L}\int_0^{T_L} \sin(h\omega_L t) i_g(t) \mathrm{d}t, \tag{4.4}$$

in which T_L is the line period and h is the harmonics order of the line frequency.

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{4.5}$$

Furthermore, the deviation of THD of PFC pre-regulators, which is calculated according to (4.6), represents an interesting parameter for the generalized analysis of the ARC technique.

$$\Delta\mathrm{THD} = \mathrm{THD}_m - \mathrm{THD}_o, \tag{4.6}$$

in which THD_m is the THD of the pre-regulator with ARC technique and THD_o is the THD of the pre-regulator when the ARC technique is not used.

Since the input current of a converter using the ARC technique is also affected by LF large-signal modulation of the control variable, so that the power processed by the converter is also modified according to the values of such parameters. Therefore, the PFC stage inductance can be calculated by means of the power balance between the input and the output of the converter, as stated in (4.7), by considering the control variable modulation.

$$\frac{1}{T_L}\int_0^{T_L} v_g(t) i_g(t) \mathrm{d}t = \frac{P_o}{\eta}, \tag{4.7}$$

in which P_o is the output power and η is the global efficiency of the integrated converter.

4.1.1.1 *Buck PFC pre-regulator*

The input current of the PFC buck operating in DCM is given by (4.8) (WEI; BATARSEH, 1998). As can be seen,The input current is proportional to the input voltage, but only within the time interval in which the rectified line voltage is higher than the bus voltage. When $|v_g(t)|$ falls below the bus voltage, the input current is zero. The period in which the input current is not zero was named as conduction angle θ, whose definition is given by (4.9). The higher the conduction angle, the closest the input current to a perfect sine waveform, and the lower the harmonic content. Moreover, a minimum conduction angle of 130^o is necessary in order to ensure the compliance with the IEC 61000-3-2:2018 class C standard (DALLA COSTA et al., 2008).

$$i_g = \begin{cases} \dfrac{d^2(|v_g| - v_B)}{2fL_{bu}}, & \text{if } |v_g| > v_B \text{ and } v_g > 0 \\ -\dfrac{d^2(|v_g| - v_B)}{2fL_{bu}}, & \text{if } |v_g| > v_B \text{ and } v_g < 0 \\ 0, & \text{if } |v_g| \leq v_B \end{cases}. \tag{4.8}$$

in which L_{bu} is the buck inductance.

$$\theta = \pi - 2\sin^{-1}\left(\frac{V_B}{\sqrt{2}V_G}\right). \tag{4.9}$$

Figure 4.2 shows the deviation of THD, defined in (4.6), of buck PFC pre-regulator for two values of θ. For each conduction angle, a set of curves was generated, being each one characterized by a certain value of modulation angle and plotted for several values of relative amplitude modulation (k_d and k_f). In order to ensure the average power balance of the converter, for each point on the graph a new value of the buck inductance must be calculated so that the power delivered to the load remains constant. Inductance L_{bu} can be designed by means of power balance between the input and the output of the converter, as stated in (4.7). By replacing (4.8) in (4.7), the first stage inductance can be obtained by (4.10).

$$L_{bu} = \frac{\eta}{T_L P_o} \int_{t_1}^{\frac{T_L}{2}-t_1} \frac{v_g(|v_g| - v_B)d^2}{f} \mathrm{d}t, \tag{4.10}$$

in which t_1 is the instant of time given by:

$$t_1 = \frac{T_L}{2\pi} \sin^{-1}\left(\frac{V_B}{\sqrt{2}V_G}\right). \tag{4.11}$$

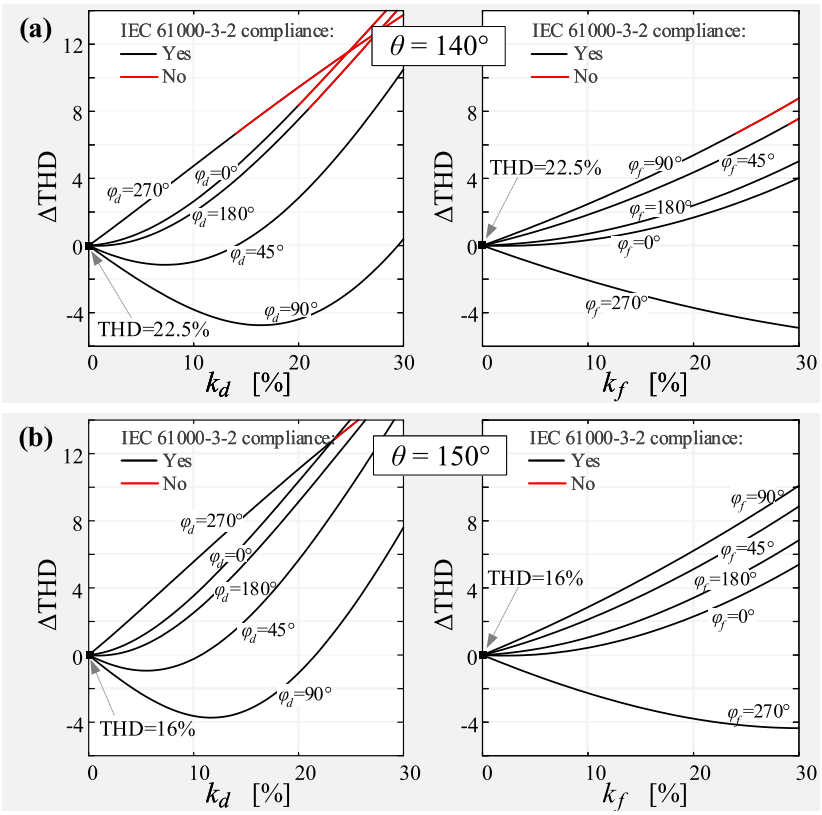


Figure 4.2 – Deviation of THD for buck PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency, considering a conduction angle of (a) $\theta = 140^o$ and (b) $\theta = 150^o$.

As can be noted in Figure 4.2, the cases that presented the harmonic components of the input current above the limits of the IEC 61000-3-2:2018 standard were highlighted in red. The ARC technique has little influence on the value of the THD when the relative amplitude of the modulation (k_d and k_f) is low, especially for modulation angles of 0^o and 180^o. On the other hand, the control variable modulation can be used to reduce the input current distortion. The highest THD reduction occurs when $\varphi_d = 90^o$ in $d(t)$ modulation and when $\varphi_f = 270^o$ in $f(t)$ modulation. In general, the THD of the converter is less sensitive to k_f when compared to k_d, thus allowing a larger $f(t)$ modulation. For example, with θ=150^o and φ_d=φ_f=0^o, ΔTHD=4% (*i.e.*, THD=20%) is obtained when k_d=11% or k_f=25%. As mentioned before, a minimum

conduction angle of 130^o is necessary for the conventional buck PFC pre-regulator in order to ensure the compliance with the IEC 61000-3-2:2018 class C standard. However, the value of this angle can be reduced with the ARC technique, i.e., the buck PFC pre-regulator with ARC can be used in applications that demand higher output voltages.

4.1.1.2 *Boost PFC pre-regulator*

According to (WEI; BATARSEH, 1998), the input current of the PFC boost operating in DCM can be rearranged as (6.10). It is possible to note that the input current of the PFC boost operating in DCM depends on the value of the bus voltage and therefore of the dc static gain (V_B/V_G). According to (ALMEIDA et al., 2015b), the converter only meets the requirements of the IEC 61000-3-2:2018 class C standard if the dc static gain is larger than 1.27. Similar to the buck converter analysis, the ΔTHD of boost pre-regulator with ARC technique for some values of V_B/V_G was presented in Figure 4.3. For each dc static gain, a set of curves was generated, being each one characterized by a certain value of modulation phase and plotted for several value of relative amplitude modulation. For each case in the graph the boost inductance is recalculated by (6.7) to keep the output power constant.

$$i_g = \frac{d^2}{2fL_{bo}}\left(\frac{v_g v_B}{v_B - |v_g|}\right). \tag{4.12}$$

where L_{bo} is the boost inductance, which can be calculated according to (6.7) in order to ensure the power balance of the converter.

$$L_{bo} = \frac{\eta}{T_L P_o}\int_0^{T_L} \frac{v_B d^2 v_g^2}{f(v_B - |v_g|)}\mathrm{d}t. \tag{4.13}$$

As verified in the buck converter, the input current distortion can be reduced by the control variable modulation, especially when $\varphi_d = 90^o$ in $d(t)$ modulation and when $\varphi_f = 270^o$ in $f(t)$ modulation. The results show that the deviation of the THD of boost pre-regulator can increase as the relative amplitude of modulation grows. However, this variation is smaller for $f(t)$ modulation when compared to $d(t)$ modulation. It is important to highlight that boost PFC pre-regulator in association with ARC technique can also meet the requirements of the IEC 61000-3-2:2018 class C standard with the dc static gain less than 1.27 if the purpose is not capacitance reduction.

4.1.1.3 *Buck-boost PFC pre-regulator*

Differing from the buck- and boost-type pre-regulators, the input current shape of the buck-boost PFC operating in DCM does not depend on the bus voltage, as given

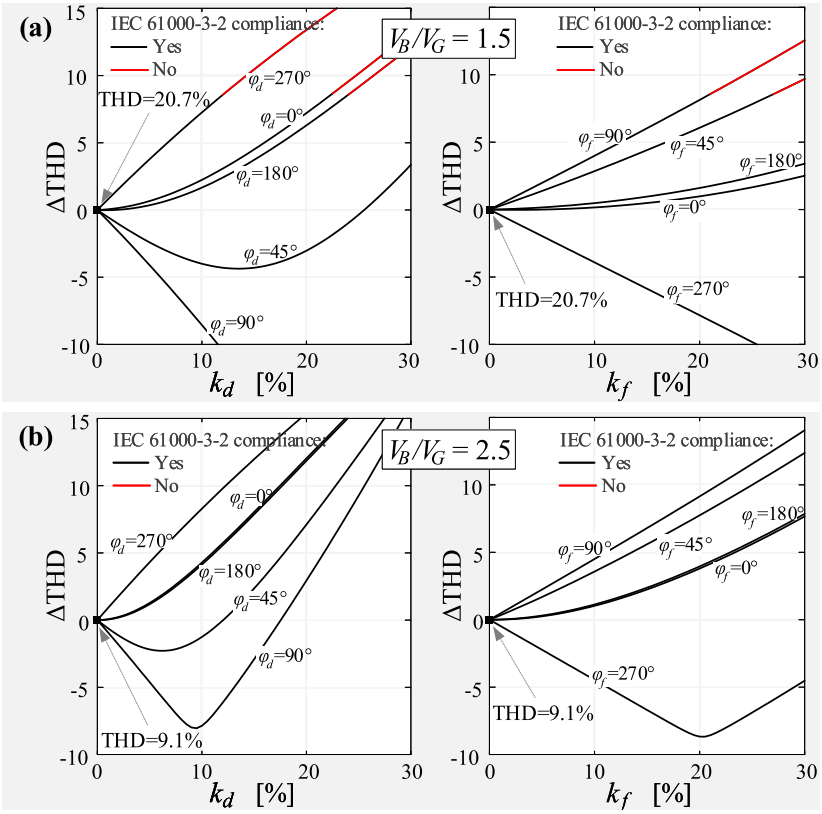


Figure 4.3 – Deviation of THD for boost PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency, considering a dc static gain of (a) $V_B/V_G = 1.5$ and (b) $V_B/V_G = 2.5$.

by (4.14) (WEI; BATARSEH, 1998). Therefore, the input current waveform is ideally sinusoidal if the duty cycle and the switching frequency are kept within a half line cycle.

$$i_g = \frac{d^2}{2fL_{bb}} v_g. \tag{4.14}$$

in which L_{bb} is the buck-boost inductance, which can be written as:

$$L_{bb} = \frac{\eta}{T_L P_o} \int_0^{T_L} \frac{d^2 v_g^2}{f} \mathrm{d}t. \tag{4.15}$$

Figure 4.4 shows the ΔTHD of buck-boost pre-regulator with ARC technique for several values of k_d and k_f, keeping the output power constant. Since the input current waveform is assumed sinusoidal, the deviation on THD for buck-boost pre-regulator always increases as the relative amplitude of large-signal modulation from ARC grows. The figure shows that the input current distortion does not depend significantly on the modulation angle when a large-signal modulation of the switching frequency is used. In addition, k_d has a greater influence than k_f on ΔTHD.

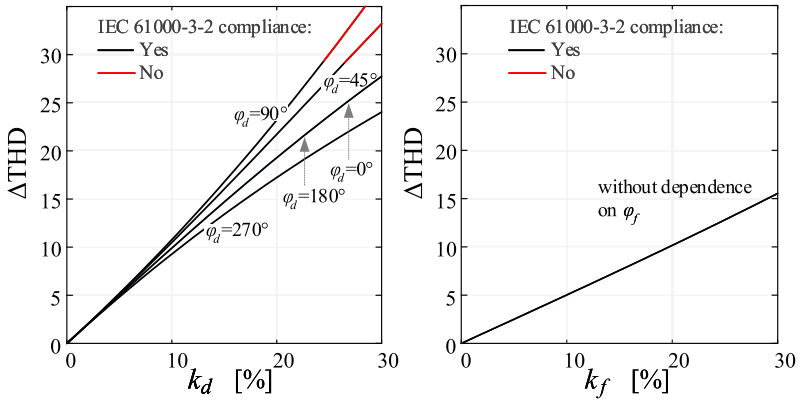


Figure 4.4 – Deviation of THD for buck-boost PFC pre-regulator operating in DCM with ARC technique modulating duty-cycle or switching frequency.

This subsection compared the more conventional and known ARC approach of duty-cycle large-signal modulation with a novel ARC technique based on the switching frequency large signal modulation, both applied to the three basic PFC pre-regulator topologies operated in DCM. The analyses showed that the $f(t)$ modulation has a lower impact on the power quality when compared with the duty cycle modulation. Furthermore, the large-signal modulation of the switching frequency can be used for the purpose of power quality improvement, which allows for the use of buck and boost topologies in compliance with the IEC 61000-3-2:2018 class C standard over a wide voltage gain range (V_B/V_G), or, as proposed in this paper, aiming the capacitance reduction in order to increase the power density and the lifespan of LED drivers. Regarding capacitance reduction, the LF ripple transmission must also be analyzed, thus the ARC technique can be evaluated according to the input current distortion and to the LF output current ripple in integrated off-line LED drivers.

4.1.2 **PC Stage Analysis**

This subsection presents how the deliberate modulation of the control variable impact the LF ripple transmission of the converters used as a PC stage. First, a converter sensitivity analysis will be presented in order to show the behavior of the converters with the control variable modulation. Thereafter, the values of the ARC parameters required to reduce the LF ripple will be measured and related to the THD analysis shown in the previous subsection.

Because in many drivers the bus voltage is significantly larger than the output voltage, step-down converters are tipically employed as the second stage in off-line LED drivers. Three topologies are studied in this section: buck and buck-boost operating in DCM, as well as LLC resonant converter with frequency modulation, which is a converter fairly common in off-line medium- and high-power LED drivers and has

become an industry standard in these off-line applications. In order to produce more generalized results, some parameters of the LLC converter were normalized as follows:

- Q is the normalized ac-side load resistance;
- λ is the inductance ratio, which can be found by dividing the series inductance by the magnetizing inductance;
- ω_n is the normalized design switching frequency;

In order to investigate the behavior of the output voltage of the converters, the normalized output voltage was evaluated for variations of the control variable, as shown in Figure 4.5. The ARC technique was disregarded in this analysis (k_d=k_f=0). In addition, the normalized control variables were defined as $c_d = D/D_{nom}$ and $c_f = f/f_{nom}$ for variations in the duty cycle and switching frequency, respectively. Figure 4.5(a) presents the behavior of the normalized output voltage V_o/V_{nom} of the buck and buck-boost converter designed for the same operating point (nominal duty cycle D_{nom} and nominal output voltage V_{nom}). Both converters present a quasi-linear behavior and have very similar curves and sensitivities.

Figure 4.5(b) shows the normalized output voltage of the LLC converter according to variations in the switching frequency for several values of λ. The results show that at the operating point the curve slope (*i.e.*, parametric sensitivity) increases as the inductance ratio grows. The lowest output voltage sensitivity occurs when $\lambda = 0$, which is a specific case of the LLC converter known as LC series resonant converter. It is important to highlight that the curves were obtained from the design methodology and the accurate modeling for an LLC resonant converter proposed in (FERRAZ et al., 2021), which is able to accurately predict the LED current.

Figure 4.5(c) depicts the normalized output voltage for several values of Q. As can be seen, the impact of the quality factor becomes negligible around the operating point. Figure 4.5(d) presents the normalized output voltage according to variations in the switching frequency for several values of normalized design switching frequency. As expected, the LLC converter operates very close to the maximum dc gain as ω_n reduces, a case that should be avoided to ensure operation under zero voltage switching (ZVS) conditions (inductive tank characteristic). On the other hand, the LLC converter is typically designed to operate at the series resonant frequency (ω_n=1), thus obtaining greater efficiency and better power quality. This case allows a wide variation of the switching frequency value while preserving the ZVS operation. In this sense, Figure 4.5 shows that the inductance ratio has a major influence on the LLC converter sensitivity.

In order to quantify the sensitivity related to converters used as PC stage, a case with $P_o = 96.6$ W, $V_o = 138$ V, $V_B = 450$ V and $f(t) = 70$ kHz was investigated

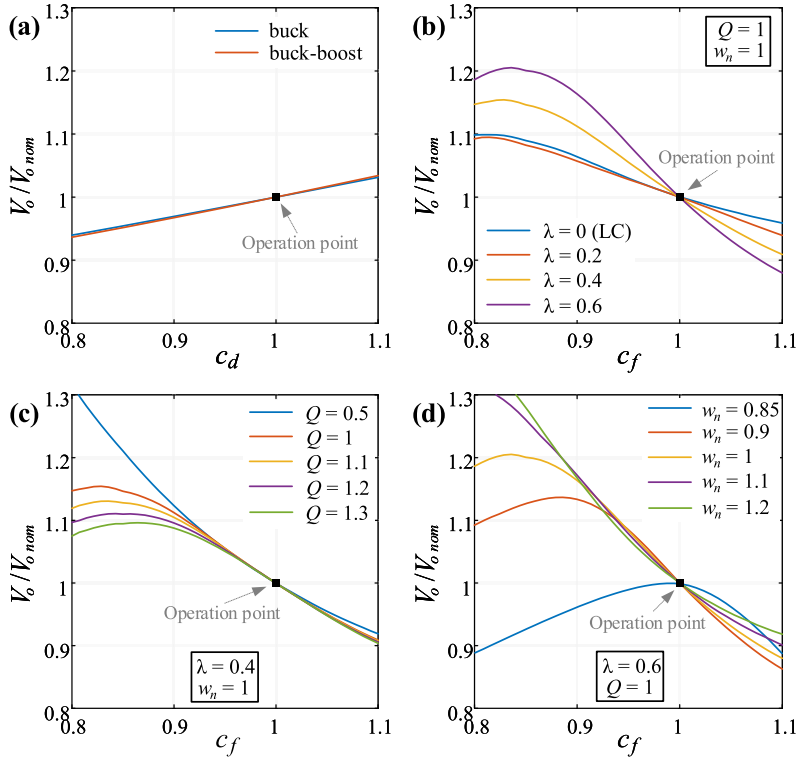


Figure 4.5 – Normalized output voltage of converters as PC stage. (a) buck and buck-boost converters; (b) LLC converter for variations of λ; (c) LLC converter for variations of Q and (d) LLC converter for variations of ω_n.

considering the converters evaluated in Figure 4.5. The sensitivity can be calculated as the partial derivative of the LLC average output voltage with respect to the normalized switching frequency, which is denoted as $\partial V_o/\partial c_f$. Figure 4.6(a) shows the sensitivity analysis in absolute values for several values of inductance ratio. As can be seen, the sensitivity of the LLC converter increases as λ grows. Figure 4.6(b) shows the sensitivity analysis in absolute values for several values of ω_n. When the LLC converter is operating close to the maximum dc gain, the sensitivity increases as ω_n grows. However, in the region in which the converter is usually designed to operate, this sensitivity reduces with increasing normalized frequency.

Regarding the hard-switching dc-dc converters, the sensitivity to duty cycle can be obtained by the partial derivative of the output voltage with respect to the normalized duty cycle ($\partial V_o/\partial c_d$). In this way, the sensitivity to duty cycle of the buck and buck-boost converter are constant and equal to 43 V and 46 V, respectively. Although uncommon, the $f(t)$ modulation was also evaluated in the hard-switching topologies (*i.e.*, buck and buck-boost). In these examples, $|\partial V_o/\partial c_f|$ of the buck and buck-boost converter are equal to 22.1 V and 23.5 V, respectively. Therefore, these hard-switching converters have a sensitivity to $d(t)$ modulation approximately twice that to $f(t)$ modulation. On the other hand, load-resonant converters can be considered more sensitive than hard-switching converters, thus requiring a lower relative amplitude

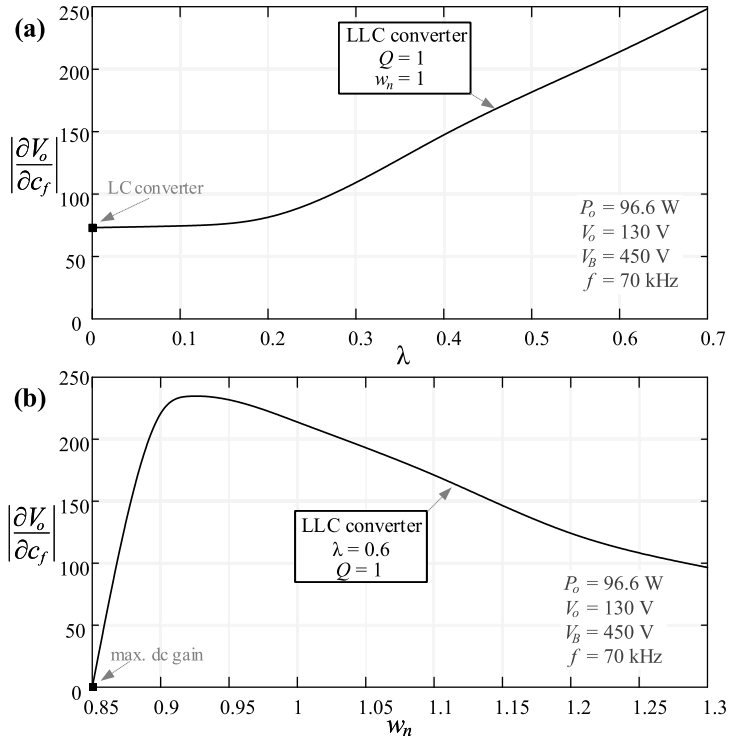


Figure 4.6 – Sensitivity analysis of the LLC converter used as the PC stage for several values of (a) λ and (b) ω_n.

modulation - thus a lower control effort - for achieving the same ripple reduction.

Finally, the previously studied converters were evaluated with the ARC technique in order to show the effect of large-signal modulation on the output ripple reduction. Table 4.1 shows k_d and k_f modulation amplitudes required to reduce the LF ripple in the LED current for several cases of dc-dc converters used as a PC stage. These converters are supplying an LED lamp with dynamic resistance $r_d = 12\ \Omega$ and nominal threshold voltage $V_t = 129.6$ V. The values of the average output current and the output current ripple were 700 mA for this analysis when k_d and k_f are equal to zero, thus obtaining a LF current ripple of 100%. The value of the bus ripple that ensures the low-frequency ripple criterion was chosen for each converter. In order to obtain the maximum ripple reduction, the modulation phase was chosen so that $d(t)$ is completely out of phase with the ac portion of the bus voltage of the hard-switching dc-dc converters. In other words, $\varphi_d = 0\%$ since the phase of the ac portion of the bus voltage is equal to 180^o. Regarding the switching frequency modulation, the modulation phase was chosen so that $f(t)$ is in phase with the ac portion of the bus voltage, *i.e.*, $\varphi_f = 180^o$.

The results show that ARC technique has a better performance in terms of ripple reduction in converters with higher sensitivity. For example, the output current ripple of 50% is obtained when $k_d = 13\%$ for the buck converter and $k_f = 1\%$ for the LLC resonant converter with $\lambda = 0.6$. For the same output current ripple, load-resonant

converters with frequency modulation require a lower relative modulation amplitude when compared to conventional converters.

In order to show the behavior of the THD of integrated converters with PC stages listed in Table 4.1, the parameters of ARC technique for an output ripple of 50% were evaluated according to subsection 4.1.1 and the values of ΔTHD are given in Table 4.2 for each combination of PFC and PC stages. For example, by considering the PFC buck-boost integrated with the buck, the output current ripple of 50 % is obtained with a duty cycle modulation that generates a THD increase of 12.8%. On the other hand, the same output ripple is obtained with ΔTHD of only 0.5% if the LLC resonant converter with $\lambda = 0.6$ is used as PC stage with frequency-based ARC. Regarding the hard-switching converters, although k_f is higher than k_d, the values of ΔTHD are similar since the $f(t)$ modulation has a lower impact on the THD when compared with the $d(t)$ modulation. Thus, the ARC technique applied to the switching frequency is also an alternative for the evaluated non-resonant converters, although the design of such topologies with a large frequency modulation can be somewhat difficult and can actually increase the volume of some passive elements. On the other hand, when a load-resonant PC stage is used, the frequency-based ARC is an excellent alternative, since it allows for a large capacitance reduction with a very small impact on the THD. This occurs owing to the high modulation sensitivity of those topologies. Furthermore, these converters have higher efficiency when compared to hard-switching converters.

In low-power applications, when the designer pursues simpler topologies composed of only one stage, the duty cycle modulation can be more interesting. On the other hand, the proposed frequency-based ARC yields better results when two-stage converters are needed since it allows for a huge capacitance reduction while maintaining a low input current distortion and a high overall efficiency.

Table 4.1 – Parameters of ARC Technique (k_d or k_f) for Output Ripple Reduction

relative amplitude of the modulation (%)		PC stages	$\Delta I_{o\%}$ 100%	75%	50%	25%
	k_d see (4.2)	buck	0%	7%	13%	20%
		buck-boost	0%	6.7%	13.5%	20.5%
	k_f see (4.3)	buck	0%	14%	27.5%	40%
		buck-boost	0%	14%	27.5%	39.8%
		LC ($\lambda = 0$)	0%	2%	4.2%	6.8%
		LLC ($\lambda = 0.2$)	0%	1.5%	2.5%	4%
		LLC ($\lambda = 0.4$)	0%	0.75%	1.5%	2.2%
		LLC ($\lambda = 0.6$)	0%	0.5%	1%	1.5%

Table 4.2 – ΔTHD of Integrated Converters with ARC Technique for $\Delta I_{o\%}$=50%

PC stages	control variable	ΔTHD - see (4.6) buck PFC	boost PFC	buck-boost PFC
buck	duty cycle	5.4%	6.5%	12.8%
buck-boost		5.7%	6.9%	13.3%
buck	frequency	5.9%	6.8%	13.9%
buck-boost		5.9%	6.8%	13.9%
LC ($\lambda = 0$)		0.26%	0.22%	2.1%
LLC ($\lambda = 0.2$)		0.13%	0.08%	1.25%
LLC ($\lambda = 0.4$)		0.06%	0.03%	0.75%
LLC ($\lambda = 0.6$)		0.04%	0.02%	0.5%

4.2 SIMULATED RESULTS OF INTEGRATED CONVERTERS WITH ACTIVE RIPPLE COMPENSATION TECHNIQUE

As mentioned before, PFC and PC stages were discussed separately in order to simplify the analysis. Thus, the values of the ARC parameters used for output ripple reduction were evaluated in the PC stage (Table 4.1). Thereafter, the PFC stage with duty cycle or frequency modulation was considered to calculate the THD (Table 4.2 shows ΔTHD for $\Delta I_{o\%}$=50%). In order to validate the theoretical results developed in the last section, a PSIM simulation of some integrated converters was carried out, and four topologies were selected:

- Integrated buck flyback converter (IBuFly);
- Integrated double buck-boost (IDBB);
- PFC buck-boost integrating HB LLC converter (IBbLLC);
- PFC boost integrating HB LLC converter (IBoLLC);

These converters are supplying an LED lamp with dynamic resistance $r_d = 12\ \Omega$ and nominal threshold voltage $V_t = 129.6$ V. The values of the average output current and the output current ripple were 700 mA for this analysis when k_d and k_f are equal to zero, thus obtaining a LF current ripple of 100%. Thereafter, the relative amplitude of the modulation selected to obtain a LF current ripple of 50% according to Table 4.1. Therefore, k_d is equal to 13.5% in the IBuFly and IDBB converters that have a buck-boost type topology as PC stage. In the case of IBbLLC and IBoLLC converters, k_f is equal to 1.5% since the LLC converter with λ=0.4 was chosen for the PC stage.

4.2.1 **Integrated buck flyback converter (IBuFly)**

Figure 4.7 shows the circuit used in the simulation of the IBuFly converter, as well as the control structure that aims to reproduce the duty cycle function $d(t)$ (see (4.2)). In order to ensure that the converter operates in DCM, the instantaneous duty cycle must be lower than the critical duty cycle value, which is given by (4.16). Choosing transformation relationship n equal to 1 and $V_B = V_o = 132$ V, the value of d_0=0.35 was assumed. The values of inductances can be obtained by means of the power balance in each stage of the circuit by considering that the input is a 220-V/60-Hz mains. Thus, L_{bu} and L_m can be calculated by (4.10) and (4.17), respectively. The bus capacitance used in this simulation was 28 μF.

$$D_{crit} = \frac{V_o}{nV_B + V_o}, \tag{4.16}$$

$$L_m = \frac{V_B^2 d_0^2}{2P_o f_s}. \tag{4.17}$$

Figure 4.8 presents the main waveforms obtained from the simulation of IBuFly converter with ARC technique. It is possible to note that the input current distortion is higher when the ARC technique is used. The deviation of THD was 5.4% in this simulation, which is close to theoretical results (5.7% shown in Table 4.2). In addition, the control variable $d(t)$ is completely out of phase with the ac portion of the bus voltage in order to obtain the maximum ripple reduction. In this simulation, the LF ripple in the LED current was 55%, which is in accordance with the table 4.1.

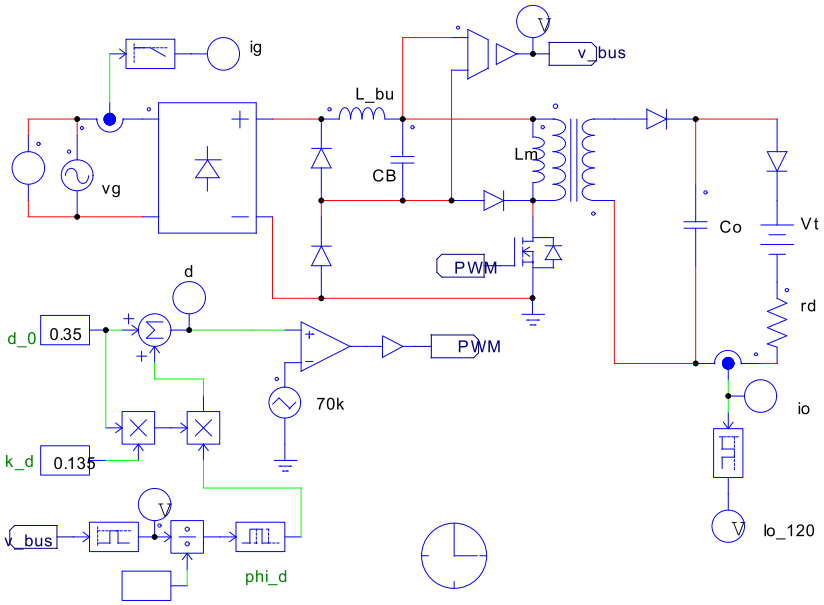


Figure 4.7 – Circuit used in the simulation of the IBuFly converter.

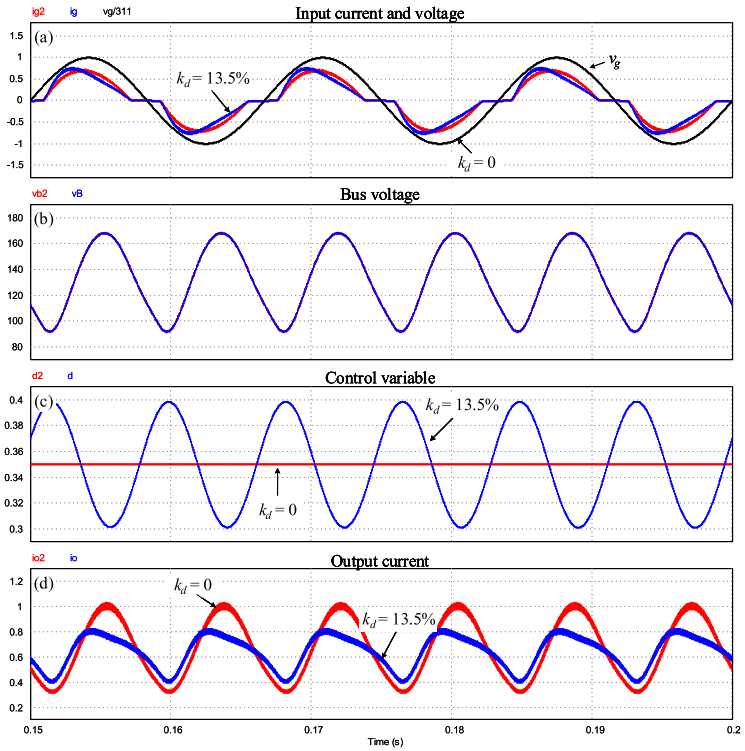


Figure 4.8 – Simulation results of the IBuFly converter.

4.2.2 **Integrated double buck-boost (IDBB)**

The circuit used in the simulation of the IDBB converter is shown in Figure 4.9 and has the same control structure as the previous converter. The instantaneous duty cycle must be lower than the critical duty cycle value, which is given by (4.16) when n equal to 1, in order to ensure that the converter operates in DCM. The value of d_0=0.22 was assumed by choosing V_B = 300 V. The value of the inductance L_2 can also be calculated by (4.17) while L_1 is given by (4.15). The bus capacitance used in this simulation was 4.5 μF.

Figure 4.10 shows the main waveforms obtained from the simulation of IDBB converter with ARC technique. In this converter, the deviation of THD was 11.8%, which is close to the 13.3% predicted by the theoretical analysis. In addition, the LF ripple in the LED current was 53.5%.

4.2.3 **PFC buck-boost integrating HB LLC converter**

Figure 4.11 shows the circuit used in the simulation of the IBbLLC converter. One can note that a ”C block”component was added to the circuit in order to implement the control signal of the MOSFETs with frequency modulation. The code used in the C-block can be seen in Appendix A. PC stage is designed according to chapter 3 for an inductance ratio of λ = 0.4 and by considering a average bus voltage of 450 V.

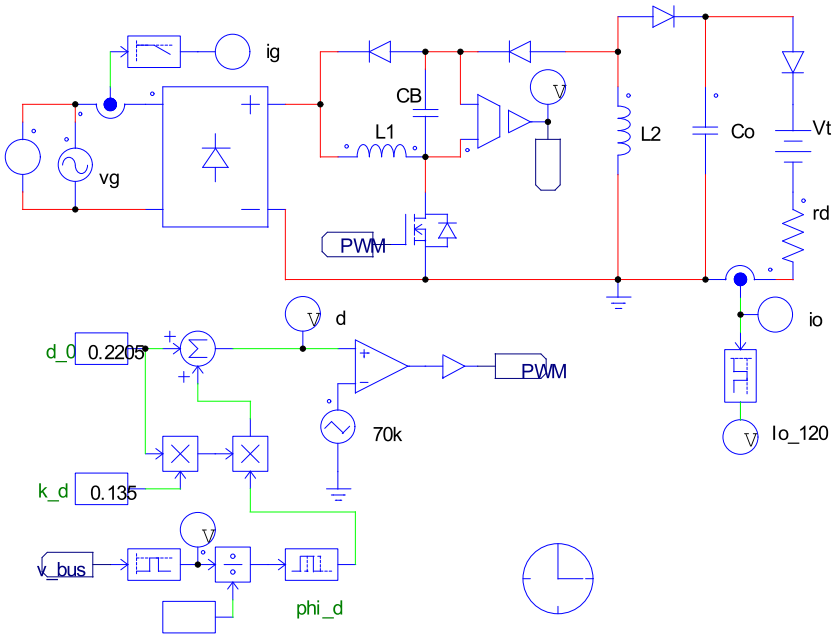


Figure 4.9 – Circuit used in the simulation of the IDBB converter.

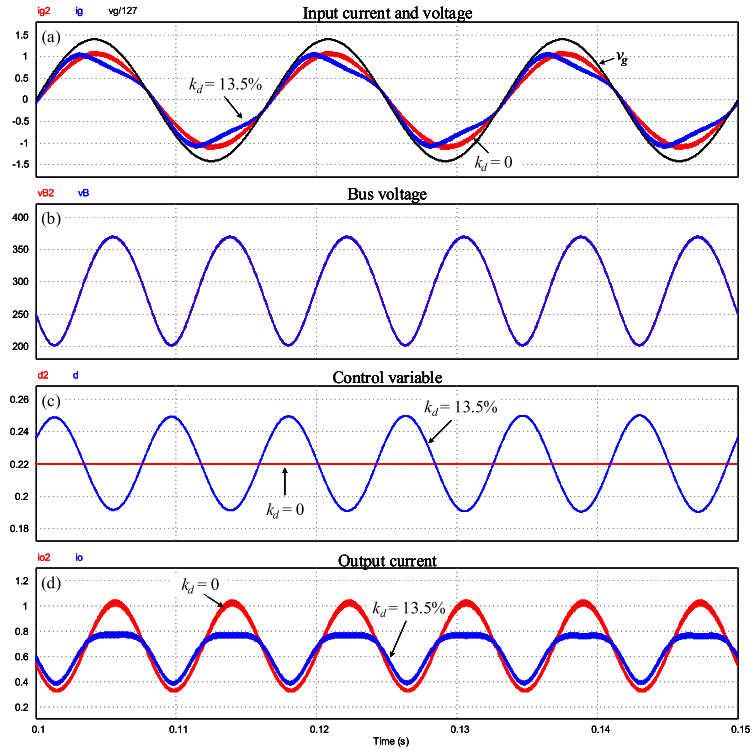


Figure 4.10 – Simulation results of the IDBB converter.

The value of the inductance L_{bb} can also be calculated by (4.15). The bus capacitance chosen was 20 μF.

The main waveforms obtained from the simulation of IBbLLC converter with ARC technique are presented in Figure 4.12. In contrast to the conventional approach, the frequency-based ARC technique has only a 0.17% increase in THD, which prac-

tically does not change the waveform of the input current. Furthermore, the control variable $f(t)$ is in phase with the ac portion of the bus voltage in order to obtain the maximum ripple reduction. The LF ripple in the LED current of 52.3% was obtained in this simulation.

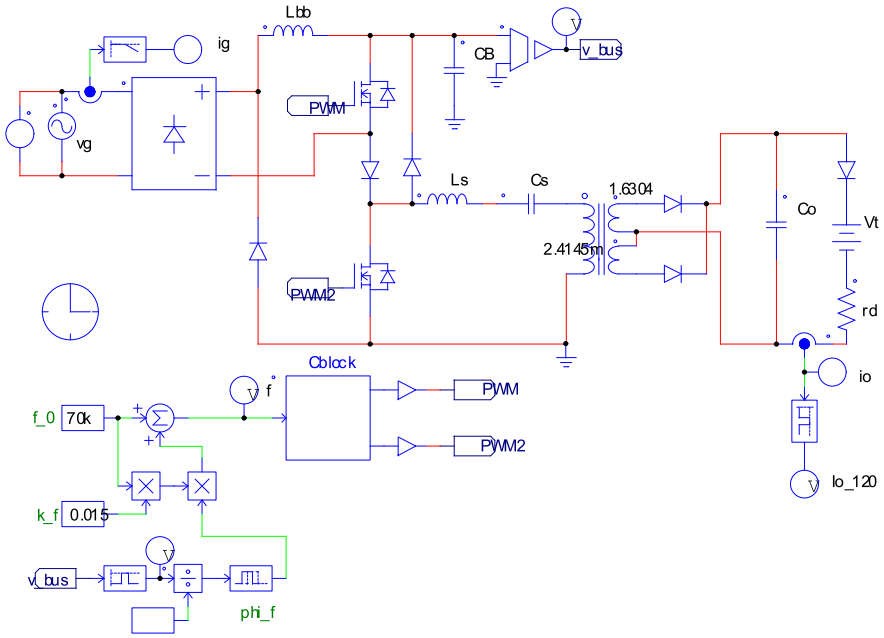


Figure 4.11 – Circuit used in the simulation of the IBbLLC converter.

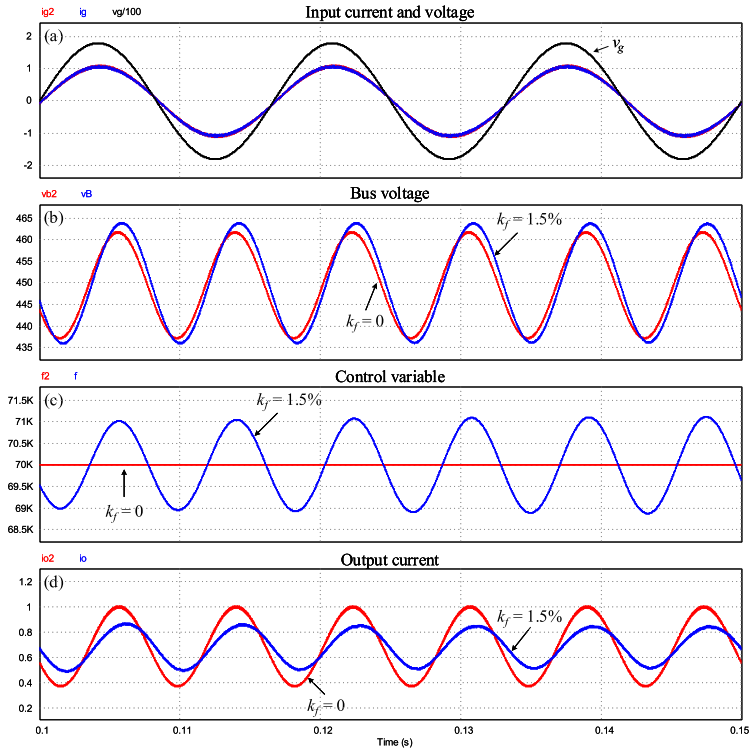


Figure 4.12 – Simulation results of the IBbLLC converter.

4.2.4 **PFC boost integrating HB LLC converter**

Figure 4.13 shows the circuit used in the simulation of the IBoLLC converter. The parameters of the PC stage are the same as for the IBbLLC converter and the value of the inductance L_{bo} can be calculated by (6.7). The bus capacitance of 20 μF was used in simulation.

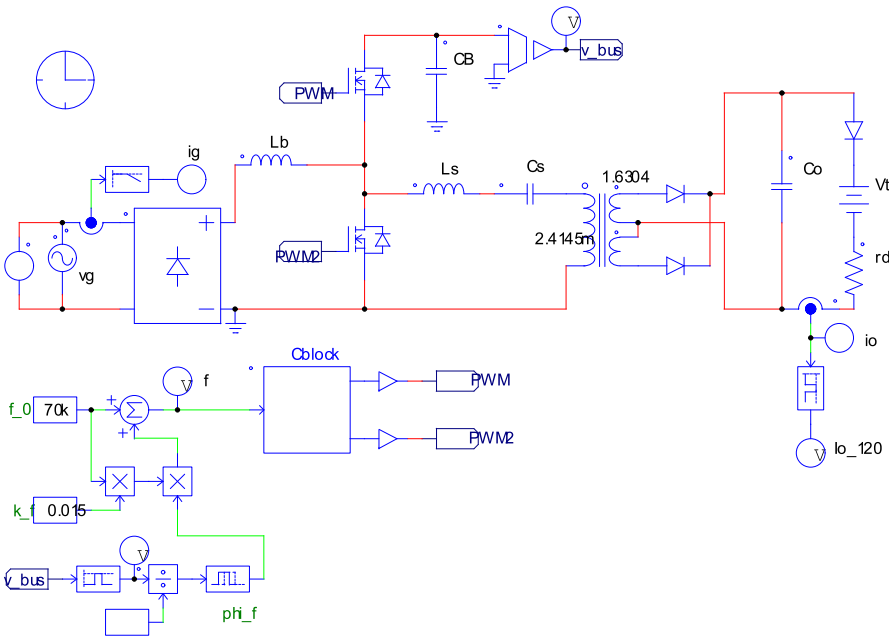


Figure 4.13 – Circuit used in the simulation of the IBoLLC converter.

Figure 4.14 presents the main waveforms obtained from the simulation of IBoLLC converter with ARC technique. In this simulation, the frequency-based ARC technique has only a 0.027% increase in THD, which is very close to the 0.03% presented in table 4.2. The LF ripple in the LED current was 52.8%, which is in accordance with the Table 4.1.

In order to compare the four topologies simulated in this section, the performance analysis tool was used, as shown in Figure 4.15. The efficiency values considered in this analysis were the typical values for each operating condition, whether in hard-switching or soft-switching. The converters performed well in terms of reliability, power density, and cost due to the capacitance reduction control technique that was applied to all of them. Since the proposed frequency-based ARC technique allows for a large capacitance reduction with a very small impact on the THD, IBbLLC and IBoLLC converters yield better results in terms of ac input power quality. In addition, whereas these converters enable soft switching, they are more efficient than IDBB and IbuFly converter.

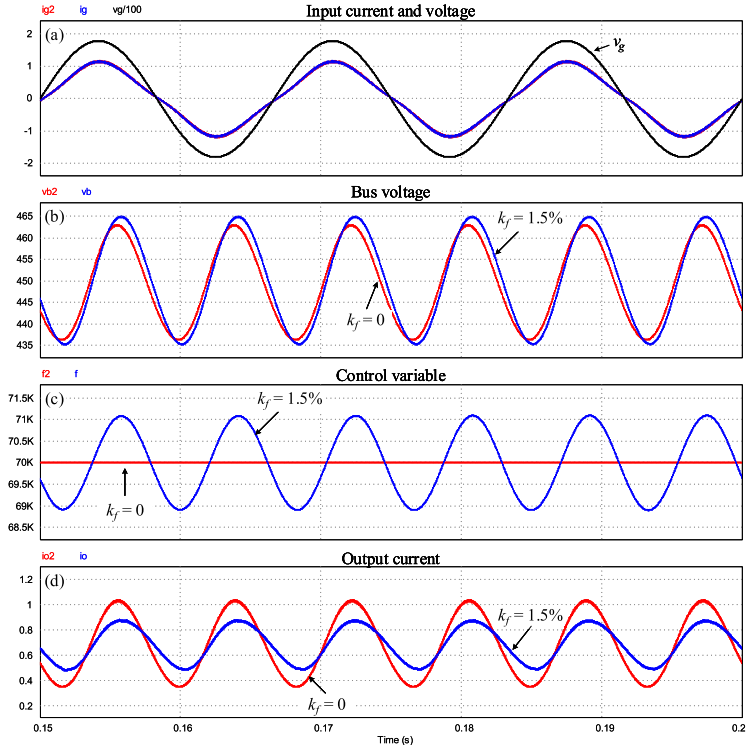


Figure 4.14 – Simulation results of the IBoLLC converter.

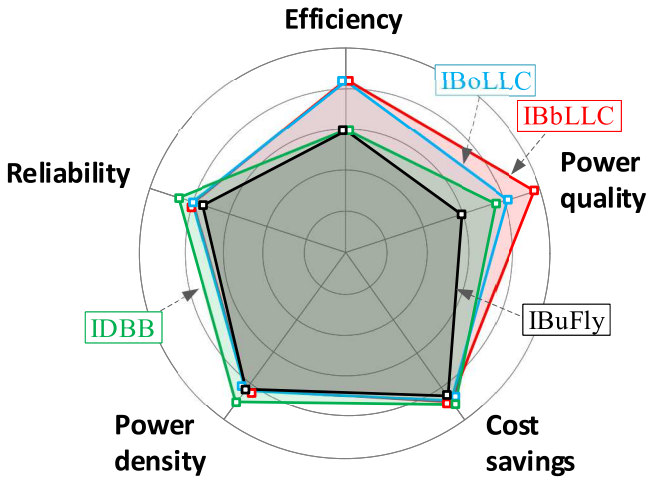


Figure 4.15 – Performance analysis of simulated converters with ARC technique.

4.3 SUMMARY OF THE CHAPTER

This chapter presented the generalized analysis of the active ripple compensation approach at the control variable of integrated off-line LED drivers. The theoretical analysis described the operation of several topologies under the modulation of switching frequency and duty cycle. The duty cycle modulation, which has been explored in some works, was analyzed for several topologies showing that it has a good capacitance reduction potential. However, all of them presenting a relevant drawback: the significant

increase in the THD. The low sensitivity of the LF ripple to duty cycle modulation implies that to achieve a good ripple reduction, a significant modulation in the control variable must be employed, causing a large distortion in the input current. On the contrary, this chapter proposed an alternative approach based on the modulation of the switching frequency, which allows for a large capacitance reduction without affecting the THD significantly when applied to converters with a load-resonant PC stage. Simulated results verified the theoretical analysis of the frequency-based ARC technique applied to basic integrated topologies operated in DCM. This alternative also increases the overall LED driver efficiency when compared to integrated converters in which both stages operate under hard-switching condition.

5 CASE OF STUDY OF AN OFF-LINE LED DRIVER WITH FREQUENCY-BASED ARC TECHNIQUE

The previous chapter introduced the frequency-based ARC technique for capacitance reduction in integrated off-line LED drivers with a load-resonant PC stage, which has high modulation sensitivity allowing for a large capacitance reduction with a very small impact on the THD. On the other hand, this chapter proposes an alternative design methodology for an integrated off-line LED drivers with a load-resonant PC stage, considering the frequency-based ARC approach. Furthermore, a design example of this converter is presented in order to validate experimentally the proposed frequency-based ARC technique.

The topology chosen in this work was obtained by integrating a totem-pole bridgeless boost PFC and a half-bridge LC series resonant converter, as illustrated in Figure 5.1, which is referred by BBLC in this document. The bridgeless input configuration achieves a better efficiency when compared with the conventional diode bridge configuration, owing to reduced conduction losses (HUBER; JANG; JOVANOVIC, 2008). Therefore, totem-pole bridgeless boost PFC is a simple alternative concerning the improvement of the efficiency. It is worth noting that the topology chosen for the PC stage is the one with the lowest sensitivity among the LLC converters evaluated in the previous chapter, being considered the worst case of load-resonant converters, which have high efficiency. In other words, this topology needs a higher modulation amplitude for capacitance reduction, thus resulting in higher input current distortion. Therefore, this converter was chosen in order to show the higher influence of the frequency modulation on the input current of the integrated off-line LED drivers based on load-resonant converters.

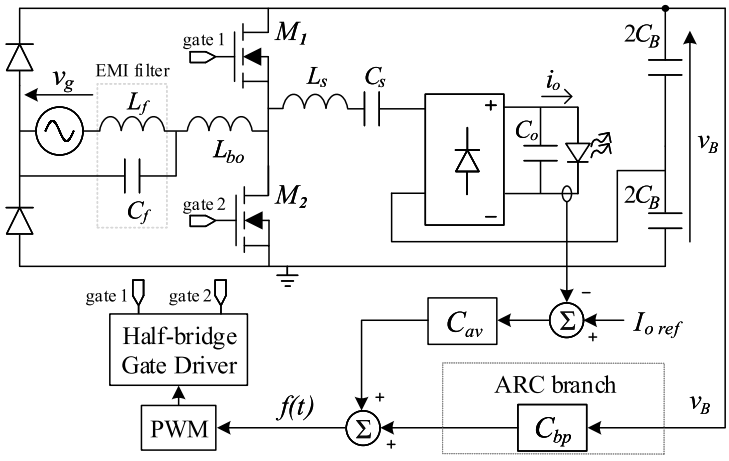


Figure 5.1 – Integrated Off-line LED driver based on the LC resonant converter with ARC technique in the switching frequency.

The PC stage operates above the series resonant frequency, thus resulting in ZVS and high efficiency. As can be seen in Figure 5.1, the ARC approach requires an additional compensator branch, C_{bp}, and one voltage sensor for its proper operation as compared to a typical control technique. The compensator C_{av} is used to synthesize the value of f_0 while the block C_{bp} generates the oscillating portion of $f(t)$ in phase with the ac portion of the bus voltage.

5.1 MATHEMATICAL DESCRIPTION OF THE CONVERTER

The design of the BBLC converter with ARC must meet both the IEC-61000-3-2 standard, and the output current requirements, which must ensure that its average value and ripple stay within the desired values in order to assure the lighting quality (LEHMAN; WILKINS, 2014). Therefore, the mathematical analysis presented in this work focuses on these two aspects. According to (ALMEIDA et al., 2015b), the PFC stage can be treated as a conventional boost DCM PFC for each line half-cycle, which simplifies the analysis and design of the converter. Therefore, as presented in chapter 4, the input current of the off-line converter can be rearranged as (6.10), in which $d(t)$ is equal to the duty cycle constant value, also denoted by D.

On the other hand, as in the previous chapter, the line voltage can be defined by its RMS value V_G and angular frequency ω_L:

$$v_g(t) = \sqrt{2}V_G \sin(\omega_L t). \tag{5.1}$$

The harmonic content of the input current can be obtained by using the Fourier series. The amplitude of the h-th order harmonic component of the converter input current can be calculated by (5.2).

$$I_h = \frac{D^2}{L_b T_L} \int_0^{T_L} \frac{\sin(h\omega_L t) v_B(t) v_g(t)}{f(t)(v_B(t) - |v_g(t)|)} \mathrm{d}t, \tag{5.2}$$

in which T_L is the line period and h is the harmonics order of the fundamental line frequency.

Regarding the converter output, the output voltage of the converter ($v_o(t)$) can be expressed by the classical piecewise-linear model of the LED string which is described by (5.3).

$$v_o(t) = i_o(t) r_d + V_t. \tag{5.3}$$

In this analysis, the bus voltage $v_B(t)$ can not be treated as a constant value to evaluate the large-signal low-frequency behavior of the converter and allow the proper

sizing of the bus capacitance. In order to evaluate the behavior of the main variables of the circuit (*e.g.*, the output current), the large-signal low-frequency model of the BBLC converter can be used. This model can be seen in Figure 5.2 in accordance to (Soares; Alonso; Braga, 2018), in which it is possible to observe that the energy transfer in the converter is performed in two stages. At first, the input power $p(t)$ is delivered to the dc bus via the PFC stage and then the PC stage transfers the dc bus power to the output. The losses in the power conversion process are represented by the efficiencies of the input and the output stages, which are η_{PFC} and η_{PC}, respectively. For the sake of simplicity, the analysis presented in this work considers that the capacitance C_o has no influence on the low-frequency ripple filtering, since this element is normally sized only to filter the high-frequency switching ripple.

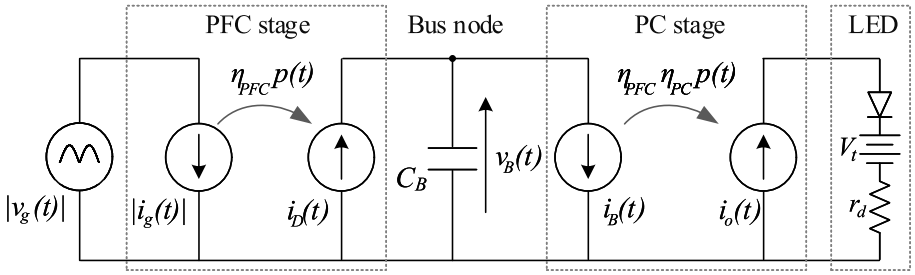


Figure 5.2 – Large-signal low-frequency model of the BBLC converter.

In order to obtain a high efficiency, the converter is designed to operate in the ZVS region, by choosing the normalized switching frequency ω_n, which can be written as in (5.4), so that all $f(t)$ values are above the resonant frequency. It is important to highlight that, as presented in Ferraz et al. (2018), the first harmonic approximation (FHA) for LC converter does not lead to accurate results when the load has a voltage-source characteristic, such as an LED, especially when the circuit operates far from the resonant frequency. Therefore, in order to represent the large-signal low-frequency behavior of the converter more faithfully, an accurate mathematical modeling of the PC stage has to be used. According to Ferraz et al. (2018), the equation system describing the behavior of the LC series resonant converter is given by the set of state-space equations represented in (5.5). The solution of this system can be obtained by means of the the numerical integration of this non-linear set of differential equations.

$$\omega_n = 2\pi f_0 \sqrt{L_s C_s}. \tag{5.4}$$

$$\begin{cases} \dfrac{\mathrm{d}i_s(t)}{\mathrm{d}t} = \dfrac{1}{L_s}(v_{HB}(t) - v_s(t) - v_o(t)\mathrm{sgn}[i_s(t)] \\ \dfrac{\mathrm{d}v_s(t)}{\mathrm{d}t} = \dfrac{1}{C_s}i_s(t) \\ \dfrac{\mathrm{d}v_o(t)}{\mathrm{d}t} = \dfrac{1}{C_o}\left(|i_s(t)| - \dfrac{v_o(t) - V_t}{r_d}\right) \end{cases}, \tag{5.5}$$

in which $i_s(t)$ represents the current flowing through the resonant tank, $v_s(t)$ is the voltage of the series capacitance and $v_{HB}(t)$ is the input voltage of the resonant tank, which is generated by the half-bridge inverter and can be written as

$$v_{HB}(t) = \frac{v_B(t)}{2}(\mathrm{sgn}[\sin(2\pi f(t)t)] + 1), \tag{5.6}$$

where *sgn()* is the sign function, defined as:

$$\mathrm{sgn}(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ -1, & \text{if } x < 0 \end{cases} \tag{5.7}$$

In order to simplify the investigation of the ARCT in the BBLC converter, the PC transconductance gain (relationship between the output current and the bus voltage) can be defined by (5.8). The value of this particular gain depends on both the instantaneous switching frequency and the instantaneous bus voltage and, therefore, it is mandatory for BBLC analysis with ARC technique. Thus, the value of the $G(v_B,f)$ can be achieved by replacing $f(t)$ and $v_B(t)$ in the accurate model of LC resonant converter presented in (5.5), solving this system using a numerical integration.

$$G(v_B,f) = \frac{i_o(t)}{v_B(t)}. \tag{5.8}$$

Regarding the bus instantaneous power of the BBLC converter, (5.9) can be found by evaluating the instantaneous power balance in the second stage of the LED driver. By using (5.8) and (5.3) in (5.9) and solving for the bus current $i_B(t)$, the expression of the input current of the PC stage is found, as shown in (6.12).

$$i_B(t)v_B(t) = \frac{i_o(t)v_o(t)}{\eta_{PC}}. \tag{5.9}$$

$$i_B(t) = v_B(t)\frac{G(v_B,f)^2 r_d}{\eta_{PC}} + \frac{G(v_B,f)V_t}{\eta_{PC}}. \tag{5.10}$$

As can be derived from Figure 5.2 using the bus node current Kirchhoff's law, the differential equation of the bus voltage $v_B(t)$ is described by (5.11) in terms of the output current of the PFC stage $i_D(t)$, which is described by (6.11) according to (ZHANG; SPENCER, 2011).

$$\frac{\mathrm{d}v_B(t)}{\mathrm{d}t} = \frac{1}{C_B}\left(i_D(t) - i_B(t)\right). \tag{5.11}$$

$$i_D(t) = \frac{\eta_{PFC} v_g(t)^2 D^2}{2L_b f(t)(v_B(t) - v_g(t))}. \tag{5.12}$$

where L_b is the inductance of the PFC stage (i.e., the boost inductance).

The inexistence of a closed-form solution for the bus voltage implies that this variable must be solved numerically. Once the $v_B(t)$ is known, the output current can be calculated by (5.13).

$$i_o(t) = v_B(t)G(v_B,f). \tag{5.13}$$

In order to obtain either the bus voltage and the output current, the numerical method shown in Soares et al. (2017) can be used to solve the equation system composed by (5.11) and (6.11). Hence, the composite midpoint rule (LEVY, 2010) was the numerical integration technique employed, which yields:

$$v_B(t_f) = \int_{t_1}^{t_f} \frac{\mathrm{d}v_B(t)}{\mathrm{d}t}\mathrm{d}t \approx \sum_{k=0}^{N_s-1} s_t \frac{\Delta v_B(t_k)}{\Delta t}, \tag{5.14}$$

where the parameters of the numerical solution procedure are:

- t_1 - initial time ;
- t_f - final time;
- s_t - time step size;
- N_s - number of steps, defined in (5.15);
- t_k - k$^{\text{th}}$ time step, defined in (5.16).

$$N_s = \frac{t_f - t_1}{s_t}. \tag{5.15}$$

$$t_k(k) = t1 + ks_t. \tag{5.16}$$

The main variables of the BBLC converter outlined in this section are obtained simultaneously. For example, for each $v_B(t_k)$, the value of the instantaneous output current $i_o(t_k)$ is calculated by using (5.8). It is worth noting that the accurate gain of the resonant PC stage must be employed for each calculated point. Therefore, the gain

$M(f,v_B)$, which takes on a different value for each combination of switching frequency and bus voltage, is an input parameter in this analysis. Figure 5.3 shows a MATLAB pseudo-code of a function that performs this calculation.

```
function [i_g, v_B, i_o] = CalcBBLC(V_G,f_L,D,f_o,k_f,φ_2,L_b,C_B,r_d,V_t,η_PFC,η_PC,M)

% Auxiliary parameters
s_t = 1/(f_L * 500);
t_1 = 0;
t_f = 9/(2 * f_L);
N_s = round((t_f − t_1)/s_t);
ω_L = 2 * π * f_L;
time = t_1 : s_t : t_f;
i_g = zeros(1,N_s);
v_B = zeros(1,N_s);
i_o = zeros(1,N_s);
v_B(1) = 700;

for  k = 1 : N_s
     t = time(k);
     f = f_0 + k_f * f_0 * sin(2 * ω_L * t + φ_2);
     v_g = √2 * V_G * sin(ω_L * t);
     i_D = v_g^2 * D^2/(2 * L_b * f * (abs(abs(v_g) − v_B(k))));

     % Solution of the bus voltage
     M_k = M(f,v_B(k));
     i_B = M_k^2 * r_d * v_B(k)/η_PC + M_k * V_t/η_PC;
     v_B(k + 1) = v_B(k) + s_t * 1/C_B * (η_PFC * i_D − i_B);

     % Solution of the input and output current
     i_g(k + 1) = D^2 * v_B(k)/(2 * f * L_b) * (v_g/(v_B(k) − abs(v_g)));
     i_o(k + 1) = M_k * v_B(k + 1);
end
```

Figure 5.3 – MATLAB pseudo-code for calculating the output current of the BBLC converter.

5.2 DESIGN EXAMPLE

The design of the BBLC converter with active ripple compensation must be performed in three steps. First, the second stage design must be carried out and the gain $G(f,v_B)$ calculated by the accurate mathematical model of the LC resonant converter. Thereafter, the passive elements of the PFC stage (L_b and C_B) and the parameters of the switching frequency function (f_0, k_f and φ_2) must be obtained. Finally, the control loop is designed so that $f(t)$ assumes the form defined in the previous step.

Table 5.1 shows the design parameters of the converter. The load adopted here as an example to be driven is composed by 48 Luxeon Rebel LEDs connected in series and is described in terms of V_t and r_d, which are also shown in Table 5.1. The criterion for choosing the output current ripple was based on (IEEE, 2015), which showed that an output current ripple of 10% has low risk to cause human biological effects when the driver is supplied by a 60-Hz line voltage.

The duty cycle of this converter is 0.5 in order to obtain a symmetrical switching in the second stage. Moreover, the average bus voltage must be chosen in compliance with the condition given by (5.17) to ensure the DCM operation in the PFC stage. Since the chosen line voltage is 127 V and by replacing this value and D in (5.17), the minimum bus voltage must be 359.2 V to ensure the DCM operation. In this work, V_B = 450 V has been chosen to allow the use of small bus capacitance values.

$$v_B(t) > \frac{\sqrt{2}V_G}{1-D}. \tag{5.17}$$

The normalized switching frequency has been chosen slightly above the resonant frequency aiming high efficiency of the PC stage (LAZAR; MARTINELLI, 2001; WANG et al., 2016a). In other words, this choice allows the converter to operate in the ZVS region despite the large-signal modulation of the switching frequency.

5.2.1 **Design of the PC stage and Gain Calculation**

The design methodology consists in calculating the PC stage's elements through the FHA approach by supposing an approximated value of the switching frequency (f_d) and then, by using the mathematical model presented in (5.5), the accurate behavior of PC gain is calculated. Therefore, the design procedure takes advantage of both the FHA approach, which allows for the straightforward calculation of the resonant tank elements, and the accurate model, which ensures that the converter will operate at the desired conditions.

In the FHA approach, the current through the resonant tank is considered purely sinusoidal. In addition, the rectifier, the output filter and the load are represented by

Table 5.1 – Design Parameters

Symbol	Description	Value
V_G	line voltage	127 V
ω_L	Angular line frequency	$2\pi 60$ rad/s
V_B	Average bus voltage	450 V
Q	Normalized ac-side load resistance	1
ω_n	Normalized switching frequency	1.2
f_d	Design switching frequency	50 kHz
V_t	Nominal threshold voltage of the LED lamp	129.6 V
r_d	Dynamic resistance of the LED lamp	12 Ω
I_o	Average output current	700 mA
V_o	Average output voltage	138 V
P_o	Output power	96.6 W
ΔI_o	Maximum LF LEDs current ripple	70 mA (10%)
η_{PFC}	Estimated efficiency of the PFC stage	97 %
η_{PC}	Estimated efficiency of the PC stage	95 %

an normalized ac-side load resistance given by (5.18).

$$Q = \frac{\pi^2}{8R_o}\sqrt{\frac{L_s}{C_s}}, \tag{5.18}$$

in which $R_o = r_d + V_t/I_o$ is the resistance of the LED lamp, at the point of operation.

According to Ferraz et al. (2018), by rewriting (5.4) and (5.18), the series capacitance and the series inductance can be calculated by (5.19) and (5.20), respectively. Therefore, using the design parameters of the converter listed in Table 5.1 into (5.19) and (5.20), the values of $C_s = 23.9$ nF and $L_s = 610.3$ μH can be found.

$$C_s = \frac{\omega_n \pi I_o}{16 f_d Q (r_d I_o + V_t)}. \tag{5.19}$$

$$L_s = \frac{4 Q \omega_n (r_d I_o + V_t)}{f_d \pi^3 I_o}. \tag{5.20}$$

In order to filter only the switching frequency, the output capacitance can be be sized in accordance to (5.21) as presented in Almeida et al. (2015b). In this work, the output capacitance C_o is defined as 4 μF.

$$\frac{\omega_L}{2\pi} \ll \frac{1}{r_d C_o} \ll f_d. \tag{5.21}$$

Since the PC stage parameters have been obtained, the accurate gain of the LC resonant converter can be calculated. By replacing the PC stage parameters in mathematical model presented in (5.5) and then solving this system for each combination of switching frequency and bus voltage, the behavior of the accurate gain $G(v_B,f)$ can be achieved by (5.8). Figure 5.4 shows the PC stage gain according to variations in the switching frequency and bus voltage. It can be noted that the value of PC stage

accurate gain has a strong dependence on switching frequency and bus voltage. In addition, this figure shows the ZVS region, which is also a constraint for ensuring high efficiency when the converter is operating with the ARC technique.

In this figure, the operating point is also highlighted, which presents the PC stage gain of 1.55 mA/V when the bus voltage is 450 V and the switching frequency is 70 kHz. It can be observed that the dc component of the switching frequency is very different from the chosen design frequency (50 kHz) owing to the use of the FHA technique, which generates the PC stage gain of 4.6mA/V and thus the output current higher than 2 A that would damage the LEDs. However, a feedback loop of this work varies f_0 in order to ensure the desired average output current. In addition, it is worth mentioning that the mathematical model presented in (5.5) is used to obtain the accurate behavior of PC gain for variations in $f(t)$ and $v_B(t)$, which is essential to investigate the BBLC converter with the large-signal modulation of the switching frequency.

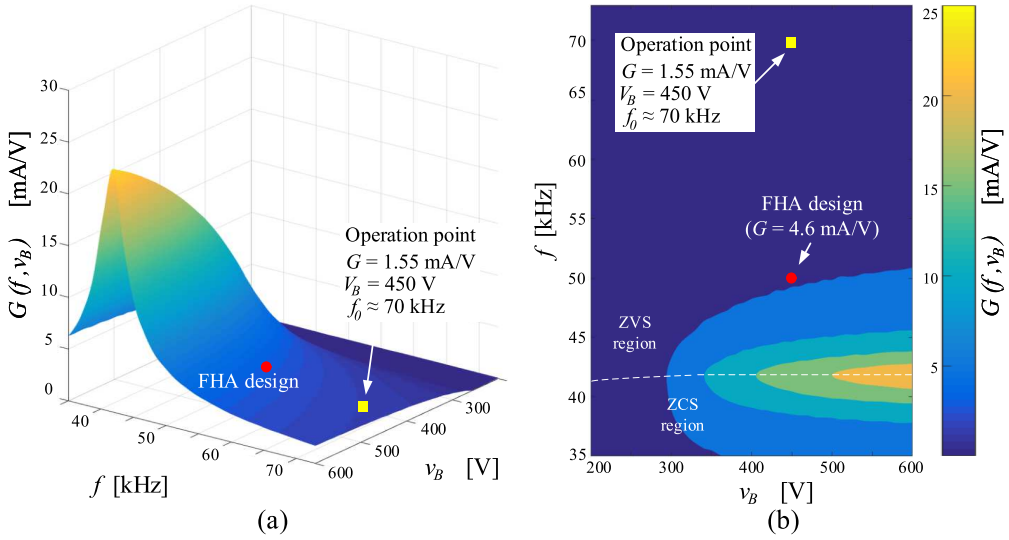


Figure 5.4 – Behavior of the PC stage gain according to variations in the switching frequency and bus voltage, with $L_s = 610.2$ μH and $C_s = 23.9$ nF.

5.2.2 Design of the PFC stage and the Parameters of the Switching Frequency Function

Since the values of switching frequency function (f_0, k_f and φ_2) affect the large-signal low-frequency behavior of the circuit, the PFC stage elements must be designed simultaneously with the definition of the switching frequency function $f(t)$ when the ARCT is employed. This task can be accomplished by adopting a graphical evaluation of the output current behaviors according to variations of the bus capacitance and the parameters of the switching frequency function.

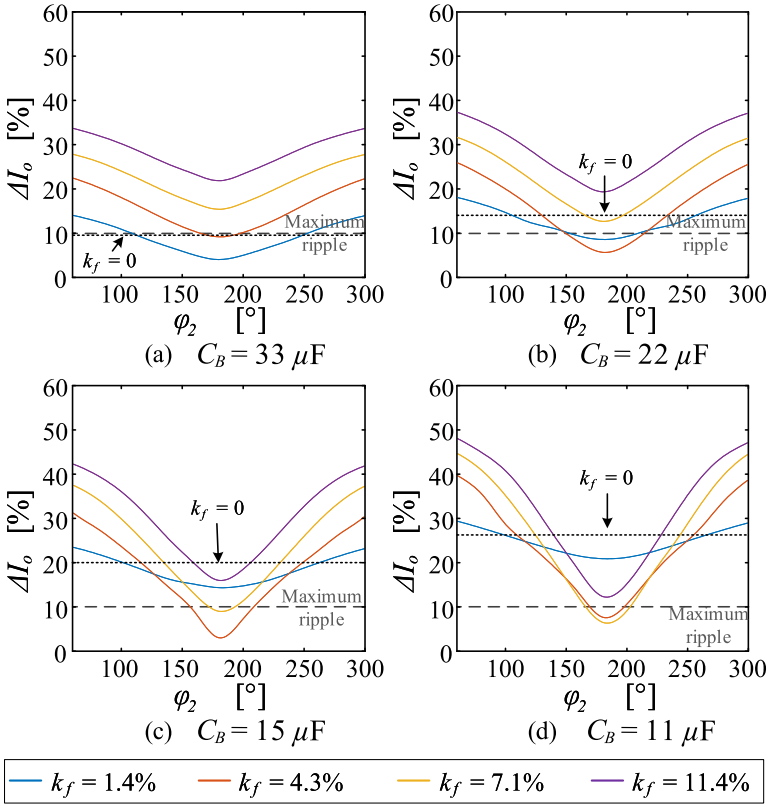


Figure 5.5 – Behavior of the peak-to-peak output current ripple according to k_f and φ_2 for several values of C_B.

Figure 5.5 shows the behavior of the relative output current ripple for some typical values of C_B. For each capacitance, a set of curves was generated and plotted as a function of φ_2 for several values of k_f. The graphs were obtained by solving (5.11), (6.11) and (5.13) using the values of k_f, φ_2 and C_B as well as the parameters presented in Table 5.1. As can be noted in Figure 5.5, if the ARC technique was not used (*i.e.*, $k_f = 0$), the output current ripple reduces with increasing capacitance as expected. However, lower capacitances would be insufficient for meeting the design requirement of maximum ripple, which can be met only by using the large-signal modulation of $f(t)$. The maximum ripple reduction occurs when φ_2 is around 180^o, which occurs when $f(t)$ is in phase with the ac portion of the bus voltage, φ_{vB}. The graphs also show that the output current ripple presents a nonlinear behavior, an increase in the modulation amplitude can either decrease the output current ripple in some cases and increase this ripple in others.

Figure 5.6a shows the behavior of the third harmonic component of the input current (I_3) as a function of the modulation angle φ_2 for different values of the modulation relative amplitude k_f. The graphs were obtained by solving (5.2) using the values of k_f and φ_2 as well as the parameters presented in Table 5.1, by considering $h = 3$. As can be seen, the third harmonic component of the input current remained

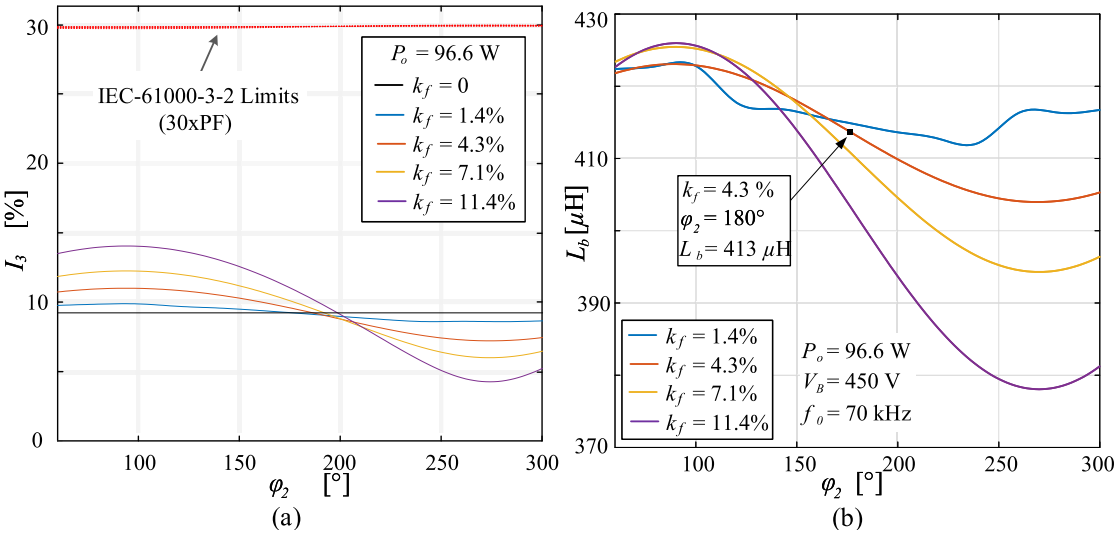


Figure 5.6 – (a) Behavior of the third harmonic component of the input current and (b) variation of the PFC stage inductance according to the switching frequency parameters.

below the limits of the IEC 61000-3-2 standard regardless the values of the switching frequency parameters. The results show that ARC technique interferes little with the input current when the angle φ_2 is close to 180^o. On the other hand, the frequency modulation can be used to reduce the input current crossover distortion of DCM boost PFC when the angle φ_2 is larger than 200^o. It is important to highlight (and experimental evidence confirms this) that the low-frequency modulation of the switching frequency has no significant influence on the values of other harmonic components.

Since the input current of the BBLC converter is also affected by k_f and φ_2, the power processed by the converter is also modified according to the values of such parameters. Therefore, in order to ensure the average power balance of the converter, for each pair (k_f, φ_2) a new value of the boost inductance L_b must be calculated by means of power balance between the input and the output of the converter, as stated in (4.7), so that the power delivered to the load remains constant. Thus, L_b can be obtained by (6.7), which for convenience is exhibited in (5.22). Figure 5.6b shows the relationship of the PFC stage inductance as a function of φ_2 for several values of k_f. It can be seen that when the angle φ_2 is larger than 180^o, the required value of the inductance L_b decreases as the amplitude of the ac portion of $f(t)$ increases.

$$L_b = \frac{\eta D^2 V_B}{T_L P_o} \int_0^{T_L} \frac{v_g(t)^2}{f(t)(V_B - |v_g(t)|)} \mathrm{d}t, \tag{5.22}$$

in which $\eta = \eta_{PFC}\eta_{PC}$ is the global efficiency.

Since the large-signal low-frequency behavior of the BBLC was investigated, the values of the switching frequency function $f(t)$ and the bus capacitance C_B can be

defined. Therefore, by choosing $k_f = 4.3\%$ and $\varphi_2 = 180^o$, the desired ripple criterion is achieved for a bus capacitance of $C_B = 11$ μF, which yields an output current ripple of 7,76 % (54.36 mA peak-to-peak). For the chosen operating point, the value of the inductance L_{bo} must be 413 μH.

It is important to highlight that, if the ARC technique was not used (*i.e.,* k_f=0), a capacitance of ca. 33 μF should be used for achieving a similar ripple level. Therefore, the modulation of the switching frequency provided a capacitance reduction of 22 μF (66.6 %) when compared to the conventional approach without modulation. In addition, for the chosen operating point, the total harmonic distortion was increased by only 0.6%, yielding a theoretical THD of 9.7% in accordance with the Figure 4.3b.

5.2.3 **Design of the Control Loop**

Since the passive elements and the switching frequency function have been defined, the control circuit can be designed. The transfer function of C_{av} is shown in (6.31). As it can be noted, this compensator is an integrator, which ensures that the system will have null steady-state error under constant current reference. Furthermore, the crossover frequency (f_{co}) of this transfer function must be tuned so that the output of the C_{av} block does not present any a.c. component in steady-state, *i.e.*, C_{av} must attenuate all the oscillating components of the error signal. It is important to highlight that the low crossover frequency allows for appropriate performance of the LED driver even when the LLC converter with higher sensitivity, such as $\lambda = 0.6$, is used. In addition, the negative signal is used here since, in the case of resonant converters, the circuit gain reduces as long as the amplitude of the control variable, which is the switching frequency, increases.

$$C_{av}(s) = -\frac{K_a}{s}. \tag{5.23}$$

In order to ensure a good attenuation at 120 Hz, a crossover frequency of ca. 1.3 Hz was chosen, which is two decade below $2\omega_L$, resulting in a $K_a = 8.17$ Hz.

The expression for C_{bp} was obtained based on a narrow-band second-order band-pass filter, as shown in Soares, Alonso e Braga (2018). This element was tuned with a center angular frequency of $2\omega_L$, which ensures that the oscillating component of the $f(t)$ presents the desired frequency. In addition, the desired phase of the modulation signal is also ensured ($\varphi_2 = 180^o$), since the filter phase at the tuned angular frequency is null. Therefore, the transfer function of C_{bp} is given by (6.32), in which $V_{B\_2\omega_L}$ is the amplitude of the $2\omega_L$ component of the bus voltage and B is the filter bandwidth.

$$C_{bp}(s) = \left(\frac{k_f f_0}{V_{B\_2\omega_L}}\right) \frac{Bs}{s^2 + Bs + 4\omega_L^2}. \tag{5.24}$$

By using the design results obtained in Section 5.2.2 in (6.12) and (6.11), by replacing these equations in (5.11) and solving numerically, the bus voltage is obtained. Thereafter, performing the Fourier series in the $v_B(t)$, for a bus capacitance of $C_B = 11\ \mu$F, the amplitude of the $2\omega_L$ component is found to be 29.54 V. Finally, the filter bandwidth was chosen as 20 rad/s in order to obtain a good attenuation of the undesired frequencies.

It is important to highlight that owing to the simplicity of the control structure used in the ARC approach (see Figure 5.1), its implementation could be performed by using a simple microcontroller or even by means of analog filters and control circuitry. In order to enable an easier tuning of parameters for the lab prototype, the control system of this work was implemented digitally.

The discretization of the elements of the control loop, which was implemented in a TIVA C-Series microcontroller, was performed using the bilinear transformation. The difference equations that represents the compensator $C_{av}(s)$, the band-pass filter $C_{bp}(s)$ and the switching frequency of the discrete-time system are given by (5.25), (5.26) and (5.27), respectively.

$$y_a(k) = y_a(k-1) + N_a(e(k) + e(k-1)), \tag{5.25}$$

$$y_b(k) = N_{b1}v_{bk}(k) + N_{b2}v_{bk}(k-2) - N_{b3}y_b(k-1) - N_{b4}y_b(k-2), \tag{5.26}$$

$$f_k(k) = f_0 + y_a(k) + y_b(k), \tag{5.27}$$

where y_a, e, y_b and f_k are the discrete variables representing the output of the average current compensator, the error signal, the band-pass filter and the switching frequency, respectively. The integer k is the index of the k^{th} sample of the discrete system. The definition and values for each coefficient in (5.25) and (5.26) are gathered in Table 5.2, in which a sampling frequency f_{sam} of 10 kHz was considered.

Table 5.2 – Coefficients used in the discrete implementation

Coefficient	Definition	Value
N_a	$\frac{K_a}{2f_{sam}}$	-28.6 Hz/A
N_{b1}	$\left(\frac{k_f f_0}{V_{B\_2\omega_L}}\right) \frac{Bf_{sam}}{2{f_{sam}}^2 + Bf_{sam} + 2\omega_L^2}$	0.10131 Hz/V
N_{b2}	$-\left(\frac{k_f f_0}{V_{B\_2\omega_L}}\right) \frac{Bf_{sam}}{2{f_{sam}}^2 + Bf_{sam} + 2\omega_L^2}$	-0.10131 Hz/V
N_{b3}	$\frac{4\omega_L^2 - 4{f_{sam}}^2}{2{f_{sam}}^2 + Bf_{sam} + 2\omega_L^2}$	-1.99233
N_{b4}	$\frac{2\omega_L^2 + 2{f_{sam}}^2 - Bf_{sam}}{2{f_{sam}}^2 + Bf_{sam} + 2\omega_L^2}$	0.998

5.3 EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a laboratory prototype was built, which is shown in Figure 5.7. Table 5.3 presents the main elements used in the prototype.

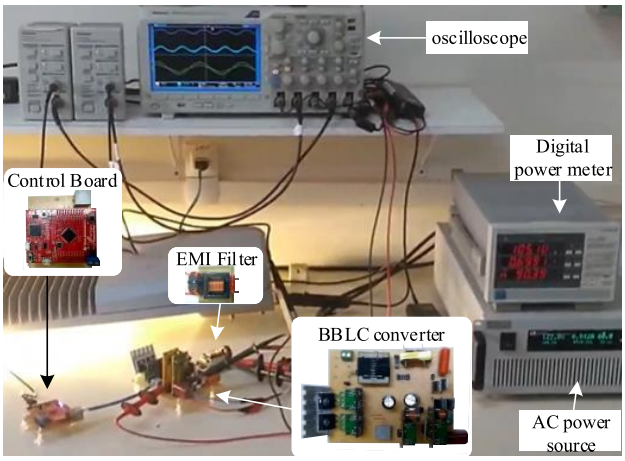


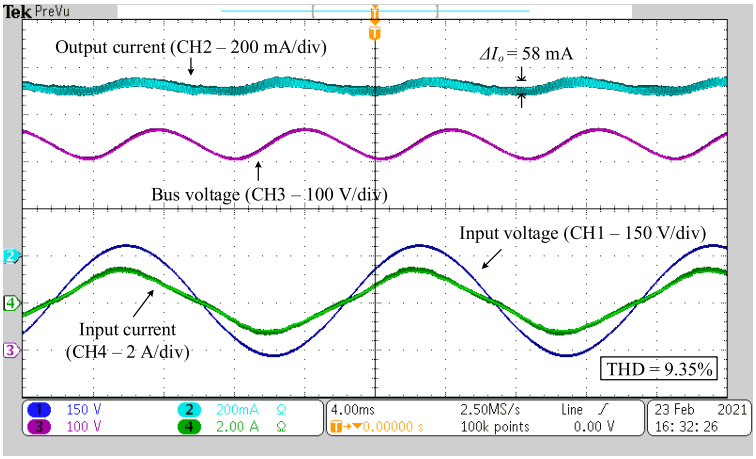
Figure 5.7 – Photograph of the experimental setup, showing each part of the prototype and the corresponding boards and components.

Table 5.3 – Main Parameters of Prototypes

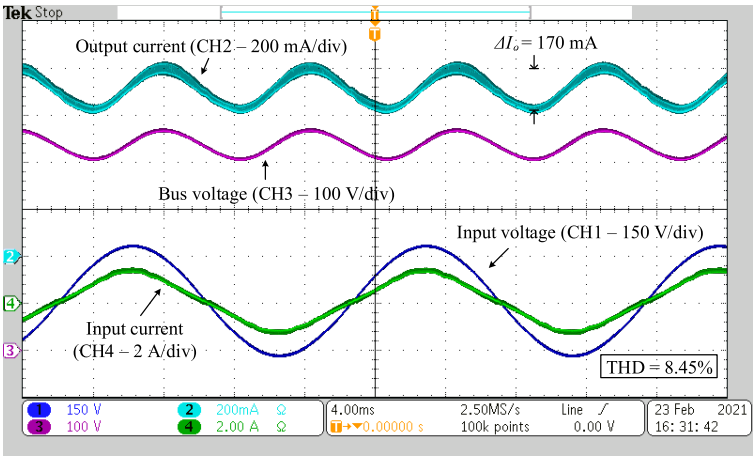
Item	Value
Half-bridge switches	2 x IRFP460 (500V / 0.25Ω)
Boost diodes (bottom)	2 x MUR360S / (600V / 3A)
Boost inductor L_b	413 μH / NEE 30-15-14 / 53 turns gap = 0.48 mm / 4x28 AWG
Bus capacitors	22 μF / 400V Electrolytic capacitor (Chong CD11X) equivalent C_B = 11 μF
Resonant inductor L_s	610.2 μH / NEE 30-15-7 / 53 turns gap = 0.16 mm / 3x28 AWG
Resonant capacitor C_s	22 nF / 630V polypropylene capacitor (B32692A6223)
Output diode bridge	4 x IDT02S60C (600V / 2A)
Output capacitor C_o	4.7 μF/ 250V polyester film capacitor (ECQE2475)
EMI Filter	CM:5 mH / DM: 470μH / 220nF
Microcontroller	Texas Instruments TM4C123G
Current and voltage sensors[1]	based on AMC-1200
Isolated gate drivers[1]	based on HCPL-3120

Figure 5.8 presents some experimental waveforms from the off-line LED driver based on the LC resonant converter employing the frequency-based ARC technique with C_B = 11 μF / 480V (Figure 5.8a) compared with the same circuit without the large-signal modulation of the switching frequency (Figure 5.8b), and also with the conventional approach (no active compensation) with a bus capacitance of 33 μF / 460V (Figure 5.8c). The low-frequency output current ripple obtained from this experiment

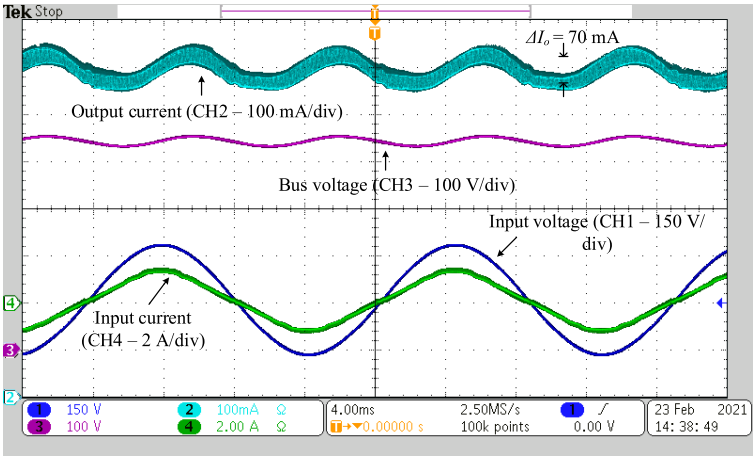
[1] For more details, see Albuquerque et al. (2017).



(a) $C_B = 11$ µF with ARC



(b) $C_B = 11$ µF without ARC



(c) $C_B = 33$ µF without ARC

Figure 5.8 – Experimental waveforms obtained (a) with ARC and $C_B = 11$ μF; (b) without ARC and $C_B = 11$ μF; (c) without ARC and $C_B = 33$ μF.

was 58 mA, which is quite close to the 54 mA from theoretical prediction. In addition, Figure 5.8b depics a larger ripple when the ARC technique is not used with the same bus capacitance of 11 μF, being necessary an additional value of 22 μF (Figure 5.8c) to decrease the output current ripple to a similar level to the one obtained when the

ARC technique is employed. The experimental results of the LED driver without ARC were obtained by using only the pure integrator shown in (6.31), which ensures that the system will have null steady-state error under constant current reference.

It is important to highlight that, as shown in Figure 5.8, the output current ripple of the circuit with low-frequency large-signal modulation of the switching frequency is lower than the conventional approach (i.e, without ARC) imposing little increase of the input current distortion. As it can be seen, experimental results showed that ARC technique increased only 0.9% the total harmonic distortion of the input current, when compared with the conventional approach. In addition, this distortion was predicted during the design procedure so that the harmonic content of the input current remains in compliance with the IEC-61000-3-2 standard, as presented in Figure 5.9. The other harmonics were not depicted in Figure 5.9 because their values were negligible. As can be noted, the experimental results of the input current are also close to the values obtained in the theoretical analysis. The measured THD was 9.35%, which is very close to the 9.4% predicted by the analysis. The measured PF of the BBLC with ARC technique was 0.986.

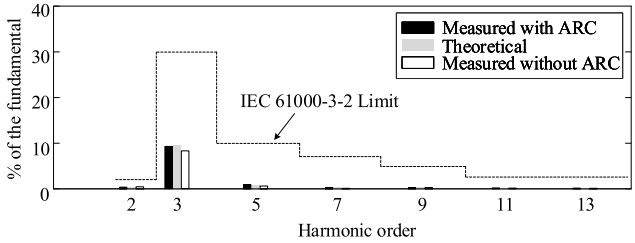


Figure 5.9 – Harmonic content of the input current compared with IEC limits

Figure 5.10 presents experimental waveforms of the current and voltage of the MOSFET M_1 and the output rectifier diode at the positive (Figure 5.10a) and negative (Figure 5.10b) peak of line voltage. These waveforms show that the converter operates above series resonant frequency and with ZVS. Table 5.4 shows the measured loss distribution in the prototype by using a Yokogawa WT230 digital power meter. The measured loss was obtained at nominal input voltage and rated load. Furthermore, those measurements did not take into account the consumption of the control board.

Figure 5.11 shows the currents through boost inductor L_b measured at the peak of the line voltage. It can be noticed that the waveform is discontinuous, which means the BBLC is indeed operating under DCM for the whole line half-cycle. Figure 5.12 presents the dynamic performance of the converter during a step of -10% in reference signal. The control system was able to ensure null steady-state error, while keeping a low-frequency large-signal modulation of the switching frequency (ARC branch), which are the very means by which ARC reduces the output current ripple.

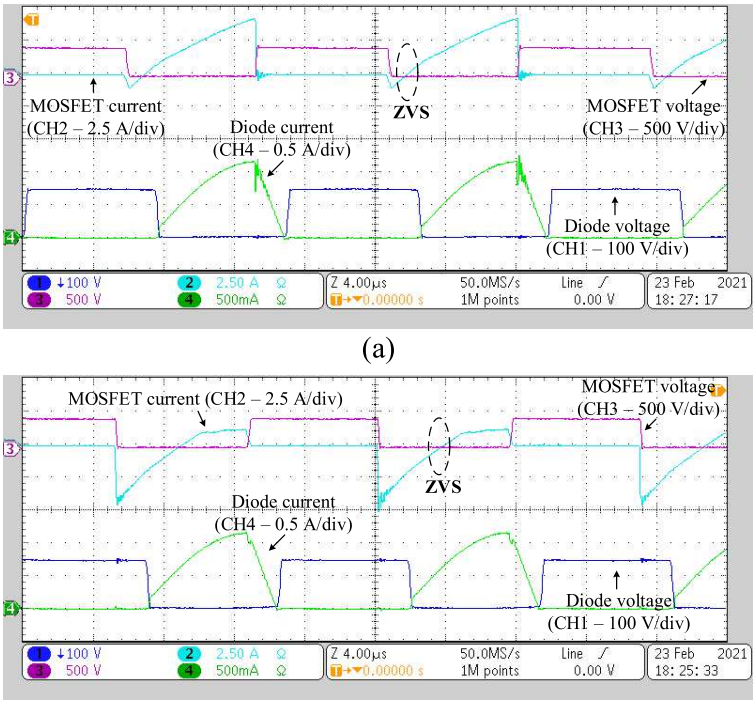


Figure 5.10 – Waveforms measured at the (a) positive and (b) negative peak of line voltage. Diode voltage (CH1 - 100V/div), MOSFET M1 current (CH2 - 2.5A/div), MOSFET voltage (CH3 - 500V/div) and diode current (CH4 - 500mA/div). Horiz. scale: 4 μs/div.

Table 5.4 – Measured Loss Distribution.

Components	Values
EMI filter	0.32 W
MOSFETs	1.7 W
Boost diodes	2 W
L_{bo}	1.3 W
C_B	0.46 W
C_s	0.8 W
L_s	1.6 W
Output diode bridge	1.8 W
C_o	0.2 W
Total	10.18 W

Figure 5.13 presents the output current ripple, THD, and efficiency of the converter according to variations in the input voltage. The results show that the output ripple (Figure 5.13a) of the driver with frequency-based ARC technique was much smaller over the entire range, with a small increment of THD (Figure 5.13b). It is important to highlight that the influence of the frequency modulation upon the efficiency (Figure 5.13c) is negligible for variations in the input voltage.

The behavior of the output current ripple, THD and efficiency owing to variations in the output power is presented in Figure 5.14. The results showed that the

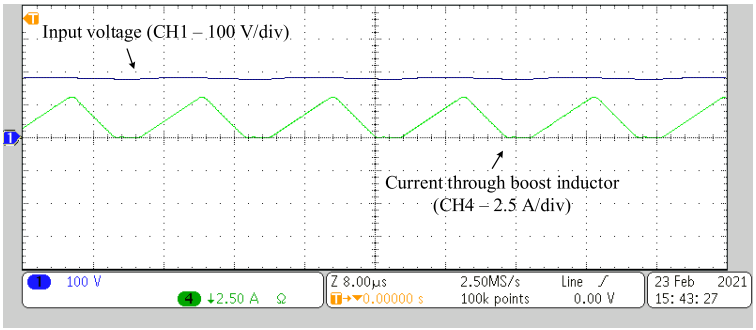


Figure 5.11 – Waveform of the current through boost inductor measured at the peak of the line voltage.

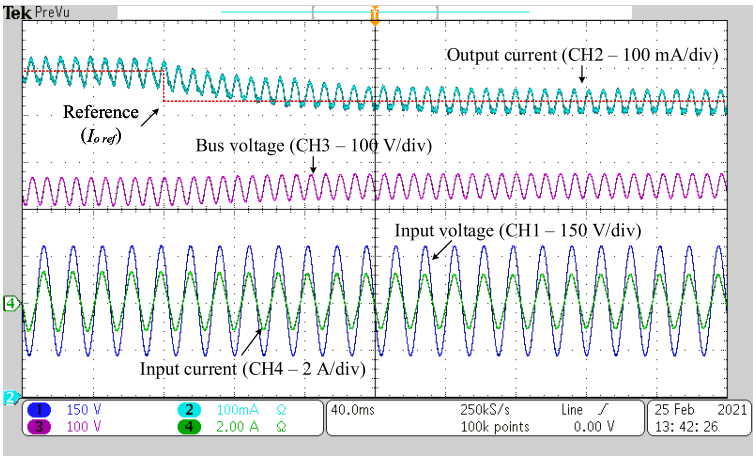


Figure 5.12 – Experimental waveforms of the BBLC following a reference command signal. Input voltage (CH1 - 150V/div), output current(CH2 - 100 mA/div), bus voltage (CH3 - 100V/div) and input current (CH4 - 2A/div). Horiz. scale: 40 ms/div.

converter with frequency modulation ensured a small current ripple for all the analyzed levels. In addition, the influence of the frequency-based ARC upon the THD and efficiency can be considered negligible for variations in the output power.

Table 5.5 shows a brief comparison among the proposed frequency-based ARC and other control techniques devised to reduce bulk capacitance in off-line LED drivers, highlighting deviation of THD and capacitance reduction. Overall efficiency, power, total harmonic distortion, and other performance parameters were also analyzed for each topology whose techniques were applied. Unlike other techniques presented in the literature, the proposed frequency-based ARC can be applied to converters with resonant stages, which allows for the design of high-efficiency low-capacitance LED drivers. A good performance in terms of efficiency was also achieved in (WONG et al., 2016) (indicated in the table by [ref.3]), since the converter presented in this paper is composed of only one stage. However, the approaches of [ref.4] (LAMAR et al., 2012) and [ref.3] yielded a moderate capacitance reduction with a high increase in the input current distortion. In the integrated off-line LED driver based on hard-switching

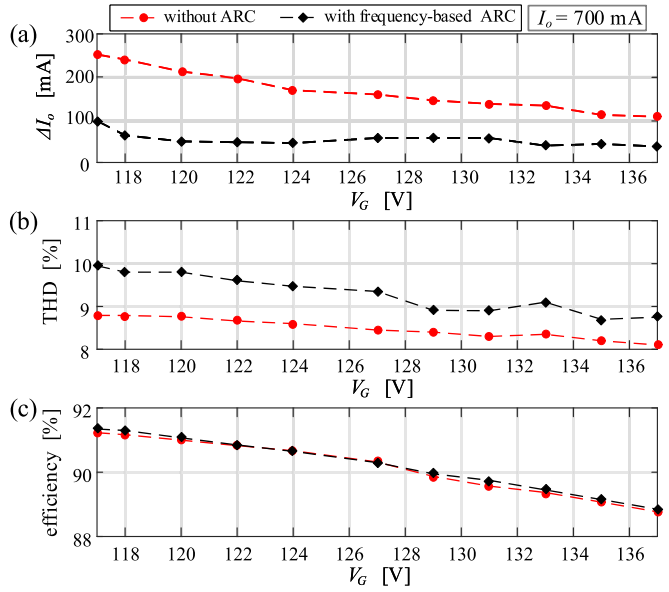


Figure 5.13 – Output ripple, THD and efficiency of the converter according to variations in the input voltage.

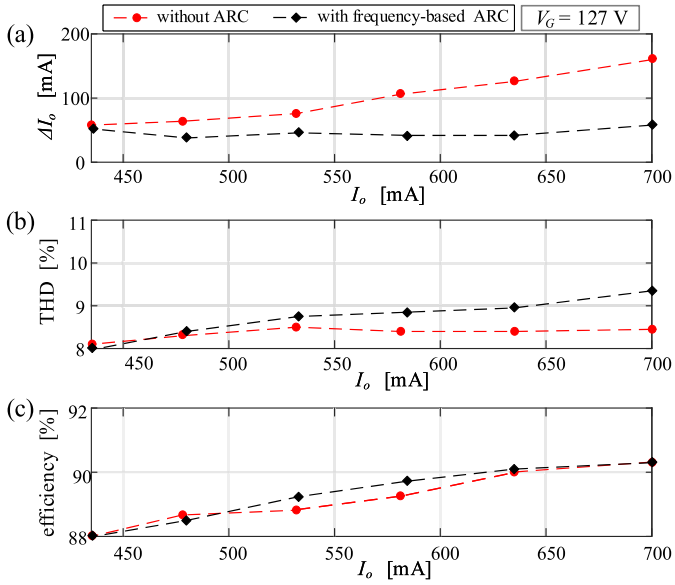


Figure 5.14 – Output ripple, THD and efficiency of the converter according to variations in the output power.

topologies proposed in [ref.1] (SOARES et al., 2018) and [ref.2] (LUZ et al., 2018), the obtained capacitance reduction was improved, mainly in [ref.1], but still resulting in a high input current distortion. Moreover, the overall efficiency of these converters is low. It is important to highlight that the proposed frequency-based ARC allows for a large capacitance reduction without affecting the THD significantly. Therefore, the proposed approach is a great alternative concerning reduction of bulk capacitance, improving the driver lifetime while still maintaining a low output ripple and preventing flickering.

Table 5.5 – Comparison among control techniques to reduce bulk capacitance in off-line LED drivers.

	Proposed frequency-based ARC	duty-cycle-based ARC [ref.1]	Proportional Integral Resonant controller [ref.2]	3rd harmonic injection [ref.3]	Distorted sinusoidal reference [ref.4]
Topology	BBLC	double buck-boost	double buck-boost	PFC boost	PFC boost
ΔTHD	0.9 %	17.2 %	10.2 %	>40 %	>25 %
Capacitance reduction	66.6 %	85 %	80.5 %	33 %	23 %
			Performance Parameters of the Topology		
Efficiency	90.3 %	84 %	-	91 %	-
Output power	96.6 W	75 W	71.5 W	20 W	500 W
Output current ripple	58 mA (8.3 %)	50 mA (10 %)	56 mA (8 %)	14 mA (29.7 %)	- -
PFC stage output capacitance	11 μF	22 μF	20 μF	8.8 μF	500 μF
PFC stage output voltage	450 V	160 V	200 V	420 V	400 V
FP	0.986	0.982	0.987	0.91	0.967
THD	9.35 %	18.2 %	19 %	-	-
Galvanic isolation	No	No	No	No	No
Dimming	Low[1]	Yes	No	No	No
Universal-input voltage	No	No	No	No	Yes

[ref.1]: (SOARES et al., 2018).

[ref.2]: (LUZ et al., 2018).

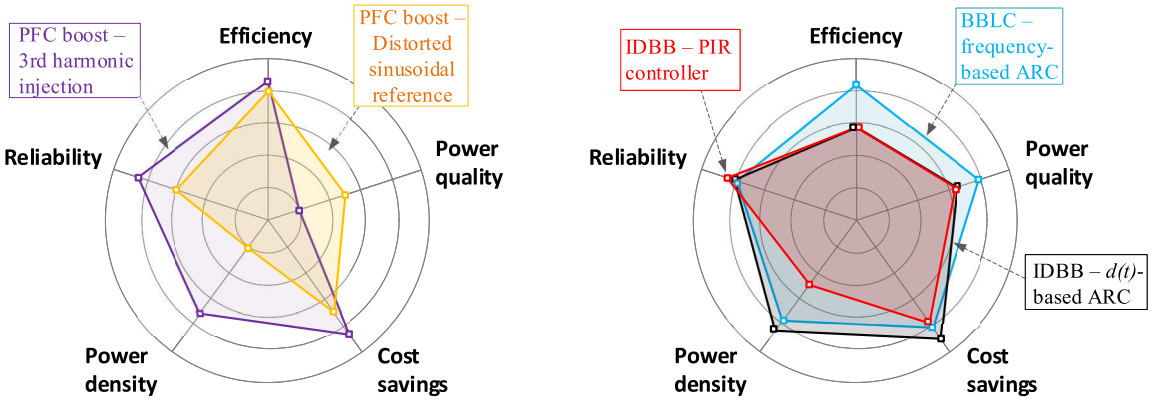
[ref.3]: (WONG et al., 2016).

[ref.4]: (LAMAR et al., 2012).

- Value not reported in the paper.

[1] The converter works properly with a 35% reduction in output power.

Based on the experimental results obtained by the works shown in Table 5.5, the performance analysis tool was used to compare the LED drivers. Among these converters, PFC boost with 3rd harmonic injection has the lowest capacitance value which implied very high reliability, but the significant harmonic injection distorted the input current considerably, thus resulting in worse ac input power quality. IDBB converter with PIR controller also achieved very high reliability, mainly by using film capacitor. However, this technology yielded a reasonable power density. When compared to the IDBB converter with duty-cycle-based ARC technique, the BBLC converter with frequency-based ARC approach also performed well regarding reliability, power density, and cost savings, but with a significant improvement in power quality and efficiency.



(a) single-stage LED drivers (b) two-stage LED drivers

Figure 5.15 – Performance analysis of off-line LED drivers with control techniques to reduce bulk capacitance.

One of the drawbacks of the BBLC topology is that the PFC stage operates with a duty cycle of 0.5 and, therefore, the bus voltage has to be at least twice the peak value of the input voltage. Hence, it poses some difficult to operate in universal-input voltage condition with the 650 V/700 V voltage rating power devices. However, this disadvantage can be solved by using one of the buck-boost type topologies instead of boost-based topologies. Regarding the PC stage, the series resonant converter adds no galvanic isolation and has a relatively low efficiency. These drawbacks can be mitigated by employing the LLC converter and performing the design procedure proposed in this work.

5.4 SUMMARY OF THE CHAPTER

This chapter discussed the investigation of the frequency-based ARC technique applied to an off-line LED driver based on the LC resonant converter, which is the lowest sensitivity of the LF ripple to frequency modulation among the LLC conver-

ters evaluated in chapter 4. The converter is composed by integrating a totem-pole bridgeless boost PFC and a half-bridge LC series resonant converter.

An application example was also detailed, highlighting the sizing of the passive elements based on design abacuses and the calculation of the control system. The experiments shown that the circuit presents a good performance in terms of current regulation. In addition, a PF higher than 0.98, a THD lower than 10% and a global efficiency of 90.3% in full load condition were achieved.

Experimental results verified the theoretical analysis and feasibility of the LED driver, showing that the frequency-based ARC technique allowed for a capacitance reduction of 66.6%, while increasing only in 0.9% the input current THD. Therefore, frequency-based ARC is greatly leveraged in resonant converters which have high sensitivity to frequency variations even for the case of LC resonant converter (λ=0), which is considered the worst case of load-resonant converters.

6 MULTI-OBJECTIVE OPTIMIZATION-BASED DESIGN OF A HIGH-PERFORMANCE LED DRIVER

The previous Chapter detailed a case study of a converter employing the frequency-based ARC, which allows for a large capacitance reduction without affecting the THD significantly when applied to converters with a load-resonant PC stage. However, the approach for designing the passive elements was based on abacuses, which start from arbitrary initial considerations.

As previously discussed, performance parameters such as power losses, volume, failure rate, and system costs are interconnected, creating a trade-off relationship. Due to the multi faceted nature of LED driver design, some design conditions are arbitrarily chosen in most works, relying on the expertise of the designer. Although it is possible to achieve good results, this type of design procedure is not systematic. In this context, this Chapter presents a multi-objective optimization strategy for designing a high-performance off-line LED driver, aiming to improve several mutually coupled performance parameters, while ensuring the compliance with some constraints, such as the ones defined in the IEC 61000-3-2:2018 standard.

6.1 DESIGN OF LED DRIVERS BASED ON A CONSTRAINED OPTIMIZATION PROBLEM

A design of a high-performance LED driver must deal with several key objectives, including:

- Minimization of the losses and thus maximization of the efficiency;
- Minimization of the volume and thus maximization of the power density;
- Minimization of the failure rate and thus maximization of the reliability;
- Minimization of the costs;
- Minimization of the total harmonic distortion of the input current;

Therefore, the design of the converter can be modeled as an optimization problem, defined in terms of an objective function (to be minimized) while satisfying constraints into a search space, as shown in (6.1). This weighted sum method assigns weights for each objective (performance function) based on the relative preferences among objectives, and combines the multiple objectives into a single objective.

$$\begin{aligned} &\min f_{obj}(\boldsymbol{x}) = \sum_{i=1}^{4} w_i c_i(\boldsymbol{x}) \\ &\text{s.t. } A(\boldsymbol{x}) \leq 0_{[8,1]} \\ &\boldsymbol{x_{lb}} \leq \boldsymbol{x} \leq \boldsymbol{x_{ub}}, \end{aligned} \tag{6.1}$$

in which $\boldsymbol{x}$ is the vector of the design variables to be optimized. In addition, w_i represents the weight for the ith single-objective cost function c_i. Different weightings of the individual cost function lead to a multitude of solutions in the search space. These solutions represent a possible compromise between competing performances. The single-objective cost functions c_1, c_2, c_3 and c_4 correspond to the volume, the total losses, the estimated failure rate and the total cost of the converter, respectively.

On the other hand, the distortion of the input current can be modeled as part of the constraints $A(\boldsymbol{x})$. The constraint functions are a set of expressions devised in order to ensure the design requirements. This vector can take into account the FP and the limits established by the IEC-61000-3-2 standard, as well as the low-frequency ripple in the LEDs.

It's important to highlight that (6.1) will be computed for a specific topology according to the system specifications and operating requirements. Therefore, the cost functions will be calculated according to the equations of the topology under analysis, considering available components/materials in the laboratory.

A constrained multi-objective minimization problem was formulated for designing the LED driver. This model requires the choice of a set of specifications (design parameters), the circuit topology, and the optimizations variables. In addition, the optimization algorithm must also be chosen in order to solve (6.1), also considering the materials available. Figure 6.1 depicts the step-by-step solution of (6.1) in each iteration of the optimization algorithm. Initially, the design of the power circuit components (such as inductors/transformers and capacitors) and the control parameters are carried out. Then, these parameters are employed in the accurate converter model to solve the main converter equations, such as input current, bus voltage, and output current. At the end of the iteration, the aforementioned variables are used to compute the individual cost functions, which are combined through the weights to calculate the $f_{obj}(\boldsymbol{x})$. Finally, the optimized converter can be prototyped and tested to validate its performance.

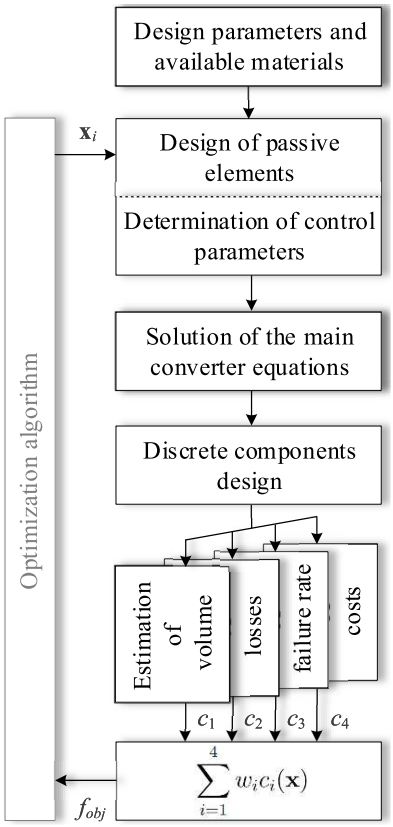


Figure 6.1 – Flowchart for computing $f_{obj}(\boldsymbol{x})$ at each iteration of the optimization algorithm.

6.2 CASE STUDY OF AN OFF-LINE LED DRIVER WITH ARC TECHNIQUE IN THE SWITCHING FREQUENCY

The topology chosen in this design example was obtained by integrating a totem-pole bridgeless boost PFC and a half-bridge LLC resonant converter, as illustrated in Figure 6.2. This converter was evaluated in the Chapter 4, yielding promising results, making it an suitable choice for designing a high-performance LED driver. When compared to the converter addressed in Chapter 5, this topology needs a lower modulation amplitude for capacitance reduction, thus resulting in lower input current distortion. Additionally, this converter typically exhibits higher efficiency and incorporates galvanic isolation, which is a desirable feature for high-performance LED drivers.

Table 6.1 summarizes the main equations of the LED driver operating in DCM and ZVS. These expressions allow for the design of the passive elements and solution of the large-signal low-frequency model of the converter. It is important to highlight that some equations presented in Table 6.1 must be solved numerically, such as the equation of the bus voltage. In addition, some equations depend on the PC transconductance gain $G(v_B,f)$, which can be achieved by replacing $f(t)$ and $v_B(t)$ in the accurate model of LLC resonant converter presented in Chapter 3, and solving this model by using a numerical integration. According to Chapter 4, the modulation of the switching-

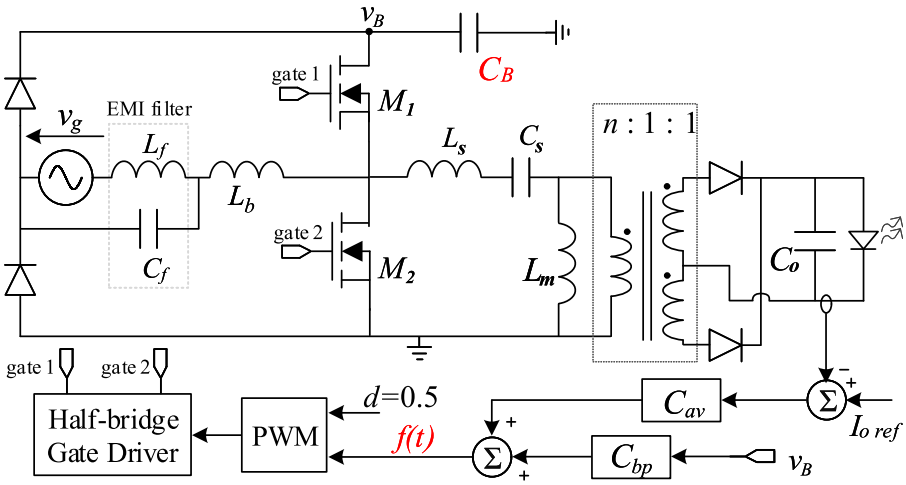


Figure 6.2 – Integrated Off-line LED driver based on the LLC resonant converter with frequency-based ARC technique.

frequency can reduce the current ripple. Therefore, this work considers this possibility and the switching frequency function is defined by (6.8) as presented in Chapter 5, *i.e.*, in terms of its average value f_0, and relative amplitude k_f. In order to simplify the design procedure, the elements of the EMI filter were not taken into account for calculating the single-cost functions.

In addition to the system specifications and operating requirements, the equations shown in the Table 6.1 are dependent on optimization variables. For this topology, the parameters commonly chosen based on the expertise of the designer are the bus capacitance C_B, the normalized ac-side load resistance Q, the inductance ratio λ, and the normalized switching frequency f_n. In order to reduce the dependence on arbitrary designer choices, these parameters constitute the vector containing the optimization variables, as shown in (6.15).

$$\boldsymbol{x} = \begin{bmatrix} C_B & Q & \lambda & f_n \end{bmatrix}. \tag{6.15}$$

Table 6.2 shows the design parameters of the example converter, representing the system specifications and operating requirements.

6.2.1 Materials Selection

This subsection presents the materials available for consideration in the optimization problem. This selection is based on the materials available in the laboratory that are suitable for the application addressed in this work. For the sake of simplicity, the same semiconductor elements were used regardless the optimization results. The IRFP460 MOSFET was selected for the half-bridge switches owing to its low on-resistance. The MURS360 and MUR820 have an ultrafast reverse recovery time and

Table 6.1 – Main equations of the converter, operating in DCM and ZVS.

Variable	Equation	
Inductance L_s	$$L_s = \frac{4Qn^2}{f_r\pi^3\left(r_d + \frac{V_t}{I_o}\right)}$$	(6.2)
Capacitance C_s	$$C_s = \frac{\pi\left(r_d + \frac{V_t}{I_o}\right)}{16Qf_rn^2}$$	(6.3)
Magnetizing inductance L_m	$$L_m = \frac{L_s}{\lambda}$$	(6.4)
Turns ratio n	$$n = \frac{V_B}{2Vo\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}}$$	(6.5)
Output capacitance	$$C_o = \frac{1}{2\omega_s r_d}\sqrt{\left(\frac{4I_o}{3\Delta I_{oHF}}\right)^2 - 1}$$	(6.6)
Inductance L_b	$$L_b = \frac{\eta d^2}{T_L P_o}\int_0^{T_L} \frac{V_B v_g(t)^2}{f(t)(V_B - \lvert v_g(t)\rvert)}\mathrm{d}t$$	(6.7)
Switching frequency function	$$f(t) = f_0[1 + k_f \sin(2\omega_L t + 180^o)]$$	(6.8)
Input voltage	$$v_g(t) = \sqrt{2}V_G \sin(\omega_L t)$$	(6.9)
Low-frequency input current	$$i_g(t) = \frac{d^2}{2f(t)L_b}\left(\frac{v_g(t)v_B(t)}{v_B(t) - \lvert v_g(t)\rvert}\right)$$	(6.10)
output current of the PFC stage	$$i_D(t) = \frac{\eta_{PFC} v_g(t)^2 D^2}{2L_b f(t)(v_B(t) - v_g(t))}$$	(6.11)
input current of the PC stage	$$i_B(t) = v_B(t)\frac{G(v_B,f)^2 r_d}{\eta_{PC}} + \frac{G(v_B,f)V_t}{\eta_{PC}}$$	(6.12)
Bus voltage	$$v_B(t) = \frac{1}{C_B}\int (i_{PFC}(t) - i_B(t))\,\mathrm{d}t$$	(6.13)
Output current	$$i_o(t) = v_B(t)G(v_B,f)$$	(6.14)

Table 6.2 – Design Parameters.

Symbol	Description	Value
V_G	line voltage	127 V
ω_L	Angular line frequency	$2\pi 60$ rad/s
V_B	Average bus voltage	450 V
v_{Bmax}	Maximum bus voltage	500 V
V_t	Nominal threshold voltage of the LED lamp	129.6 V
r_d	Dynamic resistance of the LED lamp	12 Ω
I_o	Average output current	700 mA
V_o	Average output voltage	138 V
P_o	Output power	96.6 W
η_{PC}	Estimated efficiency of the PC stage	97 %
η_{PFC}	Estimated efficiency of the PFC stage	95 %
ΔI_{oHF}	Maximum high-frequency LEDs current ripple	20mA
ΔI_{omax}	Maximum LF LEDs current ripple	70 mA (10%)
f_r	Series resonant frequency	100 kHz

were employed in the boost diodes (PFC stage) and output rectifier diodes, respectively. Some critical parameters of these semiconductor components must be extracted from their datasheets in order to estimate the power losses. The IRFP460 has a rise time of t_r=59 ns and a fall time of t_f=58 ns, with an on-resistance of R_{on}=0.27 Ω. The on-resistance of MURS360 and of MUR820 are R_D=0.1 Ω and R_{Drec}=0.12 Ω, respectively. Furthermore, the MURS360 has a maximum instantaneous forward voltage of V_D = 1.05 V, while that of the MUR820 is V_{Dred}=0.975 V.

Regarding the possible values for the bus capacitance, it was chosen the family of 500-V aluminum electrolytic capacitors from Nichicon UCY and LGN series, considering the capacitance tolerance of tol_B=20% at 120 Hz and the dissipation factor of DF_{CB}=0.2. Selecting both series provides a wide range of capacitance values for design. This search space for capacitors is shown in Table 6.3, in which the first row represents the possible values for the bus capacitance and the second is the boxed volume of each device. The boxed volume was calculated from the dimensions obtained from the datasheet. For the resonant series capacitor, the TDK B32692 series of metallized polypropylene capacitors was chosen. On the other hand, the output capacitor was selected from the Panasonic ECQE(F) series of metallized polyester film capacitors. These capacitor families are good alternatives for the prototype implementation, and were selected also considering the laboratory availability.

Materials available also needs to be defined for the inductors and transformer of the LLC converter. The magnetic components design involves the core material, shape, size selection, and winding wire selection. The area product method is employed in order to define the core size. In the design of these discrete components, the EE

Table 6.3 – Possible values for the capacitances.

Variable	Possible values of capacitance and volume																		
	UCY and LGN series - tol=20% and DF=0.24																		
C_B [μF]	10	15	18	22	27	33	39	47	56	68	82	100	120	150	180	220	270	330	390
Vol_{CB} [cm^3]	3.12	3.91	4.92	6.4	6.25	8.06	9.09	10.24	12.1	15.62	16.94	22.5	27	30.62	36.75	42.87	49	55.12	61.25
	B32692 series - DF=0.001																		
C_s [nF]	1	1.5	2.2	3.3	4.7	6.8	10	15	22	33	47								
Vol_{Cs} [cm^3]	1.42	1.42	1.482	1.662	1.662	1.995	2.65	3.762	4.22	6.03	8								
	ECQE(F) series - DF=0.001																		
C_o [μF]	1	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2	10						
Vol_{Co} [cm^3]	2.05	2.35	2.79	3.02	3.6	4.15	4.82	5.86	6.71	7.68	9.02	10.41	12.72						

shaped magnetic core was employed, considering IP12R ferrite cores from Thornton (THORNTON, 2015), as described in Table 6.4. It's worth noting that the coil former was also taken into account, including aspects such as the mean lap turn length (MLT) and the boxed volume V_{box}.

Table 6.5 shows the parameters of the AWG round copper wire. For each AWG, this table presents the cross-sectional area of the copper wire ST, cross-sectional area of the isolated copper wire ST_i, wire effective resistivity ρ, and the maximum frequency f_{max}. This frequency represent the upper limits at which 100% skin depth can still be maintained, meaning that no skin effect occurs.

Before applying the proposed design technique, a classical design procedure will be presented in order to serve as a benchmark for the strategy discussed in this chapter. It is known that it can be challenging to arbitrate the design parameters defined in (6.15), however, they will be chosen based on the literature in order to achieve a fair comparison with the optimized design.

6.2.2 **Benchmark Design**

The classical design of the converter serves as the benchmark design and acts as the starting point for the optimization algorithm. In order to initiate this process,

Table 6.4 – EE core data.

Core EE	A_eA_w [cm^4]	A_e [cm^2]	MLT [cm]	V_e [cm^3]	V_{box} [cm^3]
20/10/5	0.08	0.31	4.28	1.34	5.10
25/10/6	0.17	0.39	4.90	1.935	6.22
30/15/7	0.48	0.6	6.7	4	17.10
30/15/14	1.02	1.2	6.9	8.174	22.5
40/17/12	1.05	1.48	7.7	11.30	33.05
42/21/15	2.84	1.81	9.70	17.6	56.45
42/21/20	3.77	2.40	9.70	23.30	65.89
55/28/21	8.85	3.54	11.60	42.50	110.88
65/33/26	19.68	5.32	14.80	78.20	184.15

Table 6.5 – AWG round copper wire parameters.

AWG	ST [cm^2]	ST_i [cm^2]	ρ_r [Ω/cm]	f_{max} [Hz]
18	0.008231	0.009735	0.000280	16220
19	0.006527	0.007794	0.000353	22460
20	0.005176	0.006244	0.000445	25790
21	0.004105	0.005004	0.000561	32520
22	0.003255	0.004013	0.000708	41010
23	0.002582	0.003221	0.000892	51720
24	0.002047	0.002586	0.001125	65210
25	0.001624	0.002078	0.001419	82230
26	0.001287	0.001671	0.001789	103700
27	0.001021	0.001344	0.002256	130700
28	0.000810	0.001083	0.002845	164900
29	0.000642	0.000872	0.003587	207900
30	0.000509	0.000704	0.004523	262100

the vector of optimization variables $\boldsymbol{x}$ must be carefully chosen.

As already discussed in previous chapters, owing to the pulsating input power, off-line LED drivers have an output voltage ripple at twice the line frequency. These instantaneous power fluctuations are typically filtered out by a large bus capacitor. Therefore, in this benchmark design, the bus capacitance C_B is set to the minimum value capable of satisfying the maximum low-frequency ripple constraint in the LEDs.

The normalized ac-side load resistance Q, the inductance ratio λ, and the normalized switching frequency f_n are parameters that determine the design of passive elements in the second stage. The PC stage is typically designed to operate at the series resonant frequency, thus achieving high efficiency. Therefore, $f_n = 1$ was chosen. On the other hand, the load resistance and inductance are usually selected from the studied values (arbitrary) to achieve the desired gain. Values of 0.8 and 0.167 were chosen for resistance and inductance, respectively, which fall within the range of values used in practical designs found in the literature (SEMICONDUCTOR, 2012; HUANG, 2010; MA et al., 2018a; WANG et al., 2015b; WANG et al., 2017; FENG; LEE; MATTAVELLI, 2014). It's worth noting that these parameters were adopted in the design of the LLC converter presented in Chapter 3, which yielded good results.

6.2.3 **Multi-Objective Based-Design**

This subsection applies the methodology for systematic design of a high-performance LED driver, shown in section 6.1, whose topology was obtained by integrating a totem-pole bridgeless boost PFC and a half-bridge LLC resonant converter.

6.2.3.1 *Multi-objective function*

For the sake of simplicity, the total cost of the converter (c_4) was not taken into account in this case study. Therefore, the multi-objective function is given by:

$$\begin{aligned} &\min f_{obj}(\boldsymbol{x}) = \sum_{i=1}^{3} w_i c_i(\boldsymbol{x}) \\ &\text{s.t. } A(\boldsymbol{x}) \leq 0_{[8,1]}. \\ &\boldsymbol{x_{lb}} \leq \boldsymbol{x} \leq \boldsymbol{x_{ub}}. \end{aligned} \tag{6.16}$$

The values of w_i should be chosen according to the desired weight in each single-objective cost function. It was defined $w_1 = 1$, $w_2 = 10$, and $w_3 = 2500$, which makes 1cm^3 equivalent to 10W and 2500 failures/10^6 hours for the optimization algorithm, representing a good compromise between the performance parameters. The Pareto Front could be investigated to indicate the best possible compromise with respect to different performance indices (KOLAR et al., 2010). However, the primary focus of this work lies in formulating the optimization problem, which could be further refined by incorporating additional analyses.

6.2.3.2 *Constraint Functions*

The vector containing the constraints can be organized in the form of a column vector which addresses 8 constraints, as given by (6.17). The first one limits the output current ripple so that a good photometric performance of the LEDs is ensured. For this analysis, only the low-frequency ripple is being considered. The second constraint ensures that only designs with a high power factor will be allowed. The constraints of the third to the seventh row treat the compliance of the input current harmonic content with the IEC-61000-3-2:2018 standard (Class C). In order to reduce the computational cost, the harmonics above the 11^{th} were not considered. On the other hand, the constraint related to the bus voltage, $v_B(t)$, ensures the safe operation of the bus capacitor and the semiconductors.

$$A(\boldsymbol{x}) = \begin{pmatrix} \Delta I_o - \Delta I_{omax} \\ -PF + 0.92 \\ I_3 - 0.3PFI_1 \\ I_5 - 0.1I_1 \\ I_7 - 0.07I_1 \\ I_9 - 0.05I_1 \\ I_{11} - 0.03I_1 \\ v_B(t) - v_{Bmax} \end{pmatrix}. \tag{6.17}$$

6.2.3.3 *Definition of the search-space*

The set of all the possibilities of $\boldsymbol{x}$ is called the search space. As can be seen in (6.16), the optimization variables take on values between the bounds $\boldsymbol{x_{lb}}$ and $\boldsymbol{x_{ub}}$. These vectors with the lower and upper bounds were defined by (6.18) and (6.19), respectively, allowing for the optimization algorithm to explore a wide search space.

$$\boldsymbol{x_{lb}} = \begin{bmatrix} 5.6\mu & 0.08 & 0.00167 & 0.5 \end{bmatrix}, \tag{6.18}$$

$$\boldsymbol{x_{ub}} = \begin{bmatrix} 470\mu & 8 & 16.7 & 1.5 \end{bmatrix}. \tag{6.19}$$

6.2.3.4 *Single-objective cost functions*

As indicated in (6.17), the converter's performance related to power quality has been modeled as a constraint in the optimization problem. On the other hand, the individual cost functions are represented by volume, losses, and failure rate models. It is important to note that the size of the magnetic elements can have a significant impact on converter volume and losses.

As shown in Figure 6.1, the design of discrete elements occurs after the converter equations are solved. Thus, with the identified critical operating condition, the design of magnetic elements (boost inductor, series resonant inductor and transformer) follows a sequence of steps. First, based on the maximum rms current and the maximum frequency of the Table 6.5, the wire specifications are determined. Then, based on the well-established AeAw method (BARBI, 2007), the minimum required core size is defined according to Table 6.4. Next, the number of turns for each coil is calculated. Finally, an estimation for the dc resistance of the coil is obtained, considering wire parameters and the number of turns.

The boxed volume of the magnetic elements is shown in the last column of Table 6.4. The boxed volume of the capacitors is shown in Table 6.3. However, as will be shown in the following, the chosen optimization algorithm requires continuous cost functions. Then, in order to achieve a continuous function, the fitting curves given by (6.20) and (6.21) were used to calculate the approximate boxed volume of the magnetic elements and capacitors, respectively.

$$V_{L\_i} = k_{L1} L_i^2 + k_{L2} L_i + k_{L3}, \tag{6.20}$$

$$V_{C\_i} = k_{C1} C_i V_r^2 + k_{C2}, \tag{6.21}$$

where k_{L1}, k_{L2}, k_{L3}, k_{C1} and k_{C2} are obtained from manufacturers' data. The inductance L_i can assume the values L_b, L_s, and L_m. Similarly, capacitor C_i can take on the

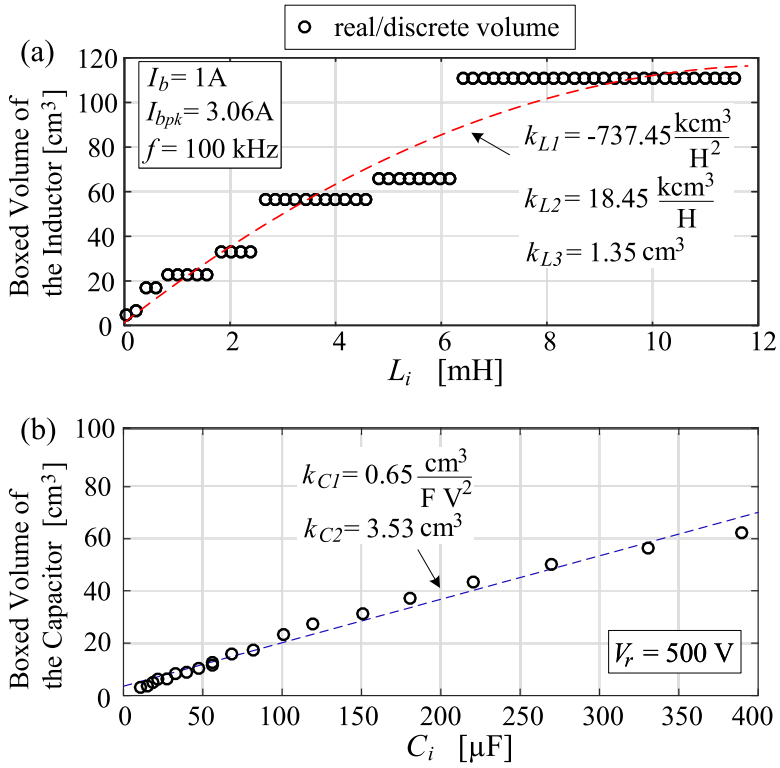


Figure 6.3 – Fitting curves. Boxed volume (a) of the inductor and (b) of the capacitor.

values C_b, C_s, and C_o. It is important to highlight that the coefficients are calculated for each passive element in each iteration of the optimization algorithm.

Therefore, from the estimated boxed volumes for each passive element, the cost function can be calculated by

$$c_1 = \sum_{i=1}^{3} V_{L\_i} + \sum_{i=1}^{3} V_{C\_i}. \tag{6.22}$$

Figure 6.3 illustrates this curve fitting process. The actual/discrete volume of the passive element is represented by the circles on the graph, while the dotted line corresponds to the fitted curve. Figure 6.3a shows the boxed volume of the inductor according to the inductance values considering the rms current of 1 A, peak current of 3 A, and frequency of 100 kHz. The boxed volume of the capacitor according to the capacitance values for Al-Caps with voltage of 500 V is shown in Figure 6.3b.

In this work, the converter power losses are calculated based on classic losses models. With respect to magnetic elements, the power losses were estimated considering core and copper losses, as shown in (6.23). Core losses primarily arise from two factors: hysteresis losses and eddy current losses, and can be calculated by (6.24), in terms of the core volume V_e, peak of the magnetic flux density B, and frequency f. On the other hand, copper losses are calculated by (6.25).

$$P_{L\_i} = P_{core} + P_{wire}. \tag{6.23}$$

$$P_{core} = V_e \left(K_h B^{\alpha_c} f + K_e B^2 f^2 \right), \tag{6.24}$$

in which K_h, K_e and α_c are coefficients dependent on the core material. For ferrite core, K_h = 4e-5, K_e = 4e-10 e α_c = 2.4 (BARBI, 2007).

$$P_{wire} = R_{dc} I_{rms}^2 + 2 R_{dcsec} I_{sec}^2, \tag{6.25}$$

where R_{dc} is the winding dc resistance and I_{rms} is the rms current through the inductor. For the case of a transformer, which has more than one winding, R_{dcsec} and I_{sec} are the dc resistance and rms current of the secondary, respectively.

The losses in the capacitors can be calculated by (6.26), which is derived from the simplified equivalent circuit of the capacitor (MENKE, 2021). As can be seen, the losses are determined by the rms current and capacitor dissipation factor DF, which is obtained from the capacitor datasheet.

$$P_{C\_i} = \left(\frac{DF}{2\pi f C\_i} \right) I_{Ci\_rms}^2 \tag{6.26}$$

For the sake of simplicity, the losses in the semiconductors were computed by focusing solely on the conduction component. It is important to note that the converter has two pairs of diodes. Therefore, the losses in each pair can be estimated by

$$P_{D\_i} = 2 \left(I_{Di\_avg} V_{F\_i} + R_{D\_i} I_{Di\_rms}^2 \right), \tag{6.27}$$

in which V_{F_i} is the diode forward voltage and R_{D_i} is the dynamic series resistance, both of which can be found in the diode datasheet.

On the other hand, the switching loss was considered in (6.28) to estimate the half-bridge switches power losses (FANG et al., 2015). The drain-source on-state resistance R_{on}, the rising time of the drain-source voltage t_r and the falling time t_f of the current are obtained from the MOSFET datasheet. In addition, I_{M_off} is the turn-off current obtained from the time-domain analysis. As outlined by Paula et al. (2018), this classical approach is susceptible to errors as it disregards critical factors such as the gate driver, parasitic inductances, and the nonlinearity of MOSFET capacitances. Nonetheless, in this study, the significance of switching losses is mitigated due to the Zero Voltage Switching (ZVS) operation.

$$P_M = 2 \left(R_{on} I_{M\_rms}^2 \right) + V_B I_{M\_off} (t_r + t_f) f. \tag{6.28}$$

Therefore, the total losses are given by (6.29), which includes the losses in the boost inductor, resonant inductor, transformer, resonant capacitor, bus capacitor, output capacitor, two pairs of diodes, and MOSFETs.

$$c_2 = \sum_{i=1}^{3} P_{L\_i} + \sum_{i=1}^{3} P_{C\_i} + \sum_{i=1}^{2} P_{D\_i} + P_M. \tag{6.29}$$

The function c_3 represents the estimated failure rate, which is the number of failures per million hours of operation (HARMS, 2010). The reliability of capacitors is strongly affected by the temperature, voltage, capacitance, and technology used. In this work, aluminum electrolytic capacitors (Al-Caps) were used in the bus because of their lower cost and volume. Additionally, this type of capacitor is the most critical element and is responsible for most failures (ALMEIDA et al., 2015c). Therefore, only the bus capacitor was considered when estimating the number of failures in time. According to Chapter 2, the failure rate can be calculated by (6.30).

$$c_3 = 3\lambda_b e^{\left[\frac{-E_a}{K_B}\left(\frac{1}{T_a+273}-\frac{1}{298}\right)\right]} \left[\left(\frac{V_{\max}}{0.6V_r}\right)^5 + 1\right] C_B^{k_c} \tag{6.30}$$

where T_a is the ambient temperature and $V_{\max}$ is the maximum applied voltage. The values of the constants λ_b, E_a and k_c have different values for each capacitor technology. For Al-Caps, λ_b=0.00012, E_a=0.35 and k_c=0.23.

6.2.3.5 *Design of the Control Loop*

The switching frequency function defined by (6.8) must be synthesized by the control loop. The average value of the switching frequency ensures that the system will have null steady-state error under constant current reference. This null error can be obtained through the C_{av} compensator, which is a pure integrator shown in (6.31). In this case, C_{av} must attenuate all the oscillating components of the error signal.

$$C_{av}(s) = -\frac{K_a}{s}. \tag{6.31}$$

On the other hand, the oscillating component of $f(t)$ can be synthesized using a second-order band-pass filter, given by (6.32), tuned with a center angular frequency of $2\omega_L$. In this compensator, B is the filter bandwidth and K_{bp} is the gain at center frequency, which can be obtained by (6.33).

$$C_{bp}(s) = K_{bp}\frac{Bs}{s^2 + Bs + 4\omega_L^2}. \tag{6.32}$$

$$K_{bp} = \frac{f_0 k_f}{V_{max} - V_B}. \tag{6.33}$$

As performed in Chapter 5, the control system of this chapter was digitally implemented by using the TIVA C-Series microcontroller. The details of the digital implementation process, including the discretization of the control loop elements, are provided in Section 5.2.3.

6.2.3.6 *Optimization Algorithm*

Several optimization algorithms can be used to solve the problem defined in (6.1), such as genetic algorithms, heuristic methods, or exhaustive search. Due to its simplicity and effectiveness, a gradient descent-based algorithm was used for this work (WANG et al., 2022). Gradient descent is a simple yet powerful optimization algorithm that can be used to minimize a function of one or more variables. The algorithm lies in its iterative approach, wherein it systematically navigates towards the minimum of the function by following the negative gradient—essentially, the steepest descent.

The gradient of a function is a vector that points in the direction of the most substantial increase in the function. The gradient for the function f_{obj} at a given point $\boldsymbol{x_n}$ is defined by (6.34). The optimization algorithm chosen for this example requires continuous cost functions so that the gradient is not zero in any situation. The gradient descent algorithm iteratively calculates the next point $\boldsymbol{x_{n+1}}$ by means of (6.35).

$$\nabla f_{obj}(\boldsymbol{x_n}) = \begin{bmatrix} \dfrac{\partial f_{obj}}{\partial x_1} & \dfrac{\partial f_{obj}}{\partial x_2} & \dfrac{\partial f_{obj}}{\partial x_3} & \dfrac{\partial f_{obj}}{\partial x_4} \end{bmatrix} \tag{6.34}$$

$$\boldsymbol{x_{n+1}} = \boldsymbol{x_n} - \alpha \nabla f_{obj}(\boldsymbol{x_n}), \tag{6.35}$$

where α is the learning rate, which is the parameter that scales the gradient and thus controls the step size. This parameter is typically chosen to be small enough to ensure that the algorithm does not overshoot the local minimum of the function.

Figure 6.4 shows the flowchart of the optimization algorithm implemented to design an off-line high-performance LED driver with frequency-based ARC. The algorithm starts by choosing an initial point in the search space. This point is the benchmark design that is based on the classical converter design and generates satisfactory results, as described in section 6.2.2. The initial value of f_{obj} is calculated, and then the algorithm moves in the direction of the negative gradient by a small step size. When calculating a new value of f_{obj}, the maximum ripple constraint on the LED current is checked and the value of k_f can be changed if necessary to meet the constraint. This loop is highlighted in Figure 6.4 and is responsible for inserting the frequency-based ARC technique.

It can be noted that the relative amplitude k_f was not included in the vector containing the optimization variables. This omission aimed to streamline computati-

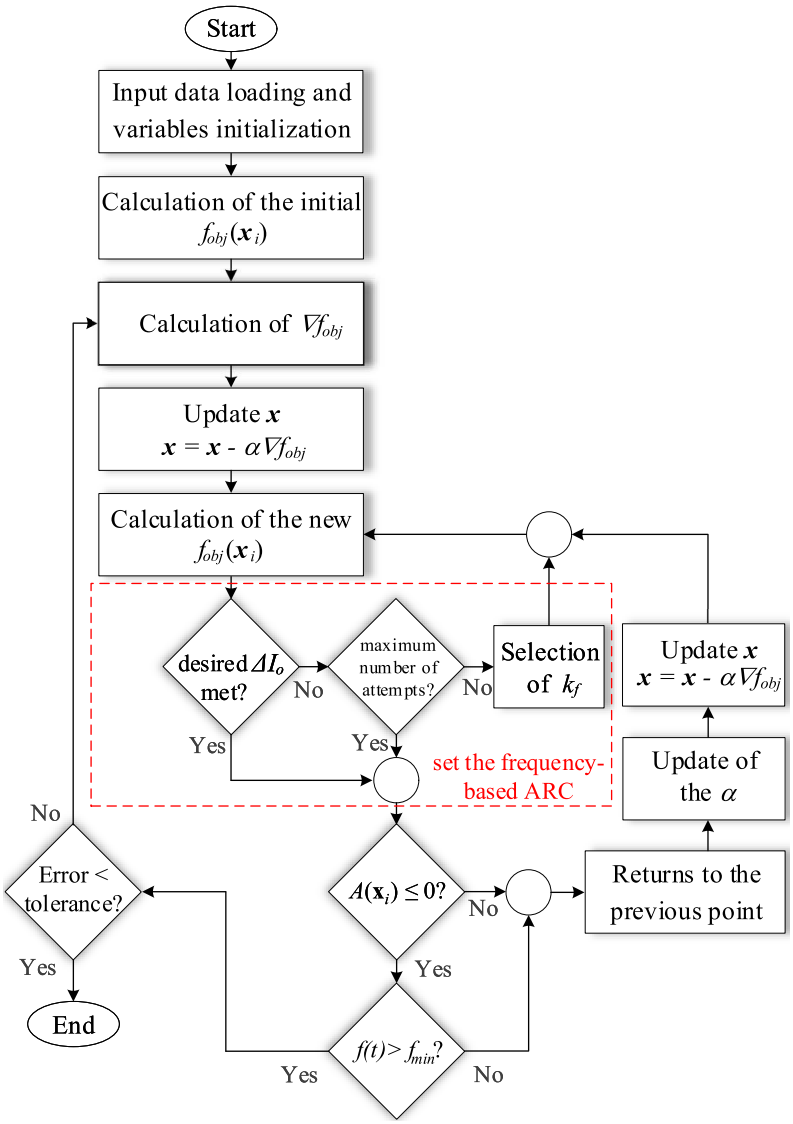


Figure 6.4 – Flowchart of the optimization algorithm used to design an off-line high-performance LED driver.

onal efficiency in the gradient calculations. Additionally, the partial derivative of the objective function can yield an infeasible point. For instance, decreasing capacitance without a corresponding value of k_f may cause the converter to violate the maximum ripple constraint. Consequently, reassessment and the identification of a new point become necessary, elongating the convergence process of the algorithm. In contrast, the proposed method exhibits a more efficient convergence, requiring fewer interaction points to arrive at a feasible solution.

When the algorithm exits the ARC loop, all constraints addressed in (6.17) are checked. If any of them are not met, the current point is discarded and the algorithm returns to the previous point. Then, the value of α is penalized to reduce the step size. Thus, a new $\boldsymbol{x}$ is computed, returning to the beginning of the ARC loop. If all constraints are met, including the minimum frequency constraint, a new feasible

point with a lower value of f_{obj} is found. Then, all steps are performed again, and the algorithm ends only when the difference between the values of f_{obj} of the last two feasible points is less than the tolerance. This means that the value of the function at the current point is no longer changing significantly.

It is important to note that the algorithm based on gradient descent can also be trapped in local minima. In the other words, the algorithm may converge to a point that is not the global minimum of the function. However, it is often effective for finding good solutions to optimization problems.

6.2.4 **Optimization Results**

In order to solve the optimization procedure defined in (6.1), a set of MATLAB scripts were produced based on the optimization algorithm outlined in Section 6.2.3. Such pieces of software can be found in the appendix B. By running the code described with the parameters and search space defined in Section 6.2, the optimized design of the LED driver is obtained.

It is well established that in a commercial LED driver, the passive elements account for the majority of the converter's total volume. To simplify the analysis, this work defines a subtotal power density for the converter, ρ_s^*, which considers only the passive elements.

Table 6.6 shows the main results for each feasible point. Iteration 0 is the starting point and represents the benchmark design of the converter, which generated a f_{obj} of 410.02. For the initial guess of the optimization algorithm (benchmark), the converter is configured to operate at the resonance frequency, yielding an estimated efficiency of 90.87%. Notably, as this follows a conventional design, the Active Ripple Compensation (ARC) technique was not taken into account ($k_f = 0$). Consequently, a capacitance of 330 μF is required to meet the specified ripple requirements. This choice significantly influences the overall volume of the passive elements (90.35 cm^3) and adversely affects the power density, resulting in 1.07 W/cm^3 for this particular design.

The algorithm successfully converged to the optimized solution (according to the tolerance of 5) at the fifth feasible point found. The normalized frequency was slightly reduced (x_4=0.927), keeping the converter in ZVS and resulting in high efficiency. It is important to highlight that the efficiency of the optimized and benchmark converter is very similar, since the algorithm started from an efficient point. However, the use of the frequency-based ARC technique with k_f=5.6% made it possible to use a capacitance of only 27μF, significantly reducing the total volume of the passive elements to 42.68 cm^3 and increasing the subtotal power density to 2.26 W/cm^3.

The optimization results showed the effectiveness of a systematic design approach, in which few parameters were determined by the designers. In addition to the slight increase in efficiency, there was a significant improvement in performance indices, such as a 38.25% reduction in failure rate, a 52.76% reduction in volume, and a 111.69% increase in subtotal power density. The drawback of the optimized design was a slight increase in the THD of the input current. In practical terms, this represents a negligible impact on any of the performance parameters, yielding a high-performance LED driver.

Table 6.6 – Optimization Results

Iterations	x_1	x_2	x_3	x_4	c_1 [cm^3]	c_2 [W]	c_3 [failures/10^{6}h]	f_{obj}	f_0 [kHz]	k_f [%]	THD [%]	η [%]	C_B [μF]	Vol [cm^3]	ρ_s^* W/[cm^3]
0	264	0.8	0.167	1	77.12	9.70	0.094	410.02	100	0	9.10	90.87	330	90.35	1.07
1	196.27	0.734	0.190	0.98	64.39	9.04	0.088	375.15	98.2	0.8	9.11	91.44	330	84.55	1.14
2	99	0.675	0.201	0.967	47.57	8.96	0.076	327.95	97.3	1.6	9.10	91.52	180	64.18	1.51
3	41.21	0.599	0.217	0.956	37.03	8.00	0.065	279.96	96.4	3.2	9.10	92.35	100	46.52	2.08
4	26.08	0.587	0.210	0.926	35.96	8.40	0.059	268.73	93	4.8	9.31	92	33	42.53	2.27
5	21.49	0.567	0.207	0.927	35.03	8.48	0.058	265.49	93	5.6	9.38	91.93	27	42.68	2.26
Reduction	-	-	-	-	-	-	38.25%	-	-	-	-3.08%	-1.16%	91.82%	52.76%	-111.69%

In this chapter, the performance analysis tool was adapted to a quantitative representation, quantifying power quality (THD of the input current), reliability (failure rate), and power density (subtotal power density). The cost savings associated with reducing the bus capacitance were also taken into account. A price quote for bus capacitors was obtained from Digi-Key on November 17, 2023, based on the unit cost for purchasing 1000 units. The performance indexes of the benchmark and optimized converter are graphically illustrated in Fig. 6.5. The scales of the axes of these parameters were defined for clear visualization, considering the qualitative analysis tool, where a further distance from the center of the graph indicates better performance.

As can be seen in this figure, the optimized converter demonstrated a slight improvement in efficiency. However, the huge reduction in bus capacitance (91.87%) led to substantial improvements in reliability and power density, as well as cost. While the 330-μF capacitor (LGN2H331MELC45) was priced at \$7.33058, the 27-μF capacitor (UCY2H270MHD) had a price of \$1.39929, yielding a cost savings of \$5.9313. Regarding power quality, a negligible THD was observed, highlighting the feature of a high-performance driver.

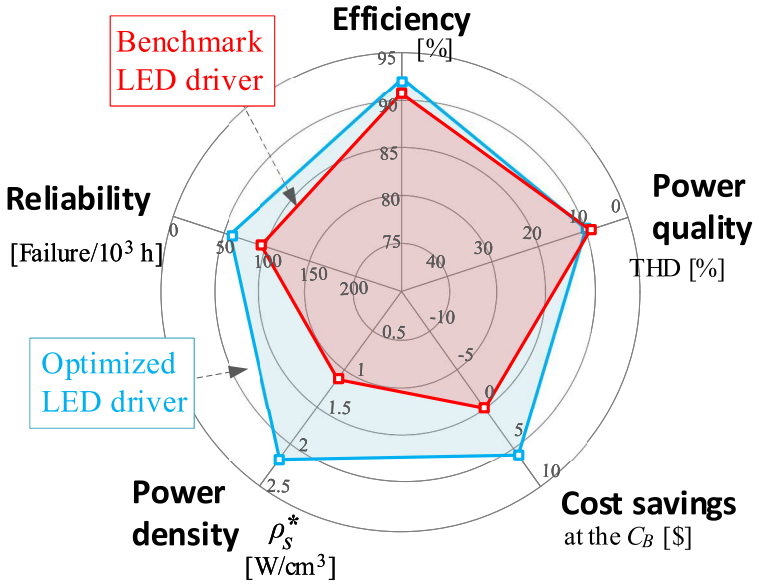


Figure 6.5 – Performance analysis of benchmark and optimized converter.

6.3 EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, two prototypes were built: one for the benchmark design and one for the optimized design. Figure 6.6 shows the prototypes, highlighting the bus capacitor used in each. Table 6.7 presents the main elements used in the prototypes.

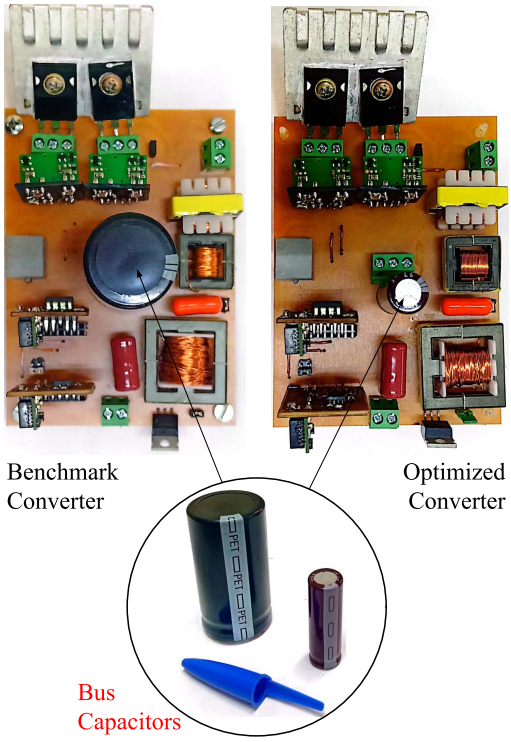
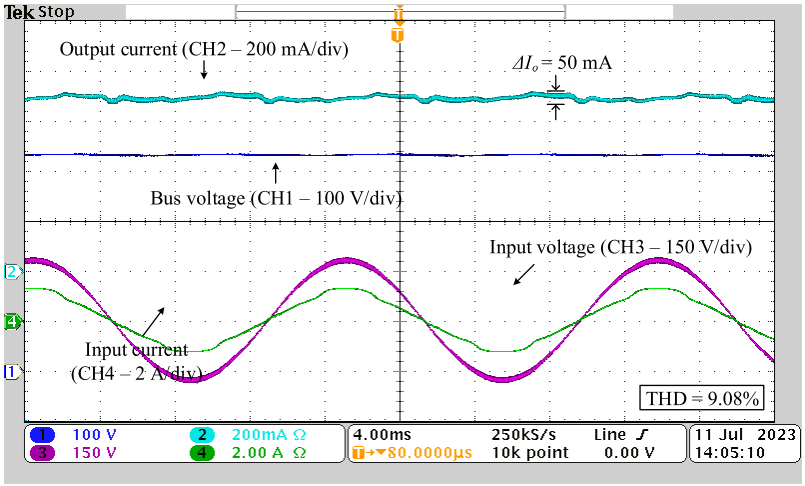


Figure 6.6 – Photographs of prototypes, highlighting the bus capacitors.

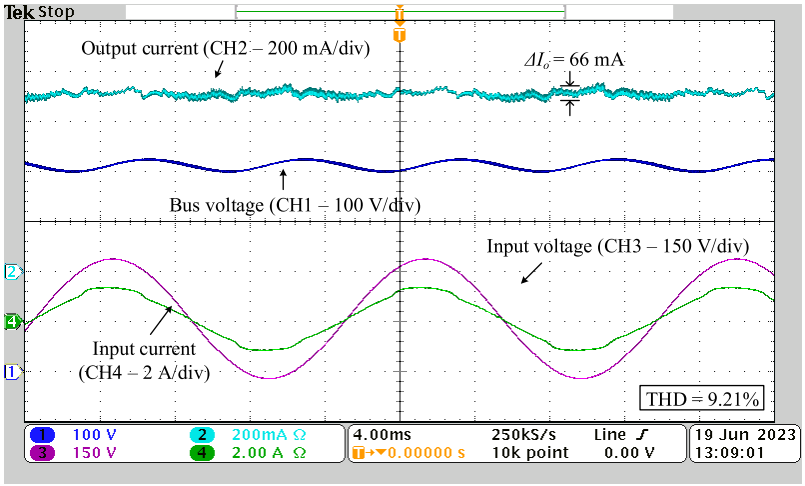
Table 6.7 – Main Parameters of Design Example Prototypes

Item	Value
Half-bridge switches	2 x IRFP460 (500V / 0.27Ω)
Boost diodes	2 x MURS360 / (600V / 3A)
Output rectifier diodes	1 x MUR820 / (200V / 8A)
EMI Filter	CM:5 mH / DM: 470μH / 220nF
Sensors and gate drivers	AMC-1200 and HCPL-3120 (ALBUQUERQUE et al., 2017)
	Benchmark Converter
Boost inductor L_b	280μH / NEE 25-10-6 / 79 turns gap = 0.48 mm / 2x26 AWG
Resonant inductor L_s	547μH / NEE 20-10-5 / 56 turns gap = 0.12 mm / 1x26 AWG
LLC Transformer L_m	2.85mH / NEE 30-15-7 / 106:65:65 turns gap = 0.12 mm / 1x26 AWG / n=1.63
Bus capacitor C_B	330μF / 500V electrolytic capacitor (LGN2H331MELC45)
Resonant capacitor C_s	6.8nF / 630V polypropylene capacitor (B32692A6682)
Output capacitor C_o	3.9 μF / 250V polyester film capacitor (ECQE2395)
	Optimized Converter
Boost inductor L_b	323μH / NEE 25-10-6 / 92 turns gap = 0.6 mm / 2x26 AWG
Resonant inductor L_s	381μH / NEE 20-10-5 / 49 turns gap = 0.12 mm / 1x26 AWG
LLC Transformer L_m	1.66mH / NEE 30-15-7 / 82:49:49 turns gap = 0.12 mm / 1x26 AWG / n=1.68
Bus capacitor C_B	27μF / 500V electrolytic capacitor (UCY2H270MHD)
Resonant capacitor C_s	6.8nF / 630V polypropylene capacitor (B32692A6682)
Output capacitor C_o	3.9 μF / 250V polyester film capacitor (ECQE2395)

Figure 6.7 presents some experimental waveforms from the two off-line LED drivers. The waveforms show the input current and voltage, the bus voltage, and the output current. The low-frequency output current ripple obtained from the benchmark converter (Figure 6.7a), which requires a much higher bulk capacitance at the output of the PFC stage, was 50 mA. Meanwhile, Figure 6.7b presents experimental waveforms obtained for the optimized converter. Even with a higher bus voltage ripple, the output current ripple still within the requirements. In other words, frequency-based ARC technique made it possible to use a bus capacitance of only 27 μF. It is important to highlight that the optimized converter showed an increase of only 0.13% in the total harmonic distortion of the input current compared to the benchmark converter. This distortion was predicted during the design procedure to ensure that the harmonic content of the input current remains in compliance with the IEC-61000-3-2:2018 standard, as shown in Figure 6.8. The PF measured in both converters was 0.99.



(a)



(b)

Figure 6.7 – Experimental waveforms obtained from (a) the benchmark converter ($C_B = 330$ μF) and (b) the optimized converter ($C_B = 27$ μF).

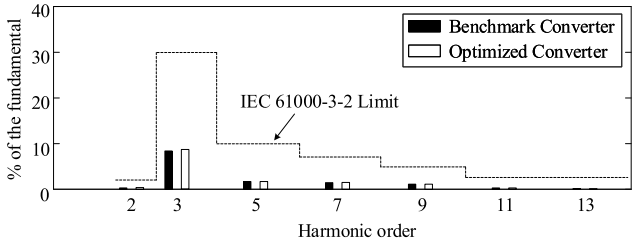


Figure 6.8 – Harmonic content of the input current compared with IEC limits

Figure 6.9 presents experimental waveforms of the current and voltage of the MOSFET M_1 and the output rectifier diode at the positive and negative peak of line voltage. The tank waveforms are shown in Figure 6.10 for both converters. As can be seen in these figures, the benchmark converter operates very close to the series resonant frequency, and the measured efficiency was 90.26%. The optimized converter operates below series resonant frequency and under ZVS. In this case, the measured efficiency was 90.96%. Table 6.8 shows the measured loss distribution for both prototypes, which was obtained at nominal input voltage and rated load by using a Yokogawa WT230 digital power meter. Furthermore, those measurements did not take into account the consumption of the EMI filter and the control board.

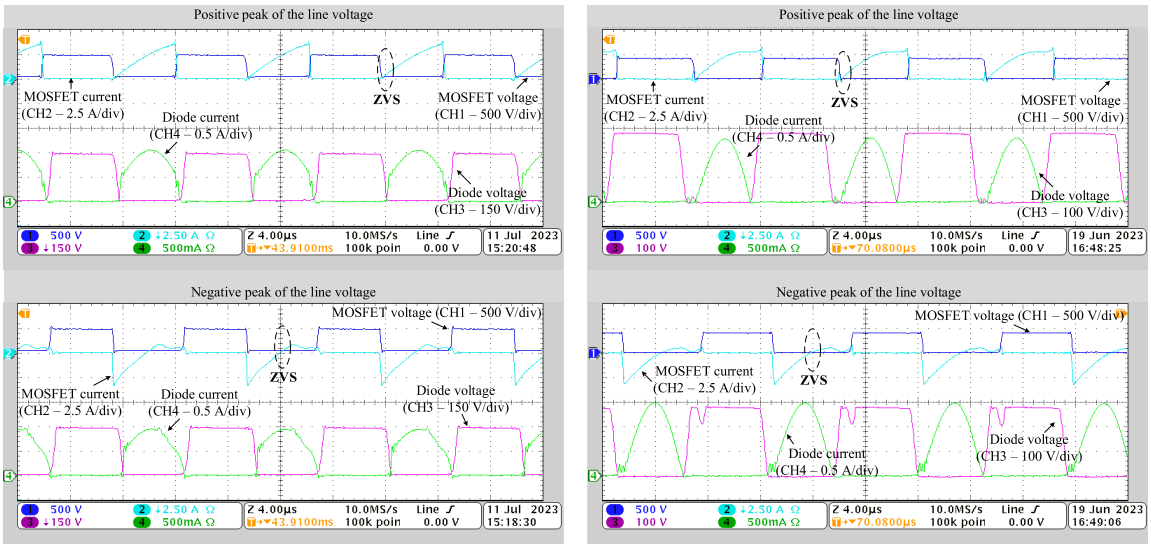


Figure 6.9 – Waveforms measured at the positive and negative peak of line voltage obtained from the (a) benchmark and (b) the optimized converter.

Figure 6.11 presents the output current ripple, THD, and efficiency of the converter according to variations in the input voltage. The results showed that the output current ripple of the optimized converter increased at higher input voltages, but not at low voltages (Figure 6.11a). The reason for this is that the open-loop control branch that inserts the modulation was designed for the nominal condition. A small increase in THD of the input current was observed in Figure 6.11b. In addition, good efficiency values were achieved across the entire range (Figure 6.11c).

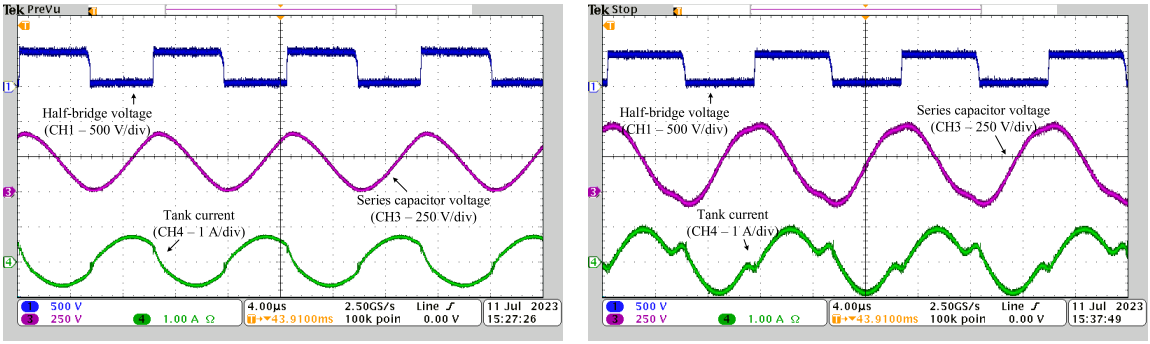


Figure 6.10 – Experimental waveforms of the resonant tank obtained from the (a) benchmark and (b) the optimized converter.

Table 6.8 – Loss Breakdown

Components	Benchmark	Optimized
MOSFETs	1.75 W	1.69 W
Boost diodes	1.35 W	1.30 W
L_b	1.48 W	1.38 W
C_B	0.11 W	0.10 W
C_s	0.19 W	0.17 W
L_s	0.95 W	0.85 W
L_m	3.50 W	3.14 W
Output diodes	1.02 W	0.90 W
C_o	0.07 W	0.07 W
Total	10.42 W	9.60 W

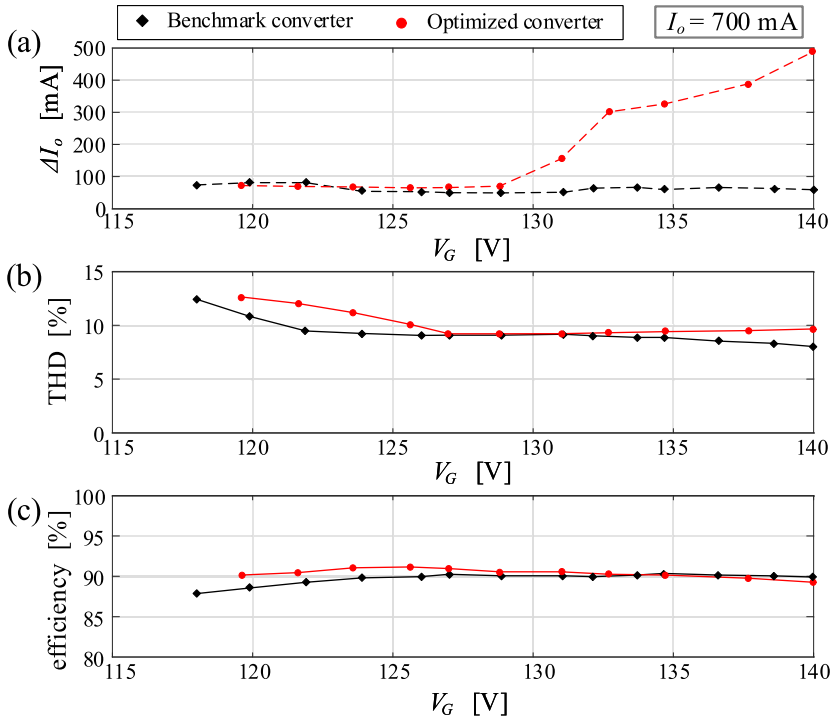


Figure 6.11 – Output ripple, THD and efficiency of the converter according to variations in the input voltage.

The behavior of the output current ripple, THD and efficiency owing to variations in the output power is presented in Figure 6.12. As mentioned earlier, the output current ripple of the optimized converter was not predicted for operation outside the nominal condition. Reducing the output power led to an increase in ripple for the optimized converter, as shown in Figure 6.12a. However, according to Figure 6.12b and Figure 6.12c, both converters exhibit similar THD and efficiency for variations in output power.

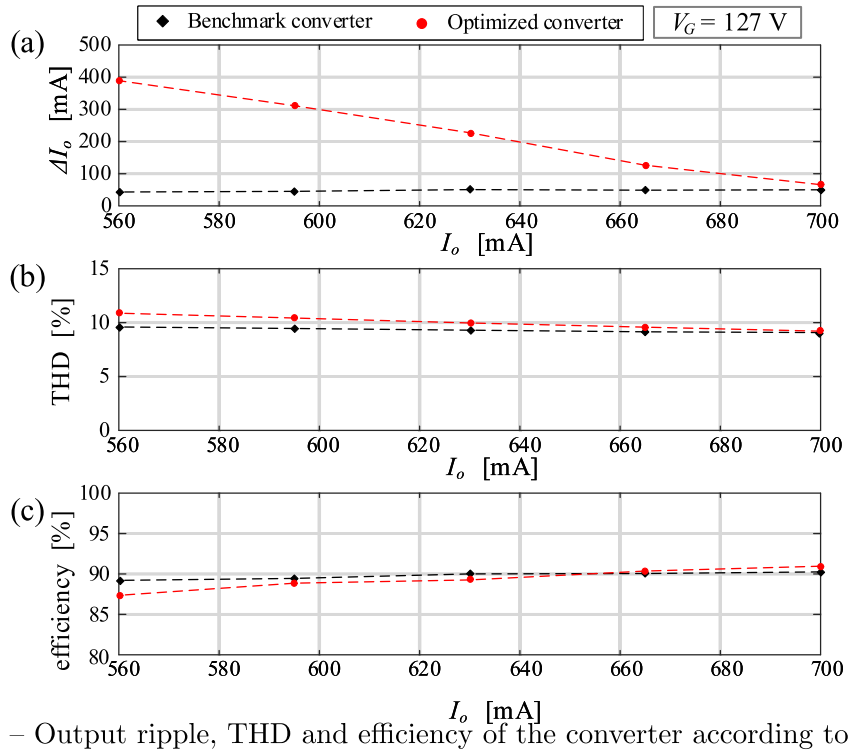


Figure 6.12 – Output ripple, THD and efficiency of the converter according to variations in the output power.

Despite the ARC control branch operates in an open-loop, the converter maintains a null steady-state error under constant current reference due to the average value of the switching frequency. This null error can be observed in Figures 6.13 and 6.14, which depict the dynamics of the optimized converter during steps in the reference and input voltage, respectively. The converter effectively follows step references and rejects disturbances in the input voltage. However, the maximum output current ripple constraint may not be met outside the operating point.

One of the drawbacks of this converter is that the output current ripple can be high when the LED driver operates outside the operating point. This disadvantage can be solved by adding an input voltage range and dimming in the constraint vector. This means that the ripple restriction will be met at all the desired operating points, which can lead to a lower capacitance reduction.

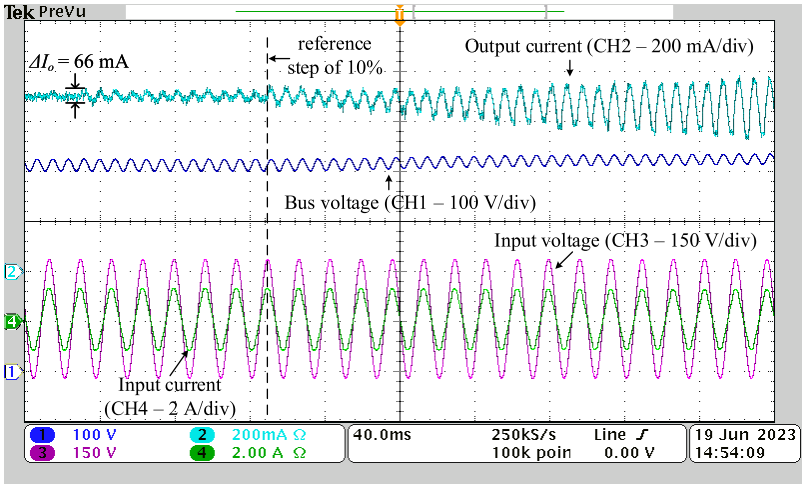


Figure 6.13 – Experimental waveforms of the optimized converter during a reference step.

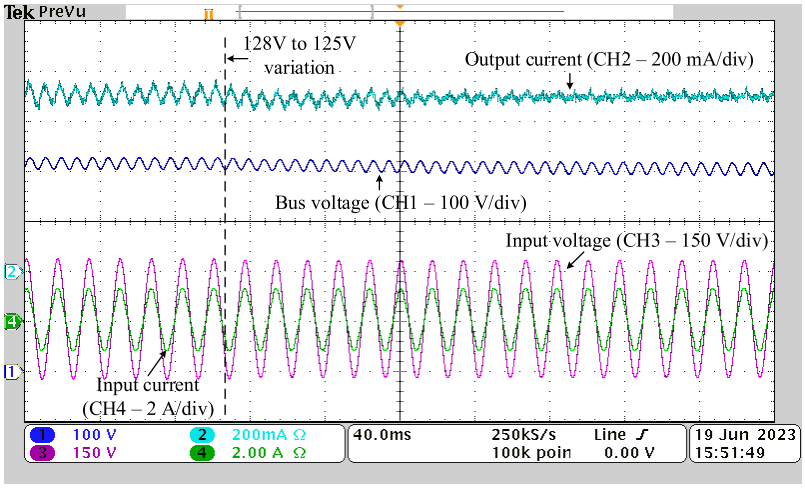


Figure 6.14 – Experimental waveforms of the optimized converter during a step of the input voltage.

6.4 SUMMARY OF THE CHAPTER

This Chapter presented a systematic design approach for high-performance LED drivers. The proposed design procedure was based on a constrained multi-objective optimization problem that aimed to minimize volume, losses, failure rate, and cost without significantly deteriorating the THD.

A case study was also detailed, using a topology that integrates a totem-pole bridgeless boost PFC and a half-bridge LLC resonant converter. The theoretical analysis included the accurate modeling of this topology and the frequency-based ARC technique, which are essential for achieving high-performance converters.

The optimization results, obtained from system specifications, operating requirements, and the availability of components and materials in the laboratory, demonstrated the effectiveness of the systematic design approach.

Experimental results from two prototypes verified the theoretical analysis, showing that the design methodology allowed for, among other improvements, a 38.25% reduction in failure rate, a 52.76% reduction in volume, and a 111.69% increase in subtotal power density. Therefore, this design approach is a promising strategy for designing high-performance LED drivers.

7 CONCLUSIONS AND PROPOSALS FOR FUTURE WORKS

7.1 CONCLUSIONS

This work proposed an approach for designing high-performance LED drivers that pursue enhanced efficiency, power density and lifetime, which are related to capacitance reduction. In order to reduce the capacitance, a frequency-based ARC technique was proposed as an alternative to the conventional ARC methodology (in which the duty cycle is modulated) allowing for a lesser negative impact on the THD of converters with a load-resonant PC stage. This alternative also increases the overall LED driver efficiency by employing soft-switching.

A review regarding the characteristics of the LED lighting system was presented, including the mandatory requirements for driving LEDs from the mains: power factor greater than 0.92 and reduced total harmonic distortion of the input current, as well as complying with the IEC-61000-3-2:2018 Class C standard. Moreover, some features of electrolytic and metallized-film capacitor technologies were discussed. This element contributes to cost, size and number of failures in time, which can be dramatically reduced with a capacitance reduction. The metallized-film capacitors provide a longer lifespan but decrease the power density of the drivers. Alternatively, a cheaper and compact LED driver is achieved by using electrolytic technology. Furthermore, some approaches for attenuating the output current ripple were also reviewed. Regarding the alternatives based on control methods, most of the techniques proposed in the literature allow for reducing the output current ripple by means of the modulation of the converter's duty cycle at the cost of an increase in the input current total harmonic distortion. In the case of integrated circuits, the combination of topology and control scheme can be selected mainly according to the input voltage, as most of them are complicated to operate at universal-input voltage.

Before discussing the frequency-based ARC technique, mathematical tools capable of evaluating and designing resonant converters with a wide variation of parameters are crucial. In this sense, an accurate model for analyzing resonant converters operating in the ZVS region applied to LED driving was presented, considering the low-frequency current ripple transmission. Given the accurate model of the LLC resonant converter, the frequency-based ARC technique was proposed to be applied in integrated off-line LED drivers for capacitance reduction. Thereafter, a more complete and generalized analysis of the active ripple compensation technique based on the large-signal modulation of the control variable in integrated off-line converters was presented, comparing duty-cycle versus switching frequency modulation. This generalized analysis was included to allow for the evaluation of the performance of several topologies with the ARC technique, addressing the output current ripple reduction and power quality regarding

each alternative. According to this analysis, load-resonant converters as PC stage are more sensitive than hard-switching converters, thus requiring a lower relative amplitude modulation - thus a lower control effort - for achieving the same ripple reduction. A lower relative amplitude modulation, in turn, implies a lesser negative impact on the THD of converters with a load-resonant PC stage. Moreover, resonant converters are more efficient. Hence, the strategy of the switching frequency modulation has several advantages and can be used to design LED drivers with high efficiency, very low capacitance with a small THD increase. The frequency-based ARC technique was applied to an off-line LED driver composed by integrating a totem-pole bridgeless boost PFC and a half-bridge LC series resonant converter. Experimental results proved that even for the less sensitive load-resonant converter, which requires a larger modulation amplitude and hence causes higher distortion, the frequency-based ARC technique allowed for a capacitance reduction of 66.6% while increasing only in 0.9% the input current THD. Furthermore, a good performance in terms of efficiency was achieved (compatible with single-stage off-line LED drivers).

Despite the excellent results achieved with frequency-based ARC techniques, the previous design approach for passive elements and control parameters relied on abacuses, which start with arbitrary initial assumptions. Additionally, performance parameters such as power losses, volume, failure rate, and system costs are interconnected, creating a trade-off relationship due to the multi-faceted nature of LED driver design. In order to address these challenges, a systematic design methodology based on a constrained multi-objective optimization problem was proposed for designing high-performance LED drivers, leveraging the accurate model and frequency-based ARC technique. A case study of a PFC bridgeless boost converter integrated with the LLC resonant converter was presented. The passive elements and controller are designed while improving several mutually coupled performance parameters according to the designer's requirements. Experimental results demonstrated the feasibility of the proposed design procedure, achieving significant improvements in performance parameters, such as a 38.25% reduction in failure rate and a 111.69% increase in subtotal power density. The optimized converter also achieved an efficiency of 90.96%, meeting the desirable characteristics for a high-performance LED driver.

7.2 PROPOSALS FOR FUTURE WORKS

The following topics address some proposals for continuity of the work that pursues alternatives for a high-performance LED driver, as well as expanding the number of features.

- Design the frequency-based ARC to maintain a low current ripple for other ope-

rating points, such as a wide input voltage range and dimming;

- Use of a single control branch with a wide-bandwidth controller responsible for both the control of the average current and the reduction of the output current ripple;
- Implementation of analog control to achieve simplicity and reduce cost;
- Study of the frequency-based ARC in topologies that can operate at high input voltage with low bus voltage (lower than 500V);
- Analysis of alternative control techniques that can be used together with the ARC so that the LED driver can achieve universal input operation;
- Improvement of the losses estimation, by using more sophisticated techniques;
- Incorporate the EMI filter and heatsink to improve the LED driver design and the volume estimation.
- Development of an optimization algorithm that evaluates and selects the most suitable semiconductors and topology for a given application;
- Explore other optimization algorithms to reduce the computational time or enlarge the search space;

7.3 RESULTING SCIENTIFIC OUTPUT

The papers published or accepted for publication as a direct result of this work are listed in the following.

- Papers published in journals:

1. FERRAZ, R. M. et al. Frequency-based Active Ripple Compensation Technique to Reduce Bulk Capacitance in Integrated Off-line LED Drivers. *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12209-12220, Oct. 2022, doi: 10.1109/TPEL.2022.3177155.
2. FERRAZ, R. M. et al. A Novel Design Approach for LLC Resonant Converters in Off-line LED Driving Applications. *Journal of Control, Automation and Electrical Systems*, v. 32, n. 6, p. 1758-1770, 2021.

- Papers published in international conferences:

1. FERRAZ, R. M. et al. Design of an Off-line LED Driver Based on the LC Resonant Converter with Active Ripple Compensation to Reduce Bulk Capacitance. In: *15th IEEE International Conference on Industry Applications (INDUSCON)*, São Bernardo do Campo, 2023.

2. FERRAZ, R. M. et al. Design of an Off-line LED Driver Based on the Interleaved BCM Boost PFC and the LLC converter with Active Ripple Compensation. In: *7th Brazilian Power Electronics Conference (COBEP)*, Florianópolis, 2023.

Moreover, some works published or accepted for publication were also indirectly results of the thesis, as listed below.

- Papers published in journals:

1. RESENDE, L. H. G. et al. An Off-line Single-Switch VLC Transmitter for Low Data Rate Applications. *AEUE - International Journal of Electronics and Communications*, v. 154, p. 154331, 2022.

- Papers published in international conferences:

1. RESENDE, L. H. G. et al. Performance Analysis of a FSK-based VLC System in Terms of BER, SNR, and Distance Range for Different Waveforms: Sinusoidal, Triangular, and Square. In: *7th Brazilian Power Electronics Conference (COBEP)*, Florianópolis, 2023.

2. RESENDE, L. H. G. et al. A Comparative Study on Off-line LED Drivers: High Frequency SEPIC-Based PFC Converter Against Low Frequency Boost-Based Pre-regulators. In: *15th IEEE International Conference on Industry Applications (INDUSCON)*, São Bernardo do Campo, 2023.

- Patent application:

1. RESENDE, L. H. G. et al. Sistema Transmissor de Dados Digitais por meio da Comunicação por Luz Visível Utilizando um Driver de LED de Estágio Único com Chave Única de Elevado Fator de Potência, 2022. Número do registro: BR1020220032114.

REFERENCES

ABDELMESSIH, G. Z. et al. Fully integrated buck and boost converter as a high efficiency, high-power-density off-line led driver. *IEEE Transactions on Power Electronics*, v. 35, n. 11, p. 12238–12251, 2020.

ABNT, N. 16026–requisitos de desempenho de dispositivo de controle eletrônico cc ou ca para módulos de led. *Janeiro de*, 2012.

ALATAILAT, M.; ELREHAIL, H.; EMEAGWALI, O. L. High performance work practices, organizational performance and strategic thinking: A moderation perspective. *International Journal of Organizational Analysis*, Emerald Publishing Limited, 2019.

ALBERTSEN, A. Electrolytic capacitor lifetime estimation. *JIANGHAI Eur. GmbH*, p. 1–13, 2010.

ALBUQUERQUE, V. M. et al. Development of a compact platform for power converter prototyping. In: *2017 Brazilian Power Electronics Conference (COBEP)*. [S.l.: s.n.], 2017. p. 1–6.

ALMEIDA, P. S. *Síntese de conversores ressonantes com alto fator de potência e alta eficiência para o acionamento de diodos emissores de luz*. Tese (Doutorado em Engenharia Elétrica) — Universidade Federal de Juiz de Fora, 2014.

ALMEIDA, P. S. et al. Static and dynamic photoelectrothermal modeling of led lamps including low-frequency current ripple effects. *IEEE Transactions on Power Electronics*, v. 30, n. 7, p. 3841–3851, July 2015. ISSN 0885-8993.

ALMEIDA, P. S. et al. Offline soft-switched led driver based on an integrated bridgeless boost–asymmetrical half-bridge converter. *IEEE Transactions on Industry Applications*, v. 51, n. 1, p. 761–769, 2015. ISSN 0093-9994.

ALMEIDA, P. S. et al. Matching led and driver life spans: A review of different techniques. *IEEE Industrial Electronics Magazine*, v. 9, n. 2, p. 36–47, 2015.

ALMEIDA, P. S. et al. Application of series resonant converters to reduce ripple transmission to led arrays in offline drivers. *Electronics Letters*, v. 49, n. 6, p. 414–415, March 2013. ISSN 0013-5194.

ALMEIDA, P. S. et al. Off-line soft-switched led driver based on an integrated bridgeless boost - half-bridge converter. In: *2013 IEEE Industry Applications Society Annual Meeting*. [S.l.: s.n.], 2013. p. 1–7. ISSN 0197-2618.

ALMEIDA, P. S. et al. An experimental study on the photometrical impacts of several current waveforms on power white leds. In: *XI Brazilian Power Electronics Conference*. [S.l.: s.n.], 2011. p. 728–733. ISSN 2165-0454.

ALMEIDA, P. S.; SOARES, G. M.; BRAGA, H. A. Storage capacitance minimization in led drivers based on photometrical constraints and converter integration. *SOBRAEP Brazilian Journal of Power Electronics*, v. 18, n. 2, p. 962–971, 2013.

ALONSO, J. M. et al. Reducing storage capacitance in off-line led power supplies by using integrated converters. In: *2012 IEEE Industry Applications Society Annual Meeting*. [S.l.: s.n.], 2012. p. 1–8.

ALWITT, R.; HILLS, R. The chemistry of failure of aluminum electrolytic capacitors. *IEEE Transactions on Parts, Materials and Packaging*, v. 1, n. 2, p. 28–34, 1965.

ARIAS, M. et al. Optimized design of a high input-voltage-ripple-rejection converter for led lighting. *IEEE Transactions on Power Electronics*, v. 33, n. 6, p. 5192–5205, 2018.

ARIAS, M. et al. Digital implementation of the feedforward loop of the asymmetrical half-bridge converter for led lighting applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 3, n. 3, p. 642–653, 2015.

ARIAS, M. et al. High-efficiency asymmetrical half-bridge converter without electrolytic capacitor for low-output-voltage ac–dc led drivers. *IEEE Transactions on Power Electronics*, v. 28, n. 5, p. 2539–2550, 2013.

ARIAS, M. et al. Design of a soft-switching asymmetrical half-bridge converter as second stage of an led driver for street lighting application. *IEEE Transactions on Power Electronics*, v. 27, n. 3, p. 1608–1621, 2012.

BARBI, I. *Eletrônica de potência: Projeto de fontes chaveadas*. [S.l.]: Ediçao do autor, 2007.

BARRUEL, F.; SCHANEN, J.; RETIERE, N. Volumetric optimization of passive filter for power electronics input stage in the more electrical aircraft. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*. [S.l.: s.n.], 2004. v. 1, p. 433–438 Vol.1.

BARTH, C. B. et al. Experimental evaluation of capacitors for power buffering in single-phase power converters. *IEEE Transactions on Power Electronics*, v. 34, n. 8, p. 7887–7899, 2019.

BEIRANVAND, R. et al. Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range llc resonant converter. *IEEE Transactions on Power Electronics*, v. 26, n. 2, p. 462–472, 2011.

BEIRANVAND, R. et al. A design procedure for optimizing the llc resonant converter as a wide output range voltage source. *IEEE Transactions on Power Electronics*, v. 27, n. 8, p. 3749–3763, 2012.

BENDER, V. C. et al. Design methodology for light-emitting diode systems by considering an electrothermal model. *IEEE Transactions on Electron Devices*, IEEE, v. 60, n. 11, p. 3799–3806, 2013.

BRAND, J. S. et al. Capacitance reduction in flicker-free integrated offline led drivers. *IEEE Transactions on Industrial Electronics*, v. 68, n. 12, p. 11992–12001, 2021.

BULLOUGH, J. D. et al. Detection and acceptability of stroboscopic effects from flicker. *Lighting Research & Technology*, Sage Publications Sage UK: London, England, v. 44, n. 4, p. 477–483, 2012.

CAMPONOGARA, D. et al. Offline led driver for street lighting with an optimized cascade structure. *IEEE Transactions on Industry Applications*, v. 49, n. 6, p. 2437–2443, 2013.

CAMPONOGARA, D. et al. Capacitance reduction with an optimized converter connection applied to led drivers. *IEEE Transactions on Industrial Electronics*, v. 62, n. 1, p. 184–192, Jan 2015. ISSN 0278-0046.

CASTRO, I. et al. A review on flicker-free ac–dc led drivers for single-phase and three-phase ac power grids. *IEEE Transactions on Power Electronics*, v. 34, n. 10, p. 10035–10057, 2019.

CENTENARO, M. et al. A survey on technologies, standards and open challenges in satellite iot. *IEEE Communications Surveys & Tutorials*, IEEE, v. 23, n. 3, p. 1693–1720, 2021.

CHANG, C.-H. et al. A novel single-stage llc resonant ac-dc converter with power factor correction feature. In: *2011 6th IEEE Conference on Industrial Electronics and Applications*. [S.l.: s.n.], 2011. p. 2191–2196.

CHCH, A. et al. High-power and high-efficiency ingan-based light emitters. *IEEE transactions on electron devices*, IEEE, v. 57, n. 1, p. 79–87, 2010.

CHEMI-CON, N. *Aluminum capacitors catalogue-Technical note on judicious use of aluminum electrolytic capacitors*. 2013. Disponível em: <http://www.chemi-con.com/2013AluminumElectrolyticCatalog.pdf>.

CHEN, H. T.; TAO, X. H.; HUI, S. Y. R. Estimation of optical power and heat-dissipation coefficient for the photo-electro-thermal theory for led systems. *IEEE Transactions on Power Electronics*, v. 27, n. 4, p. 2176–2183, April 2012. ISSN 0885-8993.

CHEN, S.-Y.; LI, Z. R.; CHEN, C.-L. Analysis and design of single-stage ac/dc *llc* resonant converter. *IEEE Transactions on Industrial Electronics*, v. 59, n. 3, p. 1538–1544, 2012.

CHENG, C.-A. et al. Design and implementation of a single-stage driver for supplying an led street-lighting module with power factor corrections. *IEEE Transactions on Power Electronics*, v. 30, n. 2, p. 956–966, 2015.

CHENG, C.-A.; CHENG, H.-L.; CHUNG, T.-Y. A novel single-stage high-power-factor led street-lighting driver with coupled inductors. *IEEE Transactions on Industry Applications*, v. 50, n. 5, p. 3037–3045, 2014.

CHENG, H.-L. et al. A novel high-power-factor ac/dc led driver with dual flyback converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 7, n. 1, p. 555–564, 2019.

CHU, C. .; LI, C. . Analysis and design of a current-fed zero-voltage-switching and zero-current-switching cl-resonant push-pull dc-dc converter. *IET Power Electronics*, v. 2, n. 4, p. 456–465, July 2009. ISSN 1755-4535.

CITTANTI, D.; VICO, E.; BOJOI, I. R. New fom-based performance evaluation of 600/650 v sic and gan semiconductors for next-generation ev drives. *IEEE Access*, v. 10, p. 51693–51707, 2022.

CRAFORD, G. Current state of the art in high brightness leds. *APS March Meetings Abstracts*, v. 1, p. 3001, 2007.

DALLA COSTA, M. A. et al. A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps. *IEEE Transactions on Industrial Electronics*, v. 55, n. 3, p. 1112–1122, 2008.

DEMING, W. E. *The new economics for industry, government, education.* [S.l.]: MIT press, 2018.

DONG, H. et al. An electrolytic capacitor-less high power factor led driver based on a "one-and-a-half stage" forward-flyback topology. *IEEE Transactions on Power Electronics*, v. 33, n. 2, p. 1572–1584, 2018.

DWELLEY, D. M. Voltage mode feedback burst mode circuit. *U. S. Patent 6307356B1*, 2001.

ERICKSON, R. W.; MAKSIMOVIC, D. *Fundamentals of power electronics.* [S.l.]: Springer Science & Business Media, 2007.

EVERTS, J. Modeling and optimization of bidirectional dual active bridge ac–dc converter topologies. *KU Leuven: Heverlee, Belgium*, 2014.

FANG, P. et al. Led driver achieves electrolytic capacitor-less and flicker-free operation with an energy buffer unit. *IEEE Transactions on Power Electronics*, v. 34, n. 7, p. 6777–6793, 2019.

FANG, X. et al. Efficiency-oriented optimal design of the llc resonant converter based on peak gain placement. *IEEE Transactions on Power Electronics*, v. 28, n. 5, p. 2285–2296, 2013.

FANG, X. et al. Operation mode analysis and peak gain approximation of the llc resonant converter. *IEEE Transactions on Power Electronics*, v. 27, n. 4, p. 1985–1995, 2012.

FANG, Z. et al. Optimal design methodology for llc resonant converter in battery charging applications based on time-weighted average efficiency. *IEEE Transactions on Power Electronics*, v. 30, n. 10, p. 5469–5483, 2015.

FANG, Z. et al. Control of an llc resonant converter using load feedback linearization. *IEEE Transactions on Power Electronics*, v. 33, n. 1, p. 887–898, 2018.

FEI, C.; LI, Q.; LEE, F. C. Digital implementation of light-load efficiency improvement for high-frequency llc converters with simplified optimal trajectory control. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 6, n. 4, p. 1850–1859, 2018.

FENG, W.; LEE, F. C.; MATTAVELLI, P. Optimal trajectory control of burst mode for llc resonant converter. *IEEE Transactions on Power Electronics*, v. 28, n. 1, p. 457–466, 2013.

FENG, W.; LEE, F. C.; MATTAVELLI, P. Optimal trajectory control of llc resonant converters for led pwm dimming. *IEEE Transactions on Power Electronics*, v. 29, n. 2, p. 979–987, 2014.

FERRAZ, R. M. *Modelagem e Projeto de um Conversor Ressonante LLC para o Acionamento de LEDs Utilizando uma Metodologia de Elevada Acurácia.* Dissertação (Mestrado em Engenharia Elétrica) — Universidade Federal de Juiz de Fora, 2019.

FERRAZ, R. M. et al. Non-linearized complete state-space model of an led driver based on the lc resonant converter. In: *2018 13th IEEE International Conference on Industry Applications (INDUSCON).* [S.l.: s.n.], 2018. p. 517–522.

FERRAZ, R. M. et al. A novel design approach for llc resonant converters in off-line led driving applications. *Journal of Control, Automation and Electrical Systems*, Springer, v. 32, p. 1758–1770, 2021.

FISHER, R. S. et al. Photic-and pattern-induced seizures: a review for the epilepsy foundation of america working group. *Epilepsia*, Wiley Online Library, v. 46, n. 9, p. 1426–1441, 2005.

FLETCHER, J. L. *Patterns of high performance: Discovering the ways people work best.* [S.l.]: Berrett-Koehler Publishers, 1995.

FRAYTAG, J. et al. A comparative performance investigation of single-stage dimmable electronic ballasts for electrodeless fluorescent lamp applications. *IEEE Transactions on Power Electronics*, v. 30, n. 4, p. 2239–2252, 2015.

GACIO, D. et al. A universal-input single-stag2e high-power-factor power supply for hb-leds based on integrated buck–flyback converter. *IEEE Transactions on Industrial Electronics*, v. 58, n. 2, p. 589–599, 2011.

GARCÍA-CHAS, R.; NEIRA-FONTELA, E.; VARELA-NEIRA, C. High-performance work systems and job satisfaction: a multilevel model. *Journal of Managerial Psychology*, Emerald Group Publishing Limited, 2016.

GARCIA, J. et al. An estimator of luminous flux for enhanced control of high brightness leds. In: IEEE. *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.* [S.l.], 2008. p. 1852–1856.

GU, L. et al. Means of eliminating electrolytic capacitor in ac/dc power supplies for led lightings. *IEEE Transactions on Power Electronics*, v. 24, n. 5, p. 1399–1408, 2009.

HARMS, J. W. Revision of mil-hdbk-217, reliability prediction of electronic equipment. In: IEEE. *2010 Proceedings-Annual Reliability and Maintainability Symposium (RAMS).* [S.l.], 2010. p. 1–3.

HE, J.; RUAN, X.; ZHANG, L. Adaptive voltage control for bidirectional converter in flicker-free electrolytic capacitor-less ac–dc led driver. *IEEE Transactions on Industrial Electronics*, v. 64, n. 1, p. 320–324, 2017.

HELDWEIN, M. L.; KOLAR, J. W. Design of minimum volume emc input filters for an ultra compact three-phase pwm rectifier. In: *Proc. 9th COBEP.* [S.l.: s.n.], 2007. p. 454–461.

HU, H. et al. A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in pv systems. *IEEE Transactions on Power Electronics*, v. 28, n. 6, p. 2711–2726, 2013.

HUANG, H. Designing an llc resonant half-bridge power converter. In: TEXAS INSTRUMENTS INCORPORATED DALLAS, TX, USA. *2010 Texas Instruments Power Supply Design Seminar, SEM1900, Topic*. [S.l.], 2010. v. 3, p. 2010–2011.

HUANG, L.-C. et al. High performance work systems, employee well-being, and job involvement: An empirical study. *Personnel Review*, Emerald Group Publishing Limited, 2016.

HUBER, L.; JANG, Y.; JOVANOVIC, M. M. Performance evaluation of bridgeless pfc boost rectifiers. *IEEE Transactions on Power Electronics*, v. 23, n. 3, p. 1381–1390, May 2008. ISSN 0885-8993.

HUI, S. Y. et al. A novel passive offline led driver with long lifetime. *IEEE Transactions on Power Electronics*, v. 25, n. 10, p. 2665–2672, Oct 2010. ISSN 0885-8993.

HUI, S. Y.; QIN, Y. X. A general photo-electro-thermal theory for light emitting diode (led) systems. *IEEE Transactions on Power Electronics*, v. 24, n. 8, p. 1967–1976, Aug 2009. ISSN 0885-8993.

HWU, K. I.; YAU, Y. T.; LEE, L.-L. Powering led using high-efficiency sr flyback converter. *IEEE Transactions on Industry Applications*, v. 47, n. 1, p. 376–386, 2011.

IEA. *Lighting, IEA, Paris*. 2021. Disponível em: <https://www.iea.org/reports/lighting>.

IEC. 61000-3-2 – limits for harmonics current emissions (equipment input current < 16 a per phase). *International Electrotechnical Commission.*, 2018.

IEEE. Recommended practices for modulating current in high-brightness leds for mitigating health risks to viewers. *IEEE Std 1789-2015*, p. 1–80, June 2015.

IVENSKY, G.; BRONSHTEIN, S.; ABRAMOVITZ, A. Approximate analysis of resonant llc dc-dc converter. *IEEE Transactions on Power Electronics*, v. 26, n. 11, p. 3274–3284, 2011.

JOVANOVIć, M. M.; IRVING, B. T. On-the-fly topology-morphing control—efficiency optimization method for <italic>llc</italic> resonant converters operating in wide input- and/or output-voltage range. *IEEE Transactions on Power Electronics*, v. 31, n. 3, p. 2596–2608, 2016.

JR, M. L. M. H. The power of great expectations. *American Journal of Health-System Pharmacy: AJHP*, Oxford University Press, v. 74, n. 16, p. 1221, 2017.

JURAN, J. M.; GRYNA, F. M. *Quality planning and analysis*. [S.l.]: McGraw-Hill, 1980.

KAZIMIERCZUK, M. K.; CZARKOWSKI, D. *Resonant power converters*. [S.l.]: John Wiley & Sons, 2012.

KEMET. *F611 Metallized Polyester Film Capacitors*. Datasheet, 2021.

KIM, B.-C.; PARK, K.-B.; MOON, G.-W. Asymmetric pwm control scheme during hold-up time for *llc* resonant converter. *IEEE Transactions on Industrial Electronics*, v. 59, n. 7, p. 2992–2997, 2012.

Kim, J. et al. Analysis and design of boost-llc converter for high power density ac-dc adapter. In: *2013 IEEE ECCE Asia Downunder*. [S.l.: s.n.], 2013. p. 6–11.

KIM, J.-H. et al. Analysis on load-adaptive phase-shift control for high efficiency full-bridge llc resonant converter under light-load conditions. *IEEE Transactions on Power Electronics*, v. 31, n. 7, p. 4942–4955, 2016.

KIM, J.-W.; MOON, J.-P.; MOON, G.-W. Duty-ratio-control-aided llc converter for current balancing of two-channel led driver. *IEEE Transactions on Industrial Electronics*, v. 64, n. 2, p. 1178–1184, 2017.

KOLAR, J. W. Multi-objective optimization of power electronics converter systems. In: NATIONAL SCIENCE FOUNDATION. *NSF Workshop on Directions in Power Electronics Research*. [S.l.], 2016.

KOLAR, J. W. et al. Performance trends and limitations of power electronic systems. In: *2010 6th International Conference on Integrated Power Electronics Systems*. [S.l.: s.n.], 2010. p. 1–20.

LAFITTE, B.; GARCIA, S. *Green Public Procurement Technical Guidelines and Specifications for Energy Efficient Lighting*. 2021. Disponível em: <https://united4efficiency.org/resources/lighting-sustainable-public-procurement-webinar/>.

LAI, C.; SHYU, K. A single-stage ac/dc converter based on zero voltage switching llc resonant topology. *IET electric power applications*, IET, v. 1, n. 5, p. 743–752, 2007.

LAMAR, D. G. et al. Active input current shaper without an electrolytic capacitor for retrofit lamps applications. *IEEE Transactions on Power Electronics*, v. 32, n. 5, p. 3908–3919, 2017.

LAMAR, D. G. et al. On the limit of the output capacitor reduction in power-factor correctors by distorting the line input current. *IEEE Transactions on Power Electronics*, v. 27, n. 3, p. 1168–1176, 2012.

LAMAR, D. G. et al. A very simple control strategy for power factor correctors driving high-brightness leds. *IEEE Transactions on Power Electronics*, v. 24, n. 8, p. 2032–2042, 2009.

LAZAR, J. F.; MARTINELLI, R. Steady-state analysis of the llc series resonant converter. In: *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*. [S.l.: s.n.], 2001. v. 2, p. 728–735 vol.2.

LEE, E. S. et al. Temperature-robust lc3 passive led drivers with low thd, high efficiency and pf, and long life. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 3, n. 3, p. 829–840, Sept 2015. ISSN 2168-6777.

LEHMAN, B. et al. Proposing measures of flicker in the low frequencies for lighting applications. In: *2011 IEEE Energy Conversion Congress and Exposition*. [S.l.: s.n.], 2011. p. 2865–2872. ISSN 2329-3721.

LEHMAN, B.; WILKINS, A. J. Designing to mitigate effects of flicker in led lighting: Reducing risks to health and safety. *IEEE Power Electronics Magazine*, v. 1, n. 3, p. 18–26, 2014.

LEVY, D. Introduction to numerical analysis. *Department of Mathematics and Center for Scientific Computation and Mathematical Modeling (CSCAMM) University of Maryland*, 2010.

LI, S. et al. A survey, classification, and critical review of light-emitting diode drivers. *IEEE Transactions on Power Electronics*, v. 31, n. 2, p. 1503–1516, Feb 2016. ISSN 0885-8993.

LI, Y.-C.; CHEN, C.-L. A novel single-stage high-power-factor ac-to-dc led driving circuit with leakage inductance energy recycling. *IEEE Transactions on Industrial Electronics*, v. 59, n. 2, p. 793–802, 2012.

LIDOW, A. et al. *GaN transistors for efficient power conversion*. [S.l.]: John Wiley & Sons, 2019.

LIU, J. et al. A modified gain model and the corresponding design method for an llc resonant converter. *IEEE Transactions on Power Electronics*, v. 32, n. 9, p. 6716–6727, 2017.

LUO, H. et al. A digital pulse train controlled high power factor dcm boost pfc converter over a universal input voltage range. *IEEE Transactions on Industrial Electronics*, v. 66, n. 4, p. 2814–2824, 2019.

LUZ, P. et al. Resonant control applied to bus capacitance reduction in integrated double buck-boost to led driver. *Eletrônica de Potência*, v. 23, n. 1, p. 98–107, 2018.

MA, H. et al. A single-stage pfm-apwm hybrid modulated soft-switched converter with low bus voltage for high-power led lighting applications. *IEEE Transactions on Industrial Electronics*, v. 64, n. 7, p. 5777–5788, 2017.

MA, H. et al. A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power ac–dc driver for supplying multiple led strings in parallel. *IEEE Transactions on Power Electronics*, v. 31, n. 8, p. 5825–5836, 2016.

MA, H. et al. A single-stage integrated boost-llc ac–dc converter with quasi-constant bus voltage for multichannel led street-lighting applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 6, n. 3, p. 1143–1153, 2018.

MA, J. et al. Led driver based on boost circuit and llc converter. *IEEE Access*, v. 6, p. 49588–49600, 2018.

MELO, M. F. de et al. Analysis of low-frequency current ripple transmission in series-resonant led drivers. *Electronics Letters*, v. 51, n. 9, p. 716–717, 2015. ISSN 0013-5194.

MELO, M. F. de et al. Analysis of series-resonant led driver applied to reduce the low-frequency current ripple transmission. In: *2015 IEEE 24th International Symposium on Industrial Electronics (ISIE)*. [S.l.: s.n.], 2015. p. 1166–1171. ISSN 2163-5145.

MELO, M. F. de et al. Self-oscillating series-resonant led driver applied to reduce low-frequency current ripple transmission. In: *2015 IEEE Industry Applications Society Annual Meeting*. [S.l.: s.n.], 2015. p. 1–7.

MENKE, M. F. *Contribuições para a modelagem, analise, projeto e controle do conversor ressonante LLC driver de LED*. Tese (Doutorado em Engenharia Elétrica) — Universidade Federal de Santa Maria, 2021.

MENKE, M. F. et al. Analysis and design of the llc led driver based on state-space representation direct time-domain solution. *IEEE Transactions on Power Electronics*, v. 35, n. 12, p. 12686–12701, 2020.

MUMTAHINA, U.; WOLFS, P. J. Multimode optimization of the phase-shifted llc series resonant converter. *IEEE Transactions on Power Electronics*, v. 33, n. 12, p. 10478–10489, 2018.

MäRZ, M. et al. Power electronics system integration for electric and hybrid vehicles. In: *2010 6th International Conference on Integrated Power Electronics Systems*. [S.l.: s.n.], 2010. p. 1–10.

NICHICON. *Nichicon LGN Aluminum Electrolytic Capacitors*. Datasheet, 2011.

NICHICON. *UCY Aluminum Electrolytic Capacitors*. Datasheet, 2011.

PARLER, S. G.; DUBILIER, P. Deriving life multipliers for electrolytic capacitors. *IEEE Power Electronics Society Newsletter*, v. 16, n. 1, p. 11–12, 2004.

PAULA, W. J. de et al. An extensive comparative study of switching losses prediction in power mosfets. In: *2018 13th IEEE International Conference on Industry Applications (INDUSCON)*. [S.l.: s.n.], 2018. p. 105–111.

PELLETIER, P. et al. Optimization of a dc capacitor tank. *IEEE Transactions on Industry Applications*, v. 45, n. 2, p. 880–886, 2009.

PERVAIZ, S.; KUMAR, A.; AFRIDI, K. K. A compact electrolytic-free two-stage universal input offline led driver with volume-optimized ssc energy buffer. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 6, n. 3, p. 1116–1130, 2018.

POWER, E. N. Capacitors age and capacitors have an end of life. *White paper*, 2008.

QU, X.; WONG, S. C.; TSE, C. K. An improved lclc current-source-output multistring led driver with capacitive current balancing. *IEEE Transactions on Power Electronics*, v. 30, n. 10, p. 5783–5791, Oct 2015. ISSN 0885-8993.

RAGGL, K.; NUSSBAUMER, T.; KOLAR, J. W. Guideline for a simplified differential-mode emi filter design. *IEEE Transactions on Industrial Electronics*, IEEE, v. 57, n. 3, p. 1031–1040, 2010.

RASHIDI, N. et al. Multi-objective design and optimization of power electronics converters with uncertainty quantification—part i: Parametric uncertainty. *IEEE Transactions on Power Electronics*, v. 36, n. 2, p. 1463–1474, 2021.

RODRIGUES, C. R. B. S. et al. Experimental characterization regarding two types of phosphor-converted white high-brightness leds: Low power and high power devices. In: *XI Brazilian Power Electronics Conference*. [S.l.: s.n.], 2011. p. 734–740. ISSN 2165-0454.

RUAN, X. et al. Optimum injected current harmonics to minimize peak-to-average ratio of led current for electrolytic capacitor-less ac–dc drivers. *IEEE Transactions on Power Electronics*, v. 26, n. 7, p. 1820–1825, 2011.

RYAN, M. J. et al. A new zvs lcl-resonant push-pull dc-dc converter topology. *IEEE Transactions on Industry Applications*, v. 34, n. 5, p. 1164–1174, Sep. 1998. ISSN 0093-9994.

SAMSUNG SEMICONDUCTOR, INC. *Middle Power LED Series 3030*. Datasheet, 2022.

SANTIAGO-GONZALEZ, J. A. et al. Single phase universal input pfc converter operating at hf. In: *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. [S.l.: s.n.], 2018. p. 2062–2069.

SCHECHNER, R. *Performance studies: An introduction*. [S.l.]: Routledge, 2020.

SCHUBERT, E. F.; GESSMANN, T.; KIM, J. K. *Light emitting diodes*. [S.l.]: Wiley Online Library, 2005.

SEMICONDUCTOR, F. Led application design guide using half-bridge llc resonant converter for 100w street lighting. *AN-9729, Fairchild Semiconductor Corporation, Rev*, v. 1, n. 0, 2012.

SFAKIANAKIS, G. E.; EVERTS, J.; LOMONOVA, E. A. Overview of the requirements and implementations of bidirectional isolated ac-dc converters for automotive battery charging applications. In: *2015 Tenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*. [S.l.: s.n.], 2015. p. 1–12.

SHAN, Z. et al. Ac–dc led driver with an additional active rectifier and a unidirectional auxiliary circuit for ac power ripple isolation. *IEEE Transactions on Power Electronics*, v. 34, n. 1, p. 685–699, 2019.

SHARMA, S. et al. Advantages of sic-based devices on the design of dual-active bridge dc/dc converter for dc faults. In: *2022 IEEE 9th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. [S.l.: s.n.], 2022. p. 159–163.

SICHIROLLO, F.; BUSO, S.; SPIAZZI, G. A high efficiency and high power factor offline converter for solid state street lighting applications. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. [S.l.: s.n.], 2012. p. 1188–1195. ISSN 2329-3721.

SIMONE, S. D. et al. Design-oriented steady-state analysis of llc resonant converters based on fha. In: *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.* [S.l.: s.n.], 2006. p. 200–207.

SOARES, G. M. *Sistema inteligente de iluminação de estado sólido com controle remoto e análise de parâmetros da rede elétrica*. Dissertação (Mestrado em Engenharia Elétrica) — Universidade Federal de Juiz de Fora, 2014.

SOARES, G. M. *Capacitance reduction in off-line LED drivers by using active ripple compensation techniques*. Tese (Doutorado em Engenharia Elétrica) — Universidade Federal de Juiz de Fora, 2017.

SOARES, G. M. et al. Capacitance minimization in offline led drivers using an active-ripple-compensation technique. *IEEE Transactions on Power Electronics*, v. 32, n. 4, p. 3022–3033, 2017.

SOARES, G. M. et al. Optimized design of a wide-bandwidth controller for low-frequency ripple compensation in offline led drivers. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 6, n. 3, p. 1166–1178, 2018.

Soares, G. M.; Alonso, J. M.; Braga, H. A. C. Investigation of the active ripple compensation technique to reduce bulk capacitance in offline flyback-based led drivers. *IEEE Transactions on Power Electronics*, v. 33, n. 6, p. 5206–5214, 2018.

SOMNUSDE. *Countries of the world, coloured according to their nominal power net voltage and frequency*. 2009. Disponível em: <https://commons.wikimedia.org/wiki/File:World_Map_of_Mains_Voltages_and_Frequencies,_Detailed.svg>.

SONG, Y.; WANG, B. Survey on reliability of power electronic systems. *IEEE transactions on power electronics*, IEEE, v. 28, n. 1, p. 591–604, 2012.

SUN, C.-C. et al. Packaging efficiency in phosphor-converted white leds and its impact to the limit of luminous efficacy. *Journal of Solid State Lighting*, Springer, v. 1, n. 1, p. 19, 2014.

SUN, Q. et al. Reliability assessment of metallized film capacitors using reduced degradation test sample. *Quality and Reliability Engineering International*, Wiley Online Library, v. 29, n. 2, p. 259–265, 2013.

THORNTON. *product catalog Thornton*. Datasheet, 2015. Disponível em: <https://www.thornton.com.br/pdf/CATALOG%20THORNTON_ing.pdf>.

TORRES, L. F.; MARTINS, M. d. C. F. High performance no brasil: uma revisão sistemática. *Revista Administração em Diálogo-RAD*, v. 23, n. 2, p. 57–77, 2021.

TUCKMAN, B. W. Developmental sequence in small groups. *Psychological bulletin*, American Psychological Association, v. 63, n. 6, p. 384, 1965.

VALIPOUR, H.; REZAZADEH, G.; ZOLGHADRI, M. R. Flicker-free electrolytic capacitor-less universal input offline led driver with pfc. *IEEE Transactions on Power Electronics*, v. 31, n. 9, p. 6553–6561, 2016.

VISHAY. *MKP1848C Metallized Polypropylene DC-Link Film Capacitor*. Datasheet, 2022. Disponível em: <https://www.vishay.com/docs/26015/mkp1848cdclink.pdf>.

WANG, B. et al. A method of reducing the peak-to-average ratio of led current for electrolytic capacitor-less ac–dc drivers. *IEEE Transactions on Power Electronics*, v. 25, n. 3, p. 592–601, 2010.

WANG, H.; BLAABJERG, F. Reliability of capacitors for dc-link applications in power electronic converters—an overview. *IEEE Transactions on Industry Applications*, v. 50, n. 5, p. 3569–3578, 2014.

WANG, H.; CHUNG, H. S.-H.; LIU, W. Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system. *IEEE Transactions on Power Electronics*, v. 29, n. 3, p. 1163–1175, 2014.

WANG, H. et al. Lifetime estimation of dc-link capacitors in adjustable speed drives under grid voltage unbalances. *IEEE Transactions on Power Electronics*, v. 34, n. 5, p. 4064–4078, 2019.

WANG, H.; LISERRE, M.; BLAABJERG, F. Toward reliable power electronics: Challenges, design tools, and opportunities. *IEEE Industrial Electronics Magazine*, v. 7, n. 2, p. 17–26, 2013.

WANG, H. et al. An overview of capacitive dc-links-topology derivation and scalability analysis. *IEEE Transactions on Power Electronics*, v. 35, n. 2, p. 1805–1829, 2020.

WANG, S. et al. A flicker-free electrolytic capacitor-less ac–dc led driver. *IEEE Transactions on Power Electronics*, v. 27, n. 11, p. 4540–4548, 2012.

WANG, Y. et al. Single-stage bridgeless led driver based on a clcl resonant converter. *IEEE Transactions on Industry Applications*, v. 54, n. 2, p. 1832–1841, 2018.

WANG, Y. et al. A single-stage led driver based on interleaved buck–boost circuit and llc resonant converter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 3, n. 3, p. 732–741, 2015.

WANG, Y. et al. A single-stage led driver based on bcm boost circuit and *llc* converter for street lighting system. *IEEE Transactions on Industrial Electronics*, v. 62, n. 9, p. 5446–5457, 2015.

WANG, Y. et al. A CLCL resonant dc/dc converter for two-stage led driver system. *IEEE Transactions on Industrial Electronics*, v. 63, n. 5, p. 2883–2891, May 2016. ISSN 0278-0046.

WANG, Y. et al. A clcl resonant dc/dc converter for two-stage led driver system. *IEEE Transactions on Industrial Electronics*, v. 63, n. 5, p. 2883–2891, 2016.

WANG, Y. et al. Single-stage led driver with low bus voltage. *Electronics letters*, IET, v. 49, n. 7, p. 455–457, 2013.

WANG, Y. et al. A single-stage led driver based on half-bridge *clcl* resonant converter and buck–boost circuit. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 7, n. 1, p. 196–208, 2019.

WANG, Y. et al. A single-stage led driver based on sepic and llc circuits. *IEEE Transactions on Industrial Electronics*, v. 64, n. 7, p. 5766–5776, 2017.

WANG, Y. et al. Safety performance boundary identification of highly automated vehicles: A surrogate model-based gradient descent searching approach. *IEEE Transactions on Intelligent Transportation Systems*, v. 23, n. 12, p. 23809–23820, 2022.

WEI, H.; BATARSEH, I. Comparison of basic converter topologies for power factor correction. In: *Proceedings IEEE Southeastcon '98 'Engineering for a New Era'*. [S.l.: s.n.], 1998. p. 348–353.

WEI, Y. et al. A magnetically controlled single-stage ac–dc converter. *IEEE Transactions on Power Electronics*, v. 35, n. 9, p. 8872–8877, 2020.

WEI, Y. et al. Analysis and design of the llc resonant converter with variable inductor control based on time-domain analysis. *IEEE Transactions on Industrial Electronics*, v. 67, n. 7, p. 5432–5443, 2020.

WEI, Y.; LUO, Q.; MANTOOTH, A. Comprehensive analysis and design of llc resonant converter with magnetic control. *CPSS Transactions on Power Electronics and Applications*, v. 4, n. 4, p. 265–275, 2019.

WEI, Y. et al. Design of a single stage llc converter based on power loss model. In: *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*. [S.l.: s.n.], 2020. p. 1832–1837.

WONG, C. S. et al. An alternative approach to led driver design based on high-voltage driving. *IEEE Transactions on Power Electronics*, v. 31, n. 3, p. 2465–2475, 2016.

WU, T.-F.; CHEN, Y.-K. Modeling of single-stage converters with high power factor and fast regulation. *IEEE Transactions on Industrial Electronics*, v. 46, n. 3, p. 585–593, 1999.

XIAO, Z. et al. Optimization of llc resonant converter with two degrees of freedom based on operation stage trajectory analysis. *IEEE Access*, v. 9, p. 79629–79642, 2021.

XIE, X. et al. Analysis and optimization of llc resonant converter with a novel over-current protection circuit. *IEEE Transactions on Power Electronics*, v. 22, n. 2, p. 435–443, 2007.

YAN, B. et al. Can junction temperature alone characterize thermal performance of white led emitters? *IEEE photonics technology letters*, IEEE, v. 23, n. 9, p. 555–557, 2011.

YANG, D. et al. A variable duty cycle soft startup strategy for llc series resonant converter based on optimal current-limiting curve. *IEEE Transactions on Power Electronics*, v. 31, n. 11, p. 7996–8006, 2016.

YANG, Y. et al. Feed-forward scheme for an electrolytic capacitor-less ac/dc led driver to reduce output current ripple. *IEEE Transactions on Power Electronics*, v. 29, n. 10, p. 5508–5517, 2014.

YI, J. et al. A novel hybrid pfm/iapwm control strategy and optimal design for single-stage interleaved boost-llc ac–dc converter with quasi-constant bus voltage. *IEEE Transactions on Industrial Electronics*, v. 68, n. 9, p. 8116–8127, 2021.

YU, W. et al. High-efficiency dc?dc converter with twin bus for dimmable led lighting. *IEEE Transactions on Power Electronics*, v. 26, n. 8, p. 2095–2100, Aug 2011. ISSN 0885-8993.

ZAWAWI, N. A.; IQBAL, S.; JAMIL, M. K. M. A single-stage power factor corrected led driver with dual half-wave rectifier. In: *2016 IEEE Industrial Electronics and Applications Conference (IEACon)*. [S.l.: s.n.], 2016. p. 12–19.

ZENG, J. et al. Llc resonant converter topologies and industrial applications — a review. *Chinese Journal of Electrical Engineering*, v. 6, n. 3, p. 73–84, 2020.

ZHANG, G. et al. Control design and performance analysis of a double-switched llc resonant rectifier for unity power factor and soft-switching. *IEEE Access*, v. 8, p. 44511–44521, 2020.

ZHANG, J.; JIANG, T.; WU, X. A high-efficiency quasi-two-stage led driver with multichannel outputs. *IEEE Transactions on Industrial Electronics*, v. 64, n. 7, p. 5875–5882, 2017.

ZHANG, X.; SPENCER, J. W. Analysis of boost PFC converters operating in the discontinuous conduction mode. *IEEE Transactions on Power Electronics*, v. 26, n. 12, p. 3621–3628, 2011.

ZHAO, J. et al. State trajectory control of burst mode for lcc resonant converters with capacitive output filter. *IEEE Transactions on Power Electronics*, v. 37, n. 1, p. 377–391, 2022.

APPENDIX A – SUPPLEMENTARY MATERIAL OF CHAPTER 4

The content of the C-block used in the simulation of the integrated converters with frequency-based ARC is presented in sections A.1 and A.2

A.1 VARIABLE/FUNCTIONS DEFINITIONS OF THE C-BLOCK

```
#include <Stdlib.h>
#include <String.h>
#include <Math.h>

int g_nInputNodes=0;
int g_nOutputNodes=0;
int g_nStepCount=0;

float T_simul = 1E-008;
float fs, fo, f2;
float Ts;
int cont = 0;
int n ;
float pi = 3.1415;
```

A.2 IMPLEMENTATION OF THE C-BLOCK

```
g_nStepCount++;

// control variable
fs = in[0];

Ts = 1/fs; n = Ts/T_simul;
if(cont < n/2)
{
 out[0] =1;
 out[1] = 0;
 cont++;
}
if(cont >= n/2)
{
 out[0]=0;
 out[1]=1;
 cont++;
if(cont>=n){cont=0;}
}
```

APPENDIX B – SUPPLEMENTARY MATERIAL OF CHAPTER 6

This appendix presents the set of MATLAB scripts that were implemented to design the high-performance LED driver from a constrained multi-objective optimization problem.

B.1 MAIN CODE WITH THE OPTIMIZATION ALGORITHM

```
clc; clear all; close all; format long

%% design parameters
VG_nom = 127;
D = 0.5;
fL = 60;
% LEDs
nLEDs = 48;
Vt = nLEDs*2.7; rd = nLEDs*0.25;
Io_design = 0.7;
deltaIo_max = 0.10*Io_design; % Maximum LF LEDs current ripple
dello_HF = 0.02; % High frequency LEDs current ripple
Ro_design = rd + Vt/Io_design;
Vo_design = Vt + rd*Io_design;
Po_design = Io_design*Vo_design;

% initial efficiency estimation
eff_pfc = 0.95; eff_pc = 0.97;

fr = 100000;
VB_max = 500;
VB_nom = 450;
f_range = 0.5;
fmin = fr*(1-f_range);

%% Selecting semiconductors
% Half-bridge switches 2 x IRFP460 (500V / 0.27Ohm)
R_on = 0.27; tr=59e-9;  tf=58e-9;
% Boost diodes
% 2 x MURS360 (600V / 3A)
V_F = 1.05; % (iF = 3.0 A, TJ = 150 C)
R_D = (0.83-0.81)/(1-0.8); % 1A, Tj=100 C

% output rectifier diodes
% 2 x MUR820 (200V / 8A)
V_Frec = 0.975; R_Drec = (0.712-0.7)/(1-0.9);

% Possible values for the bus capacitance (e_ucy-1511878)
```

```
39 CB_poss = [10 18 22 27 33 47 100 180 220 240 330]*10^(-6);
40 % Capacitance Tolerance: +/- 20% at 120Hz, 20 C
41 tol_CB = 0.2;
42
43 v_design=[VG_nom fL Vt rd Io_design deltaIo_max delIo_HF Ro_design
       Vo_design Po_design eff_pfc eff_pc fr VB_max VB_nom D f_range fmin
       ];
44 var_semi=[R_on tr tf V_F R_D V_Frec R_Drec];
45
46 %% Set initial guess values for optimization
47 CB_ini = CB_poss(end)*(1-tol_CB); %[F]
48 Q_ini =0.8;
49 lamb_ini = 0.167;
50 fnorm_ini = 1;
51
52 % load guess values into array
53 x = [CB_ini Q_ini lamb_ini fnorm_ini];
54
55 % vector with lower bounds
56 lb = [5.6e-6 0.08 0.00167 0.5];
57 % vector with upper bounds
58 ub = [470e-6 8 16.7 1.5];
59
60 %% weights of the objective function
61 % obj = weights(1)*Volume + weights(2)*P_loss + weights(3)*FIT +
       weights(4)*Cost;
62 W1 = 1;       % 1 cm3
63 W2 = 10;      % 10 W
64 W3 = 2.5e+03;% 2500 Failures/10^6 hours
65 W4 = 0;
66 weights = [W1 W2 W3 W4];
67
68 %% Optimization options
69 FunctionTolerance = 5e-0;
70 MaxIterations = 100;
71 MaxInfeasiblePoints = 100;
72
73 % step size or learning rate
74 alfa = [2e-10 13.0e-4 13.0e-5 1.5e-4];
75
76  %% auxiliary variables
77 Const = zeros(9,1);
78 gradient = zeros(1,4);
79 dx = 1.05; % dx of the partial derivatives
80
81 cont=0;fes=1;infes=1; x_ant = x;
82 iter = 0; error = 1000; flagFeasible=1; contInfeasible=0;
```

```
83  iter_vet = zeros(length(MaxIterations)+1,1);
84  fval_vet = zeros(length(MaxIterations)+1,1);
85  CB_vet = zeros(length(MaxIterations)+1,1);
86  kf_vet = zeros(length(MaxIterations)+1,1); kf = kf_vet(1);
87  Q_vet = zeros(length(MaxIterations)+1,1);
88  lamb_vet = zeros(length(MaxIterations)+1,1);
89  IsRMS_vet = zeros(length(MaxIterations)+1,1);
90  Is_pk_vet = zeros(length(MaxIterations)+1,1);
91  fo_vet = zeros(length(MaxIterations)+1,1);
92  fn_design_vet = zeros(length(MaxIterations)+1,1);
93  Volume_vet = zeros(length(MaxIterations)+1,1);
94  Vol_disc_vet = zeros(length(MaxIterations)+1,1);
95  P_loss_vet = zeros(length(MaxIterations)+1,1);
96  FIT_vet = zeros(length(MaxIterations)+1,1);
97  eff_vet = zeros(length(MaxIterations)+1,1);
98  rho_vet = zeros(length(MaxIterations)+1,1);
99  THD_vet = zeros(length(MaxIterations)+1,1);
100
101 attempt_infes = zeros(length(MaxInfeasiblePoints),1);
102 fval_infes = zeros(length(MaxInfeasiblePoints),1);
103 CB_vet_infes = zeros(length(MaxInfeasiblePoints),1);
104 Q_vet_infes = zeros(length(MaxInfeasiblePoints),1);
105 lamb_vet_infes = zeros(length(MaxInfeasiblePoints),1);
106 kf_vet_infes = zeros(length(MaxInfeasiblePoints),1);
107 IsRMS_vet_infes = zeros(length(MaxInfeasiblePoints),1);
108 Is_pk_vet_infes = zeros(length(MaxInfeasiblePoints),1);
109 fo_vet_infes = zeros(length(MaxInfeasiblePoints),1);
110 fn_design_vet_infes = zeros(length(MaxInfeasiblePoints),1);
111 Volume_vet_infes = zeros(length(MaxInfeasiblePoints),1);
112 Vol_disc_vet_infes = zeros(length(MaxInfeasiblePoints),1);
113 P_loss_vet_infes = zeros(length(MaxInfeasiblePoints),1);
114 FIT_vet_infes = zeros(length(MaxInfeasiblePoints),1);
115 eff_vet_infes = zeros(length(MaxInfeasiblePoints),1);
116 rho_vet_infes = zeros(length(MaxInfeasiblePoints),1);
117 THD_vet_infes = zeros(length(MaxInfeasiblePoints),1);
118
119 % initial frequency
120 f0acc = ceil(x(4)*fr/100)*100; % 100Hz precision
121
122 %% Call solver to minimize the objective function given the
       constraints
123 while  max(abs(error)) > FunctionTolerance
124     if iter == 0
125         [fval_ant,perf_save,var_save,~,~] = objective(x, kf, v_design,
              var_semi,weights,f0acc);
126         f0acc = var_save(1);
127         % saving data for plot
```

```
128         fval_vet(1) = fval_ant; CB_vet(1)=x(1);Q_vet(1)=x(2);lamb_vet
                (1)=x(3);fn_design_vet(1)=x(4);fo_vet(1)=var_save(1);
                kf_vet(1)=kf;
129         IsRMS_vet(1)=var_save(7); Volume_vet(1)=var_save(3);
                Vol_disc_vet(1)=var_save(4);P_loss_vet(1)=var_save(5);
                Is_pk_vet(1)=var_save(17);
130         FIT_vet(1)=perf_save(1); eff_vet(1)=perf_save(2); rho_vet(1)=
                perf_save(3); THD_vet=perf_save(4);
131
132         save('data0');
133
134         % Displaying the Benchmark converter
135         printConverter(x,Const,v_design, kf_vet,fo_vet,Is_pk_vet,
                var_save,CB_vet,tol_CB,CB_poss,'Benchmark');
136     else
137         fval_ant = fval;
138     end
139
140     if flagFeasible ==1
141             parfor j = 1:4
142                 x_temp = x;
143                 x_temp(j) = x(j) * dx;
144                 f0acc_temp = [f0acc f0acc f0acc ceil(x_temp(4)*fr/100)
                        *100];
145                 [fval, ~, ~, ~,~] = objective(x_temp, kf, v_design,
                        var_semi,weights,f0acc_temp(j));
146                 gradient(j) = (fval - fval_ant) / ((dx - 1) * x(j));
147             end
148              % File name based on attempts
149             nome_arquivo = sprintf('gradient_%d_.mat', iter);
150             save(nome_arquivo, 'gradient');
151     else
152         % penalizing alpha
153         alfa = alfa*0.8;
154     end
155
156     x_ant = x;
157     x = x_ant - alfa.*gradient; % Gradient Descent
158
159     % cheking negative values
160     if any(x < 0)
161         while any(x < 0)
162             i_neg = x < 0;
163             gradient(i_neg) = gradient(i_neg)*0.5;
164             x = x_ant - alfa.*gradient;
165         end
166     end
```

```
167
168     % checking the bounds
169     x = checkBounds(x, lb, ub)
170
171     if iter == 0
172         f0acc = ceil(x(4)*fr/100)*100;
173     end
174     [fval,perf_save,var_save,flag,Const] = objective(x, kf,v_design,
            var_semi,weights,f0acc);
175     f0acc = var_save(1);
176
177     % setting the frequency modulation
178     kf_ant = kf;
179     if Const(1)>0
180         if x(1) <= 20.5e-6
181             flag = 0;
182         else
183             [fval,perf_save,var_save,flag,Const] = setModulation(x,
                    kf_ant,v_design,var_semi,weights,f0acc);
184             f0acc = var_save(1);
185             kf = var_save(2);
186         end
187     end
188
189     % checking if the point is feasible
190     col = find(Const > 0);
191     if  isempty(col) == 1 && flag == 1
192         flagFeasible = 1; % feasible point
193     else % infeasible point
194         disp('Infeasible point found');
195         % saving data for plot
196          attempt_infes(infes)= cont; fval_infes(infes)= fval;
                CB_vet_infes(infes)=x(1);Q_vet_infes(infes)=x(2);
                lamb_vet_infes(infes)=x(3);fn_design_vet_infes(infes)=x
                (4);kf_vet_infes(infes)=kf; Is_pk_vet_infes(infes)=
                var_save(17);
197         IsRMS_vet_infes(infes)=var_save(7); Volume_vet_infes(infes)=
                var_save(3);Vol_disc_vet_infes(infes)=var_save(4);
                P_loss_vet_infes(infes)=var_save(5); fo_vet_infes(infes)=
                var_save(1);
198         FIT_vet_infes(infes)=perf_save(1); eff_vet_infes(infes)=
                perf_save(2); rho_vet_infes(infes)=perf_save(3);
                THD_vet_infes(infes)=perf_save(4);
199
200         infes = infes + 1;
201         x = x_ant;
202         fval = fval_ant;
```

```
203         kf = kf_ant;
204
205         flagFeasible = 0;
206         contInfeasible = contInfeasible + 1;
207         if contInfeasible > MaxInfeasiblePoints
208             flagFeasible = 1;
209             disp('Routine terminated because the maximum number of
                    attempts was achieved');
210             break;
211         end
212     end
213
214     % checking a decrease of f(x)
215     if flagFeasible == 1 && fval > fval_ant
216         x = x_ant;
217         fval = fval_ant;
218         kf = kf_ant;
219
220         flagFeasible = 0;
221     end
222
223     if flagFeasible == 1
224         error = fval - fval_ant;
225         iter = iter + 1;
226         % saving data for plot
227         fval_vet(iter+1) = fval; CB_vet(iter+1)=x(1);Q_vet(iter+1)=x
                (2);lamb_vet(iter+1) = x(3); fn_design_vet(iter+1)=x(4);
                kf_vet(iter+1)=kf;fo_vet(iter+1)=var_save(1);
228         IsRMS_vet(iter+1)=var_save(7); Volume_vet(iter+1)=var_save(3);
                Vol_disc_vet(iter+1)=var_save(4);P_loss_vet(iter+1)=
                var_save(5); Is_pk_vet(iter+1)=var_save(17);
229         FIT_vet(iter+1)=perf_save(1); eff_vet(iter+1)=perf_save(2);
                rho_vet(iter+1)=perf_save(3); THD_vet(iter+1)=perf_save(4)
                ;
230
231         if iter > MaxIterations
232             disp('The maximum number of iterations has been achieved')
                    ;
233             break
234         end
235     end
236     cont = cont+1;
237     % File name based on attempts
238     nome_arquivo = sprintf('data_%d_.mat', cont);
239     vars = evalin('base', 'who');
240     save(nome_arquivo, vars{:});
241
```

```
242     if max(abs(error)) < FunctionTolerance
243         disp('Possible local minimum has been found');
244     end
245 end
246
247 % Displaying the Optimized Converter
248 printConverter(x,Const,v_design, kf_vet,fo_vet,Is_pk_vet,var_save,
      CB_vet,tol_CB,CB_poss,'Optimized');
```

B.1.1 Objective Function for Optimization

```
1  % Define objective function for optimization
2  function [obj,perf_save,var_save,flag,Const] = objective(x, kf,
       v_design,var_semi,weights,f0acc)
3
4      VG_nom=v_design(1);fL=v_design(2);Vt=v_design(3);rd=v_design(4);
           Io_design=v_design(5);deltaIo_max=v_design(6);
5      delIo_HF=v_design(7);Ro_design=v_design(8);Vo_design=v_design(9);
           Po_design=v_design(10); eff_pfc=v_design(11);
6      eff_pc=v_design(12);fr=v_design(13);VB_max=v_design(14);VB_nom=
           v_design(15);D=v_design(16);f_range=v_design(17);
7      fmin=v_design(18);
8      var_nom = [VG_nom fL VB_nom Po_design fr rd Io_design delIo_HF
           Ro_design Vo_design eff_pfc*eff_pc];
9
10     % auxiliary variables
11     flagDCM=0; flag_nom = 0; flag = 0;
12     CB = x(1);
13
14     % designs the passive elements of the converter
15     [Lb, Ls, Cs, Lm, n, Co] = designConverter(x,kf,var_nom);
16     Vo_Co = Vo_design;
17     v1 = [Ls Lm n Cs Co Vo_Co];
18
19     fo = f0acc;
20     VB_ini=VB_nom;
21     v2 = [CB, kf, fo, Lb, D, fL, VG_nom, Vt, rd, eff_pfc, eff_pc,
           VB_ini, fr,Io_design];
22     [fs,flag_nom,cont_n, time,io,ig,Is,vB,iCB,Is_pk,I_SW_off]=
           setControlVariable(v1,v2,'frequency');
23
24     % evaluate the converter
25     [deltaIo,PF,THD,harm,vBmax,var,flagDCM]=evaluateConverter(time,io,
           ig,Is,I_SW_off,vB,iCB,VG_nom,fL,D,fs,kf,Lb,n,var_nom);
26     I1=harm(1); I3=harm(2); I5=harm(3); I7=harm(4); I9=harm(5); I11=
           harm(6);
27
```

```
28      % building the constraint matrix (Power quality)
29      Const = [deltaIo - deltaIo_max
30                   -PF+0.92
31                    I3 -0.3*PF*I1
32                    I5 -0.1*I1
33                    I7 -0.07*I1
34                    I9 -0.05*I1
35                    I11 -0.03*I1
36                    vBmax-VB_max
37                    -(1-kf)*fr+fmin];
38
39      if flagDCM==1 && flag_nom == 1
40          flag = 1;
41      end
42
43      % estimate volume of passive elements
44      [Volume, Vol_disc, B_vet, Ve_vet, Rdc_vet, Rdc_sec] = calcVolume(var,
            Is_pk, Ls,(1-kf)*fs, Lm, n, Cs, Co, x(1), Lb, 'no');
45
46      % Power Density
47      rho = Po_design/Vol_disc; % [W/cm^3]
48
49      % power losses
50      P_loss = calcLosses(fs*(1+kf), B_vet, Ve_vet, Rdc_vet, Rdc_sec, var, CB,
            fL, Cs, Co, n, var_semi);
51
52      % Efficiency
53      eff = Po_design/(Po_design + P_loss)*100;
54
55      % Failures in Time (Reliability)
56      FIT = calcFailures(CB,vBmax,VB_max,80,'Al-Caps'); % Failures/10^6
            hours
57
58      % Cost (cost savings) Cost ($USD)@10,000
59      Cost = 0;
60
61      % objective function
62      obj = weights(1)*Volume + weights(2)*P_loss + weights(3)*FIT +
            weights(4)*Cost;
63
64      % saving data
65      perf_save = [FIT, eff, rho, THD];
66      var_save = [fs, kf, Volume, Vol_disc, P_loss, Cost, var, Is_pk];
67  end
```

B.1.1.1 *Function to Examine the Boundaries of the Search Space*

```
function x = checkBounds(x, lb, ub)
    % lower bounds
    for k=1:length(x)
        if x(k) < lb(k)
            x(k) = lb(k);
            disp(['Lower bound achieved for x(', num2str(k), ')']);
        end
    end
    % upper bounds
    for k=1:length(x)
        if x(k) > ub(k)
            x(k) = ub(k);
            disp(['Upper bound achieved for x(', num2str(k), ')']);
        end
    end
end
```

B.1.1.2 *Script for Designing Converter*

```
function [Lb, Ls, Cs, Lm, n, Co] = designConverter(x, kf, var_nom)
    VG = var_nom(1);
    fL = var_nom(2);
    VB = var_nom(3);
    Po_design = var_nom(4);
    fr = var_nom(5);
    rd = var_nom(6);
    Io_design = var_nom(7);
    delIo_HF  = var_nom(8);
    Ro_design = var_nom(9);
    Vo_design = var_nom(10);
    eff_est= var_nom(11);
    Q = x(2);
    lamb = x(3);
    fnorm = x(4);
    f = fnorm*fr;

    % PFC stage design
    D = 0.5;
    v1 = [f, D, fL, VG, VB, Po_design, eff_est, kf];
    Lb = calcLb(v1);

    % PC stage design
    M = Vo_design/VB;
    % turns ratio
    error = 1; n = 0;
    while abs(error) > 0.00001
```

```
28          n = n + 0.000005;
29          error = (1/(2*n*sqrt((1+lamb-(lamb/fnorm^2))^2 + Q^2*(fnorm-1/
                fnorm)^2))) - M;
30      end
31
32      Rr = (8*n^2/(pi^2))*Ro_design;
33      wr = 2*pi*fr;
34      Ls = double(vpa((Q*Rr)/wr,9));    % inductor series
35      Cs = double(vpa(1/(Q*Rr*wr),9)); % capacitor series
36      Lm = Ls/lamb;                     % parallel inductor
37
38      ws = 2*pi*f;
39      ripple_HF = 1; Co = 2e-6;
40      while abs(ripple_HF) > delIo_HF
41          Co = Co + 0.5e-6;
42          Z_real = 1/(1-(2*ws*Co*rd)^2);
43          Z_imag = -2*ws*Co*rd/(1-(2*ws*Co*rd)^2);
44          Z_mod_p = sqrt(Z_real^2 + Z_imag^2);
45          ripple_HF = 4*Io_design/3*Z_mod_p;
46      end
47  end
```

B.1.1.3 *Script for Setting the Control Variable*

```
1   function [controlVar_min,flag, cont, time,io,ig,is,vB,iCB,Is_pk,
        I_SW_off] = setControlVariable(v1,v2,controlVariable)
2       fL = v2(6);
3       Io_design = v2(14);
4       nmax = 5; % maximum number of attempts
5       e = 0.01*Io_design;
6
7       tff = strcmp(controlVariable,'frequency');
8       tfd = strcmp(controlVariable,'duty');
9       if tff == 1
10          ind = 3;
11          v = 1;
12      end
13      if tfd == 1
14          ind = 5;
15          v = -1;
16      end
17      controlVar = v2(ind);
18
19      [time,io,ig,is,vB,iCB,Is_pk,I_SW_off] = calcConverter(v1,v2,
            Io_design);
20      wL = 2*pi*fL;
```

```
21      [a, b] = fouriercoeff(time, io, 0, 2*wL);    Io = 0.5*sqrt(a^2 + b
            ^2);
22      erro = Io-Io_design;
23      step = v*sign(erro)*0.06*controlVar;
24      if tff == 1 %frequency
25          if abs(erro) < 0.1
26              step = v*sign(erro)*0.01*controlVar;
27          else
28              step = v*sign(erro)*0.05*controlVar;
29          end
30      end
31
32      cont=0; flag = 1; Io_1 = Io;
33      while (abs(erro) > e)
34          cont=cont+1;
35          if cont > nmax
36              flag = 0;
37              break;
38          end
39          if tff == 1 %frequency
40              if step > 0 &&  Io_1 < Io   % ZCS condition
41                  flag = 0;
42                  break;
43              end
44              if step < 0 &&  Io_1 > Io   % ZCS condition
45                  flag = 0;
46                  break;
47              end
48          end
49
50          controlVar_1 = controlVar; Io_1 = Io;
51          controlVar = controlVar + step;
52          if tff == 1 %frequency
53              controlVar = ceil(controlVar/100)*100;
54          end
55
56          v2(ind) = controlVar;
57          [time,io,ig,is,vB,iCB,Is_pk,I_SW_off] = calcConverter(v1,v2,
                Io_design);
58          [a, b] = fouriercoeff(time, io, 0, 2*wL);        Io = 0.5*sqrt(
                a^2 + b^2);
59
60          erro = Io-Io_design;
61          step = v*erro*abs(controlVar - controlVar_1)/abs(Io - Io_1);
62          if step == 0
63              step = v*sign(erro)*0.01*controlVar;
64          end
```

```
65          if step > 1e5
66              step = step/10;
67          end
68      end
69      controlVar_min = controlVar;
70  end
```

B.1.1.4 *Routine for Evaluating the Converter*

```
1  function [deltaIo,PF,THD,harm,vBmax,var,flagDCM] = evaluateConverter(
       time,io,ig,Is,I_SW_off,vB,iCB,VG,fL,D,fo,kf,Lb,n, var_nom)
2      wL = 2*pi*fL;   f_min = (1-kf)*fo;
3      flagDCM = 0;
4
5      % evaluating the input power quality
6      [a, b] = fouriercoeff(time, ig, 1, wL);      I1 = sqrt(a^2 + b^2);
7      [a, b] = fouriercoeff(time, ig, 2, wL);      I2 = sqrt(a^2 + b^2);
8      [a, b] = fouriercoeff(time, ig, 3, wL);      I3 = sqrt(a^2 + b^2);
9      [a, b] = fouriercoeff(time, ig, 5, wL);      I5 = sqrt(a^2 + b^2);
10     [a, b] = fouriercoeff(time, ig, 7, wL);      I7 = sqrt(a^2 + b^2);
11     [a, b] = fouriercoeff(time, ig, 9, wL);      I9 = sqrt(a^2 + b^2);
12     [a, b] = fouriercoeff(time, ig, 11, wL);     I11 = sqrt(a^2 + b^2);
13     harm = [I1 I3 I5 I7 I9 I11];
14     THD = sqrt(0.5*(I2^2+I3^2+I5^2+I7^2+I9^2+I11^2))/(I1/sqrt(2));
15     PF = 1/sqrt(1+THD^2);
16
17     % values of the currents required for efficiency estimation
18     [a, b] = fouriercoeff(time, Is, 0, 2*wL);
19     Is_RMS = 0.5*sqrt(a^2 + b^2);
20     Ib_pk = sqrt(2)*VG*D/(Lb*f_min); % vgmax*ton/L
21     [Ib_RMS, Ib_main] = calcIb_RMS(Lb,fo,kf,D, var_nom);
22     ICB_RMS = calcRMS(time, iCB, 2*wL);
23     I_sec_RMS = Is_RMS*n/sqrt(2);
24     [a, b] = fouriercoeff(time, io, 0, 2*wL);
25     Io = 0.5*sqrt(a^2 + b^2);
26     I_sec_avg = Io/2;
27
28     ID_RMS = Ib_RMS/sqrt(2);
29     [a, b] = fouriercoeff(time, abs(ig), 0, wL);
30     ID_avg = 0.5*sqrt(a^2 + b^2)/2;
31     I_SW_rms = sqrt(Ib_RMS^2+Is_RMS^2)/sqrt(2);
32     [a, b] = fouriercoeff(time, vB, 0, 2*wL);   VB = 0.5*sqrt(a^2 + b
           ^2);
33
34     var = [Is_RMS Ib_RMS Ib_pk ICB_RMS I_sec_RMS I_sec_avg ID_RMS
           ID_avg I_SW_rms Ib_main I_SW_off VB];
35
```

```
36      deltalo = max(io)-min(io);
37      vBmax = max(vB);
38
39      if min(vB) > (sqrt(2)*VG/(1-D))*1.1
40          flagDCM = 1;
41      end
42  end
```

B.1.1.5 *Function for Applying the Frequency Modulation*

```
1  function [fval,perf_save,var_save,flag,Const] = setModulation(x,kf_1,
       v_design,var_semi,weights,f0acc)
2      fmin=v_design(18);
3      deltalo_max = v_design(6);
4      nmax = 5; % maximum number of attempts
5      step = 0.008;
6      kf = kf_1 + step;
7      [fval,perf_save,var_save,flag,Const] = objective(x, kf, v_design,
           var_semi,weights,f0acc);
8      f0acc = var_save(1);
9      deltalo = Const(1) + deltalo_max;
10
11     cont=0;
12     while (deltalo > deltalo_max)
13         cont=cont+1;
14         if cont > nmax
15             break;
16         end
17         kf_1 = kf; deltalo_1 = deltalo;
18
19         kf = kf + step;
20         if var_save(1)*(1-kf) < fmin % kf > kf_max
21             kf = kf - step;
22             disp('f_min achieved');
23         end
24         [fval,perf_save,var_save,flag,Const] = objective(x, kf,
               v_design,var_semi,weights,f0acc);
25         f0acc = var_save(1);
26         deltalo = Const(1) + deltalo_max;
27
28         if deltalo < deltalo_1
29             step = 0.25*(deltalo-deltalo_max)*abs(kf - kf_1)/abs(
                   deltalo - deltalo_1);
30         else
31             kf = kf - step;
32             step = step*0.5;
33         end
```

```
34      end
35  end
```

B.1.2 **Single-cost functions**

B.1.2.1 *Script for Computing the Volume*

```
1  function [Volume,Vol_disc, B_vet, Ve_vet, Rdc_vet, Rdc_sec] =
       CalcVolume(var,Is_pk,Ls,freq,Lm,n,Cs,Co,CB,Lb,display)
2  Is_RMS = var(1);
3  Ib_RMS = var(2);
4  Ib_pk = var(3);
5  I_sec_RMS = var(5);
6
7  %% EE core data
8  core = char({'NEE-20/10/5'
9       'NEE-25/10/6'
10      'NEE-30/15/7'
11      'NEE-30/15/14'
12      'NEE-40/17/12'
13      'NEE-42/21/15'
14      'NEE-42/21/20'
15      'NEE-55/28/21'
16      'NEE-65/33/26'});
17 %     core   AeAw    Ae    Aw    MLT   Ve     BoxVol (c/ carretel em cm3)
18 EE = [1    0.08    0.31  0.26  4.28   1.34    5.10     % EE.20/10/5
19      2    0.17    0.39  0.62  4.90   1.935   6.22     % EE.25/10/6
20      3    0.48    0.6   0.8   6.7    4       17.10    % EE.30/15/7
21      4    1.02    1.2   0.85  6.9    8.174   22.5     % EE.30/15/14
22      5    1.05    1.48  1.02  7.7    11.30   33.05    % EE.40/17/12
23      6    2.84    1.81  1.57  9.70   17.6    56.45    % EE.42/21/15
24      7    3.77    2.40  1.57  9.70   23.30   65.89    % EE.42/21/20
25      8    8.85    3.54  2.50  11.60  42.50   110.88   % EE.55/28/21
26      9    19.68   5.32  3.70  14.80  78.20   184.15];% EE.65/33/26
27
28 %% AWG round copper wire parameters
29 %       AWG ST(cm2)   STi(cm2) (ohm/cm) freq_max
30 AWG = [18   0.008231  0.009735  0.000280  16220
31      19   0.006527  0.007794  0.000353  22460
32      20   0.005176  0.006244  0.000445  25790
33      21   0.004105  0.005004  0.000561  32520
34      22   0.003255  0.004013  0.000708  41010
35      23   0.002582  0.003221  0.000892  51720
36      24   0.002047  0.002586  0.001125  65210
37      25   0.001624  0.002078  0.001419  82230
38      26   0.001287  0.001671  0.001789  103700
39      27   0.001021  0.001344  0.002256  130700
```

```
40      28   0.000810  0.001083  0.002845  164900
41      29   0.000642  0.000872  0.003587  207900
42      30   0.000509  0.000704  0.004523  262100
43      31   0.000404  0.000568  0.005704  330600
44      32   0.000320  0.000459  0.007192  416800
45      33   0.000254  0.000371  0.009070  525600
46      34   0.000201  0.000300  0.011437  662800
47      35   0.000160  0.000243  0.014422  835700];
48
49 %% auxiliary variables
50 Jm = 500;
51 Bm = 0.35;
52 mi_o = 4*pi*0.0000001;
53 kw = 0.7;
54 kms = 0.61; % manual mult-strand wire factor
55
56 % leakage inductance Ld from the self-inductance Lm (~1-5% of Lm)
57 Ld = 0.02*Lm;
58
59 L_vet = [Lm Ls-Ld Lb];
60 VolL_vet = zeros(1,length(L_vet));
61 Vol_L_cont = zeros(1,length(L_vet));
62 B_vet = zeros(1,length(L_vet));
63 Ve_vet = zeros(1,length(L_vet));
64 Rdc_vet = zeros(1,length(L_vet));
65
66 for m=1:length(L_vet)
67     if m>=3 % boost inductance
68         I_RMS = Ib_RMS;
69         I_pk = Ib_pk;
70     else
71         I_RMS = Is_RMS;
72         I_pk = Is_pk;
73     end
74
75     % wire selection
76     ST_L = I_RMS/Jm; % Cross-sectional area of the copper wire
77     n_vet = ceil(ST_L./AWG(:,2));
78     for k=1:length(AWG)
79         if AWG(k,5) > freq
80             row = k;
81             break
82         end
83     end
84     L_AWG = AWG(row,1);
85     ST_L = AWG(row,2);
86     npar = n_vet(row);
```

```
87
88      % magnetic selection
89      L = L_vet(m); Np=0;Ns=0;
90      AeAw_min = L*I_RMS*I_pk/(Bm*Jm*kw) * 10000;
91      ind = 1;
92      for i=1:length(EE(:,1))
93          if EE(i,2) > AeAw_min
94              EE_vet(ind) = EE(i,2);
95              ind = ind +1;
96          end
97      end
98      [row,col] = find(EE(:,2)==EE_vet(1));
99
100     while 1
101         % select the cross-sectional area Ae
102         Ae = EE(row,3);
103         MLT = EE(row,5)
104         nf = 0; B = 0.5;
105         while B > 0.95*0.35
106             nf=nf+1;
107             gap = nf*0.12;
108
109             relutancia_gap =(2*gap/1000)/(mi_o*Ae/10000)*1.08;
110             Np = round(sqrt(L*relutancia_gap)); % number of turns
111
112             J17 = ((exp(2.1104-0.11594*L_AWG)^2)*pi/4)*npar;
113             Rdc_L = MLT/100*Np * 0.0000000172 /(J17/1000000);
114
115             B =((Np*I_pk)/((2*gap/1000)/(mi_o*Ae)))/Ae;
116         end
117
118         if m == 1 % trafo
119             Ns = round(Np/n);
120
121             ST_L2 = I_sec_RMS/Jm;
122             n_vet = ceil(ST_L2./AWG(:,2));
123             for k=1:length(AWG)
124                 if AWG(k,5) > freq
125                     row2 = k;
126                     break
127                 end
128             end
129             L_AWG2 = AWG(row2,1);
130             ST_L2 = AWG(row2,2);
131             npar2 = n_vet(row2);
132
133             J17 = ((exp(2.1104-0.11594*L_AWG2)^2)*pi/4)*npar2;
```

```
134             Rdc_sec = MLT/100*Ns * 0.0000000172 /(J17/1000000);
135         end
136
137         % minimal core window area necessary to accommodate the
                transformer windings
138         Aw = EE(row,4);
139         Aw_min = (Np*npar*ST_L + 2*Ns*npar2*ST_L2)/(kw*kms);
140         if Aw > Aw_min
141             break;
142         else
143             row = row + 1;
144         end
145     end
146
147     % box volume
148     VolL_vet(m) = EE(row,7);
149     B_vet(m) = B;
150     Ve_vet(m) = EE(row,6);
151     Rdc_vet(m) = Rdc_L;
152
153
154     if strcmp(display,'yes') == 1
155         if m==1
156             disp('---------- Transformer Design (Lm) ----------');
157         end
158         if m==2
159             disp('---------- Series Resonant Inductor Design (Ls)
                    ----------');
160         end
161         if m==3
162             disp('---------- Boost Inductor Design (Lb) ----------');
163         end
164
165         disp(['Core ', core(row,:)]);
166         disp(['gap = ', num2str(gap), ' mm']);
167         disp(['AWG ', num2str(L_AWG)]);
168         if m==1
169             disp(['number of turns of prim.= ', num2str(Np), ' ; sec.=
                    ', num2str(Ns), ' (AWG)',num2str(L_AWG2)]);
170         else
171             disp(['number of turns: ', num2str(Np)]);
172         end
173         disp(['cond. em paralelo: ', num2str(npar)]);
174         disp(['box volume: ', num2str(VolL_vet(m)), ' cm^3']);
175     end
176 end
177
```

```
%% linearizing the volume (continuous function)
for m=1:length(L_vet)
    if m>=3
        k_L = fittingVolume(Ib_RMS,Ib_pk,freq);
    else
        k_L = fittingVolume(Is_RMS,Is_pk,freq);
    end
    Vol_L_cont(m) = k_L(1).*L_vet(m).^2 + k_L(2)*L_vet(m)+ k_L(3);
end

%% Estimated Capacitors volume

% Al-Cap Volume (Vr = 500V)
Vol_CB = 0.65*CB*500^2 + 3.53;

% Metallized Polypropylene Capacitors
Vol_Cs = (0.1657*10^9)*Cs + 1.0851;

% Plastic Film Capacitors
Vol_Co = (1.1742*10^6)*Co + 1.0078;

%% estimate volume of passive elements (continuous function)
Volume = sum(Vol_L_cont) + Vol_CB + Vol_Cs + Vol_Co;

%% real volume of passive elements

% Al-Cap (Vr = 500V) - Nichicon UCY e LGN
Al_Cap_vet = [10 15 18 22 27 33 39 47 56 68 82 100 120 150 180 220 270
    330 390]*10^(-6);
Vol_Al = [3.12 3.91 4.92 6.4 6.25 8.06 9.09 10.24 12.1 15.62 16.94
   22.5 27 30.62 36.75 42.87 49 55.12 61.25]; % cm3
Vol_Al_cap = Vol_Al(min(find(CB <= Al_Cap_vet)));

% Metallized Polypropylene Capacitors - TDK B32692A7102+
MP_Cs_vet = [1 1.5 2.2 3.3 4.7 6.8 10 15  22 33 47]*10^(-9);
Vol_MP_Cs = [1.42 1.42 1.482 1.662 1.662 1.995 2.65 3.762 4.22 6.03
   8]; % cm3
Vol_MP_capCs = Vol_MP_Cs(min(find(Cs <= MP_Cs_vet)));
if isempty(Vol_MP_capCs)
    Vol_MP_capCs = Vol_MP_Cs(end);
end

% Plastic Film Capacitors - ECQE(F) series
MP_Co_vet = [1 1.2 1.5 1.8 2.2 2.7 3.3 3.9 4.7 5.6 6.8 8.2 10]*10^(-6)
   ;
Vol_MP_Co = [2.0535 2.3532 2.7972 3.0225 3.6023 4.1548 4.8204 5.863
   6.708 7.6818 9.0272 10.41755 12.71682]; % cm3
```

```
220 Vol_MP_capCo = Vol_MP_Co(min(find(Co <= MP_Co_vet)));
221
222 Vol_disc = sum(VolL_vet)+ Vol_Al_cap + Vol_MP_capCs + Vol_MP_capCo;
223 end
```

B.1.2.2 *Script for Computing the Losses*

```
1  function P_loss = calcLosses(freq,B_vet,Ve_vet,Rdc_vet,Rdc_sec,var,CB,
       fL,Cs,Co,n,var_semi)
2  R_on = var_semi(1);
3  tr = var_semi(2);
4  tf = var_semi(3);
5  V_F = var_semi(4);
6  R_D = var_semi(5);
7  V_Frec = var_semi(6);
8  R_Drec = var_semi(7);
9
10 Is_RMS = var(1);
11 Ib_RMS = var(2); % Ib_pk = var(3);
12 ICB_RMS = var(4);
13 Irec_RMS = var(5);
14 Irec_avg = var(6);
15 ID_RMS = var(7);
16 ID_avg = var(8);
17 I_SW_rms = var(9);
18 I_SW_off = var(11);
19 VB = var(12);
20
21 Kh = 4e-5;
22 Ke = 4e-10;
23 alfa = 2.4;
24
25 %% inductors power losses [Lm Ls Lb Lf]
26 PL_vet = zeros(1,length(Rdc_vet));
27 I_RMS = [Is_RMS Is_RMS Ib_RMS Ib_RMS];
28 for m=1:length(Rdc_vet)
29     if m > 1
30         Rdc_sec = 0;
31     end
32     % inductor core total losses
33     Pcore = Ve_vet(m)*(Kh*B_vet(m)^alfa*freq + Ke*B_vet(m)^2*freq^2);
34     % inductor copper loss
35     Pc = Rdc_vet(m)*I_RMS(m)^2 + 2*Rdc_sec*Irec_RMS^2;
36
37     % inductor power losses
38     PL_vet(m) =  Pcore + Pc;
39 end
```

```
40
41 %% resonant and output capacitor power losses
42 % DF = tan(phi)
43 DF = 1e-3;% Metallized Polypropylene Capacitors, Series/Type: B32692
       ... B32694
44 ESR_s = DF/(2*pi*freq*Cs);
45 P_Cs = ESR_s*Is_RMS^2;
46
47 ESR_o = DF/(2*pi*freq*Co);
48 P_Co = ESR_o*(Is_RMS*n)^2;
49
50 %% bus capacitor power losses
51 DF = 0.24; % Aluminum electrolytic capacitors % datasheet: e_lgn
       -1511829
52 ESR_B = DF/(2*pi*2*fL*CB);
53 P_CB = ESR_B*ICB_RMS^2;
54
55 %% output rectifier losses
56 % only conduction
57 P_rec = 2*(Irec_avg*V_Frec + R_Drec*Irec_RMS^2);
58
59 %% input diodes losses
60 P_D = 2*(ID_avg*V_F + R_D*ID_RMS^2);
61
62 %% half-bridge switches power losses
63 P_HB = 2*(R_on*I_SW_rms^2);
64 Psw =2*(VB*I_SW_off*(tr+tf)*freq)/2;
65
66 %% total power losses
67 P_loss = sum(PL_vet)+P_Cs+P_Co+P_CB+P_rec+P_D+P_HB+Psw;
68 end
```

B.1.2.3 *Script for Computing the Failure Rate*

```
1  function lamb_f = calcFailures(CB,Vcmax,Vr,Ta,tec)
2  C = CB*10^6;
3
4  KB = 8.617*10^(-5); % Boltzmann constant
5  % quality factor
6  kQ = 3; % for Non-Established Reliability capacitors
7  % environment factor
8  kE = 1; % fixed ground environment
9
10 %  different values for each capacitor technology
11 if strcmp(tec,'MPPF-Caps') == 1
12     lamb_b = 0.00051;
13     Ea = 0.15;
```

```
14      k1 = 0.09;
15  end
16  if strcmp(tec,'Al-Caps') == 1
17      lamb_b = 0.00012;
18      Ea = 0.35;
19      k1 = 0.23;
20  end
21
22  % temperature factor
23  kT = exp((-Ea/KB)*(1/(Ta+273)-1/298));
24  % voltage stress factor
25  kV = ((Vcmax/(0.6*Vr))^5)+1;
26  % capacitance factor
27  kC = C^k1;
28
29  lamb_f = lamb_b*kT*kV*kC*kQ*kE;  % failures/10^6hours
30  end
```

B.1.3 **Functions for Evaluating the Converter**

B.1.3.1 *Script for Calculating Low-Frequency Voltages and Currents*

```
1  function [time_ss,io_ss,ig_ss,Is_ss,vB_ss,iCB_ss,Is_pk,I_SW_off] =
       calcConverter(v1,v2,Io_design)
2  Ls = v1(1);
3  Lm= v1(2);
4  n= v1(3);
5  Cs= v1(4);
6  Co= v1(5);
7  Vo_Co= v1(6);
8  CB = v2(1); % kf = v2(2);
9  f2 = v2(2)*v2(13);
10 fo = v2(3);
11 phi2 = (180)*2*pi/360;
12 Lb = v2(4);
13 do = v2(5);
14 fL = v2(6);
15 VG = v2(7);
16 Vt = v2(8);
17 rd = v2(9);
18 eff_pfc = v2(10);
19 eff_pc = v2(11);
20 VB_ini = v2(12);
21
22 % Auxiliary parameters
23 st = 1/(fL*50);
24 t1 = 0;
```

```
25 np = 1;
26 tf = 2/fL;
27
28 ppc = 1/fL/st;
29 wL = 2*pi*fL;
30 time = t1:st:tf;
31 N = length(time)-1;
32 vB = zeros(1,length(time));
33 ig = zeros(1,length(time));
34 Is = zeros(1,length(time));
35 iCB = zeros(1,length(time));
36 io = zeros(1,length(time));
37 Ipeak = zeros(1,length(time));
38 vB(1) = VB_ini;
39 io(1)=Io_design;
40
41 limiar = 0.1; %100mA
42 cont=0;
43 difVp = 100; erv = 0.5;
44 difVi = 100; eri = 0.007;
45
46 while (abs(difVp) > erv || abs(difVi) > eri)
47       for k=1:(length(time)-1)
48          t = time(k);
49          f = fo + f2*sin(2*wL*t+phi2);
50          d = do;
51          vg = sqrt(2)*VG*sin(wL*t);
52          iD = vg^2*d^2/(2*Lb*f*(abs(abs(vg)-vB(k))));
53
54          % solution of the LLC converter
55          var = [vB(k) f d Ls Lm n Cs Co Vo_Co Vt rd];
56          if k==1
57              U0 = [0; 0; 0; Vo_Co];
58          else
59              U0 = Uf;
60          end
61          [t_sim, is_sim, io_sim,I_SW_off, Uf] = solveLLC(var,U0);
62
63          Ipeak(k+1) = max(is_sim);
64          Is(k+1) = calcRMS(t_sim, is_sim, f);
65          [a, b] = fouriercoeff(t_sim, io_sim, 0, 2*wL);    Io = 0.5*sqrt
               (a^2 + b^2);
66          % checking error
67          flagError = Io < limiar;
68          if flagError == 0
69              M = Io/vB(k);
70          else
```

```
71              M = io(k)/vB(k);
72          end
73
74          % solution of the bus voltage
75          iCB(k+1) = eff_pfc*iD-(vB(k)*M^2*rd+M*Vt)/eff_pc;
76          vB(k+1) = vB(k)+st*1/CB*iCB(k+1);
77
78          % solution of the input current and output current
79          ig(k+1) = d^2*vB(k)/(2*f*Lb)*(vg/(vB(k+1) - abs(vg)));
80          io(k+1)= M*vB(k+1);
81       end
82
83
84      difVp = checkTransient(time,vB);
85      if cont > 3
86          difVp = 0;
87      end
88      if abs(difVp) < 0.5
89          yy = smooth(time,io,0.1,'rloess');
90          io = yy';
91          difVi = checkTransient(time,io);
92      end
93
94
95      if abs(difVi) > eri
96          t1 = time(k+1);
97          tf = tf+np/fL;
98          time = t1:st:tf;
99          aux = vB(k+1);
100         vB = zeros(1,length(time)); vB(1) = aux;
101         aux = ig(k+1);
102         ig = zeros(1,length(time)); ig(1)= aux;
103         aux = Is(k+1);
104         Is = zeros(1,length(time)); Is(1)= aux;
105         aux = iCB(k+1);
106         iCB = zeros(1,length(time)); iCB(1) = aux;
107         aux = io(k+1);
108         io = zeros(1,length(time)); io(1)= aux;
109         Ipeak = zeros(1,length(time));
110         cont = cont +1;
111     end
112 end
113
114 % Exclusion of the data regarding the transitory state
115 time_ss = time(length(time)-ppc:length(time));
116 vB_ss = vB(length(time)-ppc:length(time));
117 ig_ss = ig(length(time)-ppc:length(time));
```

```
Is_ss = Is(length(time)-ppc:length(time));
io_ss = io(length(time)-ppc:length(time));
iCB_ss = iCB(length(time)-ppc:length(time));
Is_pk = max(Ipeak);
end
```

B.1.3.2 *Script for Calculating the High-Frequency Current of the Tank*

```
function [t,is,io,I_SW_off,Uf] = solveLLC(var,U0)
    vB = var(1);ws = 2*pi*var(2);d = var(3);Ls = var(4); Lp = var(5);
    n = var(6);Cs = var(7); Co = var(8); Vo_Co = var(9); Vt = var(10);
        rd = var(11);

        % Iteration Parameters
    ppc=180; dt=1/(ppc*var(2));
    ti = 0.38e-3;
    tf = ti + 2/var(2);
    t_print = [ti tf];
    t1 = 0;

    % Auxiliary variables
    tol_fsolve = 2e-3; %1e-3;
    Ls_1 = 1/Ls;
    Cs_1 = 1/Cs;
    Lp_n = n/Lp;
    Co_1 = 1/Co;
    rd_1 = 1/rd;

    sz = round(tf/dt);
    u = zeros(length(U0),sz);
    t = zeros(1,sz);
    t_k = 0;
    io = zeros(1,sz); is = zeros(1,sz);
    iM1 = zeros(1,sz);
    options = optimoptions(@fsolve,'Display','off','TolFun',tol_fsolve
        ,'TolX',tol_fsolve);
    u(:,1) = U0;
    k=1;

 while t_k < tf
        k = k+1;
        t1 = t1 + dt;
        t_k = t_k + dt;
        u_k1 = u(:,k-1);

        vhb = d*vB*(1+ sign(sin(ws*t1)));

```

```
38          f_k1 = [(Ls_1*(vhb-n*u_k1(4)*(sign(u_k1(1)-u_k1(3)))-u_k1(2)))
39                  (Cs_1*u_k1(1))
40                  (Lp_n*(u_k1(4))*(sign(u_k1(1)-u_k1(3))))
41                  (Co_1*(n*abs(u_k1(1)-u_k1(3))-((u_k1(4)-Vt)*rd_1)))];
42
43              varf = [Vt rd_1 Ls_1 Lp_n n Cs_1 Co_1 dt u_k1(1) u_k1(2)
                    u_k1(3) u_k1(4) f_k1(1) f_k1(2) f_k1(3) f_k1(4) vhb];
44              u(:,k) = fsolve(@(u) LLC_solve_k(u, varf), u(:,k-1),
                    options);
45
46          t(k) = t_k;
47          io(k) = (u(4,k) - Vt)*rd_1;
48          % Other variables of interest:
49          is(k) = u(1,k);
50          iM1(k) = (0.5*(sign(sin(ws*t(k)))+1)*is(k));
51  end
52          Uf = [u(1,k) u(2,k) u(3,k) u(4,k)];
53
54      dbstop if error
55
56      ii = find(t >= t_print(1), 1);
57      t = t(ii:k);
58      is = is(ii:k);
59      io = io(ii:k);
60      iM1 = iM1(ii:k);
61      aux = iM1(find(diff(iM1 > 0.010) < 0));
62      if isempty(aux)
63          I_SW_off = 0;
64      else
65          I_SW_off = aux(end);
66      end
67  end
```

B.1.3.3 *Supplementary Function of the LLC Script*

```
1  function F = LLC_solve_k(u,var)
2  % Script with the system of nonlinear equations
3  Vt=var(1); rd_1=var(2); Ls_1=var(3); Lp_n=var(4); n=var(5); Cs_1=var
       (6);
4  Co_1=var(7); dt=var(8); vhb=var(17);
5
6  F = zeros(4, 1);
7  u_k1 = zeros(4, 1); f_k1 = zeros(4, 1);
8  u_k1(1) = var(9); u_k1(2) = var(10); u_k1(3) = var(11); u_k1(4) = var
       (12);
9  f_k1(1) = var(13); f_k1(2) = var(14); f_k1(3) = var(15); f_k1(4) = var
       (16);
```

```
10 F(1) = u(1) - u_k1(1) - 0.5*dt*(f_k1(1) + ((Ls_1)*(vhb-n*u(4)*(sign(u
       (1)-u(3)))-u(2))) );
11 F(2) = u(2) - u_k1(2) - 0.5*dt*(f_k1(2) + ((Cs_1)*u(1)));
12 F(3) = u(3) - u_k1(3) - 0.5*dt*(f_k1(3) + ((Lp_n)*(u(4))*(sign(u(1)-u
       (3)))) );
13 F(4) = u(4) - u_k1(4) - 0.5*dt*(f_k1(4) + ((Co_1)*(n*abs(u(1)-u(3))
       -(((u(4)-Vt)*rd_1)))) );
14 end
```

B.1.3.4 *Script for Checking the Transient*

```
1  function difVp = checkTransient(t,y)
2  ind = 0; peak=zeros(1,2); tp=zeros(1,2);
3  for k=2:length(t)-1
4      if y(k)>y(k-1) && y(k)>y(k+1)
5          ind = ind + 1;
6          peak(ind) = y(k);
7          tp(ind) = t(k);
8          if ind>1 && tp(ind)-tp(ind-1) < 0.0075 %1/120*0.9
9              ind = ind - 1;
10         end
11     end
12 end
13 if ind <= 1
14     difVp = 1000;
15 else
16     difVp = peak(ind)-peak(ind-1);
17 end
18 end
```

B.1.4 **Auxiliary Functions Beyond the Previously Discussed Ones**

B.1.4.1 *Script for Fitting the Volume Curve*

```
1  function k_L = fittingVolume(I_RMS,I_pk,freq)
2
3  L_vet = 2e-6:200e-6:12e-3;
4  VolL_vet = zeros(1,length(L_vet));
5
6  %% EE core data
7  %    core  AeAw   Ae   Aw   MLT  Ve    BoxVol (c/ carretel em cm3)
8  EE = [1    0.08   0.31 0.26 4.28 1.34   5.10    % EE.20/10/5
9        2    0.17   0.39 0.62 4.90 1.91   6.22    % EE.25/10/6
10       3    0.48    0.6  0.8  6.7  4       17.10   % EE.30/15/7
11       4    1.02    1.2  0.85 6.9  8       22.5    % EE.30/15/14
12       5    1.05    1.48 1.02 7.7  11.39   33.05   % EE.40/17/12
```

```
13          6    2.84    1.81  1.57  9.70   17.6     56.45   % EE.42/21/15
14          7    3.77    2.40  1.57  9.70   23.30    65.89   % EE.42/21/20
15          8    8.85    3.54  2.50  11.60  42.50    110.88  % EE.55/28/21
16          9    19.68   5.32  3.70  14.80  78.20    184.15];% EE.65/33/26
17
18 %% AWG round copper wire parameters
19 %       AWG ST(cm2)  STi(cm2) (ohm/cm) freq_max
20 AWG = [18   0.008231  0.009735  0.000280  16220
21          19   0.006527  0.007794  0.000353  22460
22          20   0.005176  0.006244  0.000445  25790
23          21   0.004105  0.005004  0.000561  32520
24          22   0.003255  0.004013  0.000708  41010
25          23   0.002582  0.003221  0.000892  51720
26          24   0.002047  0.002586  0.001125  65210
27          25   0.001624  0.002078  0.001419  82230
28          26   0.001287  0.001671  0.001789  103700
29          27   0.001021  0.001344  0.002256  130700
30          28   0.000810  0.001083  0.002845  164900
31          29   0.000642  0.000872  0.003587  207900
32          30   0.000509  0.000704  0.004523  262100
33          31   0.000404  0.000568  0.005704  330600
34          32   0.000320  0.000459  0.007192  416800
35          33   0.000254  0.000371  0.009070  525600
36          34   0.000201  0.000300  0.011437  662800
37          35   0.000160  0.000243  0.014422  835700];
38
39 %% auxiliary variables
40 Jm = 500;
41 Bm = 0.35;
42 mi_o = 4*pi*0.0000001;
43 kw = 0.7;
44 kms = 0.61; % manual mult-strand wire factor
45
46 for m=1:length(L_vet)
47     ST_L = I_RMS/Jm; % Cross-sectional area of the copper wire
48     n_vet = ceil(ST_L./AWG(:,2));
49     for k=1:length(AWG)
50         if AWG(k,5) > freq
51             row = k;
52             break
53         end
54     end
55     ST_L = AWG(row,2);
56     npar = n_vet(row);
57
58     L = L_vet(m); Np=0;
59
```

```
60      AeAw_min = L*I_RMS*I_pk/(Bm*Jm*kw) * 10000;
61      ind = 1;
62      for i=1:length(EE(:,1))
63          if EE(i,2) > AeAw_min
64              EE_vet(ind) = EE(i,2);
65              ind = ind +1;
66          end
67      end
68      [row,col] = find(EE(:,2)==EE_vet(1));
69
70      while 1
71          Ae = EE(row,3);
72          MLT = EE(row,5);
73
74          nf = 0; B = 0.5;
75          while B > 0.95*0.35
76              nf=nf+1;
77              gap = nf*0.12;
78
79              relutancia_gap =(2*gap/1000)/(mi_o*Ae/10000)*1.08;
80              Np = round(sqrt(L*relutancia_gap));
81
82              B =((Np*I_pk)/((2*gap/1000)/(mi_o*Ae)))/Ae;
83          end
84
85          % minimal core window area necessary to accommodate the
                transformer windings
86          Aw = EE(row,4); Ns = 0;
87          Aw_min = (Np*npar*ST_L + 2*Ns*npar*ST_L)/(kw*kms);
88          if Aw > Aw_min
89              break;
90          else
91              row = row + 1;
92          end
93      end
94
95      % box volume
96      VolL_vet(m) = EE(row,7);
97  end
98
99  k_L = polyfit(L_vet,VolL_vet,2);
100
101 % figure
102 % plot(L_vet*10^3,VolL_vet,'ok'); hold on
103 % plot(L_vet*10^3,Vol_e_fit,'-r'); hold off
104 % xlabel('mH'); grid on
105 end
```

B.1.4.2 *Script for displaying Components of the converter*

```
function printConverter(x,Const,v_design, kf_vet,fo_vet,Is_pk_vet,
    var_save,CB_vet,tol_CB,CB_poss, converter)

    VG_nom=v_design(1);fL=v_design(2);
    rd=v_design(4);Io_design=v_design(5);
    dello_HF=v_design(7);Ro_design=v_design(8);Vo_design=v_design(9);
        Po_design=v_design(10); eff_pfc=v_design(11);
    eff_pc=v_design(12);fr=v_design(13);
    VB_max=v_design(14);
    VB_nom=v_design(15);

    var_nom = [VG_nom fL VB_nom Po_design fr rd Io_design dello_HF
        Ro_design Vo_design eff_pfc*eff_pc];
    var = var_save(7:16);

    tff = strcmp(converter,'Benchmark');
    tfd = strcmp(converter,'Optimized');
    if tff == 1
        kf = kf_vet(1);
        fs = fo_vet(1);
        Is_pk = Is_pk_vet(1);
        disp(' ---------- Benchmark converter ---------- '); disp('');
    end
    if tfd == 1
        kf = kf_vet(end);
        fs = fo_vet(end);
        Is_pk = Is_pk_vet(end);
        disp(' ---------- Optimized converter ---------- '); disp('');
    end

    f2 = kf*fr;
    disp(['fo = ', num2str(fs*0.001), ' kHz']);
    disp(['kf = ', num2str(kf*0.001), ' kHz and f2 = ', num2str(f2
        *0.001), ' kHz']); disp('');

    [Lb, Ls, Cs, Lm, n, Co] = designConverter(x,kf,var_nom);

    % Selecting the commercially available capacitance value
    CB_opt = CB_vet./(1-tol_CB);
    CB_com = zeros(size(CB_opt));
    for i = 1:length(CB_opt)
        indices = find(CB_poss >= CB_opt(i));
        if ~isempty(indices)
            CB_com(i) = min(CB_poss(indices));
        end
```

```
42      end
43
44      disp(['Lb = ', num2str(Lb*10^6), ' uH']);
45      if tff == 1 disp(['CB = ', num2str(CB_com(1)*10^6), ' uF']); end
46      if tfd == 1 disp(['CB = ', num2str(CB_com(end)*10^6), ' uF']); end
47      disp(['Ls = ', num2str(Ls*10^6), ' uH']);
48      disp(['Cs = ', num2str(Cs*10^9), ' nF']);
49      disp(['Lm = ', num2str(Lm*10^3), ' mH']);
50      disp(['n = ', num2str(n)]); disp(' ');
51
52      [~,~,~,~,~,~] = calcVolume(var,Is_pk,Ls,(1-kf)*fs,Lm,n,Cs,Co,x(1),
            Lb,'yes');
53      disp('');
54
55      disp(' ---------- controller gains ---------- '); disp('');
56      % Average control (pure integrator)
57      Ka = 2*pi*1.3;
58      % Discretizing the controller
59      f_sam = 10000;
60      % ---> y = y_1 + Nav*(e + e_1)
61          Nav = Ka/(2*f_sam)*2*pi*fr;
62      disp(['discretized gain: Nav = ', num2str(Nav)]);
63
64      if tfd == 1
65          % Controladores
66          VB_120  = (Const(8) + VB_max - VB_nom);
67          % ARC branch
68          Kbp = f2/VB_120;
69  %         disp(['ARC branch']);
70          disp(['low-pass filter gain: Kbp = ', num2str(Kbp)]);
71      end
72      disp('');
73  end
```

B.1.4.3 *Function for Computing the Coefficients of the Fourier Serie*

```
1  function [ax, bx] = fouriercoeff(time, i, h, w)
2  % Function for calculating the coefficients of the fourier series
3  T = 2*pi/w;
4  tstep = time(2)-time(1);
5
6  time = time - time(1);
7  th = w*time;
8
9  per = time(length(time))/T;
10
11 ax = (2/T)*trapz(tstep*i.*cos(h*th))/per;
```

```
12 bx = (2/T)*trapz(tstep*i.*sin(h*th))/per;
13 end
```

B.1.4.4 *Function for Designing the Boost Inductance*

```
1  function Lb = CalcLb(v1)
2
3  fo = v1(1);
4  D = v1(2);
5  fL = v1(3);
6  VG = v1(4);
7  VB = v1(5);
8  Po = v1(6);
9  eff = v1(7);
10 f2 = v1(8)*fo;
11 phi2 = (180)*2*pi/360;
12
13 % Auxiliary parameters
14 st = 1/(fL*1000);
15 t1 = 0;
16 tf = 1/(2*fL);
17 wL = 2*pi*fL;
18 time = t1:st:tf;
19 N = length(time)-1;
20 int = zeros(1,length(time));
21 int(1) = 0;
22
23 for k=1:N
24     t = time(k);
25     f = fo + f2*sin(2*wL*t+phi2);
26     vg = sqrt(2)*VG*sin(wL*t);
27     int(k+1) = int(k) + st*vg^2/(VB - abs(vg))/f;
28 end
29 Lb = eff*fL*D^2*VB/Po*int(end);
30 end
```

B.1.4.5 *Function for Computing the rms Value*

```
1 function [rms] = calcRMS(time, i, f)
2 % Function for calculating the RMS value of the waveform
3 T = 1/f;
4 tstep = time(2)-time(1);
5 time = time - time(1);
6 per = time(length(time))/T;
7
8 rms = sqrt((1/T)*trapz(tstep*i.^2)/per);
```

```
9 end
```

B.1.4.6 *Function for Rebuilding the Boost Inductor Current and Calculating its rms Value*

```
1  function [Ib_RMS, Ib_main] = calcIb_RMS(Lb,fo,kf,do, var_nom)
2  VG_nom=var_nom(1);
3  fL=var_nom(2);
4  VB_nom=var_nom(3);
5  Po_design=var_nom(4);
6  fr=var_nom(5);
7
8  wL = 2*pi*fL;
9  phi2 =0;
10 f2 = kf*fr;
11 R = VB_nom^2/Po_design;
12 t3= 0; aux = 0;
13
14 nper = 1/(2*fL)*fo;
15 time = 0:1/fo:nper/fo;
16 iL = zeros(3*floor(nper)-2,1);
17 time_v = zeros(3*floor(nper)-2,1); kk=2;
18
19  for k=2:nper
20      t = time(k);
21      f = fo + f2*sin(2*wL*t+phi2);
22      d = do;
23      vg = sqrt(2)*VG_nom*sin(wL*t);
24
25      aux = aux + 1;
26      D2 =  VB_nom/(sqrt(2)*VG_nom)*(2*Lb*f/(R*d))/f;
27      t1 = d/f + t3;
28      t2 = t1 + D2;
29      t3 = aux/f;
30
31      Ipk = abs(vg)*d/(Lb*f);
32
33      time_v(kk)=t1; time_v(kk+1)=t2; time_v(kk+2)=t3;
34      iL(kk)=Ipk;
35      kk=kk+3;
36  end
37
38   timeq = time_v(1):(time_v(3)-time_v(2))/3:time_v(end);
39   iLq = interp1(time_v,iL,timeq);
40
41   Ib_RMS = calcRMS(timeq, iLq, 2*fL);
```

```
42
43    [a, b] = fouriercoeff(timeq, iLq, 1, wL);      I1 = sqrt(a^2 + b^2);
44    Ib_main = I1/sqrt(2);
45  end
```