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A Prototype of a Narrowband Hybrid PLC/Wireless Transceiver

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Dedico este trabalho aos meus pais Luís Guilherme e Tereza Maria, ao meu irmão Vítor e à minha namorada Larissa.

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"Our virtues and our failings are inseparable, like force and matter. When they separate, man is no more."

(Nikola Tesla)

RESUMO

Esta dissertação descreve o protótipo de um transceptor banda estreita (*narrowband* - NB) *hybrid power line communication* (PLC)/Wireless (NB hybrid PLC/Wireless), o qual utiliza a rede de energia elétrica e o ar, em paralelo, para transmissão de dados, visando aplicações de redes inteligentes (*smart grid* - SG) e Internet das Coisas (*Internet of Things* - IoT). Nesse protótipo é introduzida uma versão aprimorada e adaptada do padrão IEEE 1901.2, contemplando a subcamada de controle de acesso ao meio (*medium access control* - MAC) e da camada física (*physical* - PHY) para transmissão de dados por ambos os meios de comunicação. O aprimoramento é baseado no uso da transformada de Hilbert para a recuperação da informação em quadratura em ambos os canais, possibilitando a estimação do desvio de frequência entre os *clocks* do transmissor e do receptor. Uma das adaptações no padrão IEEE 1901.2 é a introdução do protocolo de roteamento, o qual possibilita o transceptor a se comunicar com nós a dois ou mais saltos de distância entre eles. A outra adaptação é a implementação de uma técnica de correção de pacotes com erro a nível de camada de enlace, a qual combina os pacotes com erros recebidos pelas interfaces PLC e/ou wireless e corrige-os, dentro de uma certa capacidade. Importante ressaltar que o transceptor NB hybrid PLC/Wireless é capaz de interoperar com o transceptor NB PLC baseados no padrão IEEE 1901.2. O protótipo do transceptor NB hybrid PLC/Wireless é implementado usando um dispositivo *field-programmable gate array* (FPGA) usando uma linguagem descritiva de hardware (*hardware description language* - HDL), buscando-se a economia de recursos de hardware. Os resultados numéricos discutem o tempo necessário para execução da técnica de correção de pacotes com erros, levando em consideração as restrições de tempo do padrão IEEE 1901.2. Além disso, uma análise de taxa de dados na camada PHY mostra que a implementação está de acordo com o padrão IEEE 1901.2 e pode perfeitamente satisfazer as necessidades de aplicações para SG e IoT. Ademais, a análise do uso de recursos de hardware e do consumo de energia mostram que o protótipo do transceptor NB hybrid PLC/Wireless demanda menos que uma vez e meia os recursos de hardware e o consumo de energia do protótipo do transceptor NB PLC.

Palavras-chave: Comunicação via rede de energia elétrica, comunicação sem fio, híbrido, taxa de dados, probabilidade de interrupção.

ABSTRACT

This thesis focuses on a prototype of the so-called narrowband (NB) hybrid power line communication (PLC)/Wireless transceiver, which jointly uses power line and wireless channels, in parallel, for data communication related to smart grid (SG) and Internet of Things (IoT) applications. To build the prototype, it is introduced an enhanced and adapted version of the IEEE 1901.2 Standard to implement the medium access control (MAC) sublayer and the physical (PHY) layer to transmit data through both channels. The enhancement is based on the use of the Hilbert transform to recover the quadrature information from both channels, enabling to estimate the frequency deviation between the transmitter and receiver's clocks. One adaptation in the IEEE 1901.2 Standard is the introduction of a routing protocol, which enables the transceivers to communication with nodes two hops or farther from each other. The other adaptation is the implementation of a packet error correction technique at the link layer level, which combines packets with errors received from PLC and wireless media and correct them, under certain constraint. Moreover, relevant is the fact that the NB hybrid PLC/Wireless transceiver is compatible with the NB PLC transceiver based on the IEEE 1901.2 Standard. The NB hybrid PLC/Wireless transceiver prototype is implemented in a field-programmable gate array (FPGA) device and details about the implementation, using a hardware description language (HDL), are provided, highlighting the pursuit of hardware resource savings. Numeric results discuss the time analysis of the packet error correction technique, calculating its maximum capacity of correction taking into account the IEEE 1901.2 Standard time constraints. Furthermore, a PHY layer data-rate analysis shows that the implementation agree with the IEEE 1901.2 Standard and can perfectly satisfy the needs of SG and IoT applications. In addition, the hardware resource usage and power consumption analysis show that the NB hybrid PLC/Wireless transceiver prototype demands less than one and a half times the hardware resource usage and power consumption of the NB PLC transceiver prototype.

Key-words: power line communication, wireless communication, hybrid, achievable data-rate, outage probability.

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ACRONYMS

ACK acknowledgment

ADC analog-to-digital converter

AFE analog front-end

AGC automatic gain control

ARIB Association of Radio Industries and Businesses

ARQ automatic repeat request

Avalon-MM Avalon Memory-Mapped

Avalon-ST Avalon Streaming

Avalon-TC Avalon Tri-State Conduit

BPSK binary phase-shift keying (PSK)

CC convolutional code

CENELEC Comité Européen de Normalisation Électrotechnique

CFS contention-free slot

CIFS contention interframe spacing

CP cyclic prefix

CRC-8 cyclic redundancy check - 8

CRC-16 cyclic redundancy check - 16

CSMA/CA carrier sense multiple access/collision avoidance

CW contention window

D8PSK differential eigth PSK

DAC digital-to-analog converter

DBPSK differential binary PSK

DFT discrete Fourier transform

DQPSK differential quaternary PSK

DSP digital signal processing

e-PHY RX enhanced-PHY RX

ETSI European Telecommunications Standards Institute

FCC Federal Communications Commission

FCH frame control header

FEC forward error correction

FIFO firts-in first-out

FPGA field-programmable gate array

GPIO general purpose input-output

HDL hardware description language

HPCW high-priority contention window (CW)

IDFT inverse discrete Fourier transform

IoT Internet of Things

ISI inter-symbol interference

ISM industrial, scientific, and medical

ITU-T ITU Telecommunication Standardization Sector

LE logic element

LNA low-noise amplifier

LP-RF low-power radio frequency

LUT look-up table

LV low-voltage

M2P MAC-to-PHY

MAC medium access control

MFR MAC footer

MHR MAC header

MSB most-significant bit

MV medium-voltage

NB narrowband

NLOS non-line-of-sight

NPCW normal-priority CW

OFDM orthogonal frequency-division multiplexing

OFDMA orthogonal frequency-division multiple access

P-AFE PLC-analog front-end (AFE)

P/S parallel-to-serial

P2M PHY-to-MAC

PA power amplifier

PCS physical carrier sense

PGA programmable gain amplifier

PHY physical

PLC power line communication

PLCP physical layer convergence protocol

PLL phase-locked loop

PRIME Power Intelligence Metering Evolution

PSDU PLCP Service Data Unit

PSK phase-shift keying

QAM quadrature amplitude modulation

QPSK quaternary PSK

RAM random-access memory

RC repetition code

RF radio frequency

RIFS response interframe spacing

RREQ routing request

RREP routing reply

RREP-ACK routing reply (RREP) acknowledge

ROBO robust OFDM

ROM read-only memory

RS Reed-Solomon

RX receiver

S-ROBO super-robust OFDM

S/P serial-to-parallel

SG smart grid

SI serial interface

SISO single-input single-output

SPI serial peripheral interface

TX transmitter

UART universal asynchronous receiver/transmitter

W-AFE wireless-AFE

CONTENTS

1 Introduction

Nowadays, due to the interest to turn electric power grids into smart grids (SGs) and to widespread the concept of Internet of Things (IoT), research efforts have been made to investigate and improve power line communication (PLC) systems [1–12], which is one of the main data communication technologies for accomplishing or assisting this aim [13]. On the other hand, wireless communication is also a remarkable alternative to constitute telecommunication infrastructures for SG, having in mind that this technology is in a well-established level of development for this purpose. Furthermore, it is a common sense that SG and IoT will be supported by a wide range of data communication technologies, as no single solution fits all the expected scenarios [6, 7]. When cost and installation complexity aspects come to matter, technical literatures recognize that PLC and wireless technologies sound to be the best options on the market for designing a pervasive telecommunication infrastructure for SG. In this context, narrowband (NB)-PLC and unlicensed wireless communication are selected as the two main data communication technologies for SG [14] and IoT [15]. Moreover, recent researches are showing that these two technologies can bring improvements when combined, in order to exploit the existing diversity between PLC and wireless channels and, therefore, to bring a lot of benefits for low-bit-rate applications, such as flexibility, reliability, and coverage [16, 17].

Regarding the used of electric power grids for data communication purpose, it is well-known that they are harsh media for data communication, because they were specified and designed to maximize energy transmission and delivery at low frequency, and not for data transmission at high frequencies. The presence of impulsive noises due to loads dynamic; the use of unshielded cables that results in electromagnetic interference; power line breakers that open the electric circuit and interrupts the flow of energy; the existence of increasing time and frequency signal attenuations at the distance increase due to nonideal propagation characteristics of power cables; the occurrence impedance mismatching at the connection points (e.g. outlets) can severally degrade and corrupt the propagation of signals carrying information in these media [4, 5, 18, 19]. Aiming to characterize electric power grids for data communication purpose and to come up with tools to overcome the harsh medium hindrance, several measurement campaigns with measurement setups relying on digital signal processing techniques, which estimate time frequency behavior of PLC channels, measure the access impedance and electromagnetic interference, and characterize the additive noise, are being reported in the literature [20–26]. Moreover, special attentions are being driven to the use of mathematical tools and algorithms for improving the performance of PLC systems at the physical (PHY) and link layer levels. The results of these initiatives are the introduction of PLC systems based on advanced digital communication schemes, such as the orthogonal frequency-division multiplexing (OFDM) [27], orthogonal frequency-division multiple access (OFDMA) [28, 29], ultra-wideband [30–32],

wavelet-OFDM [33, 34], and single carrier cyclic prefix [35] together with advanced channel coding, resource allocation, cooperative communication, among others. Regarding the link layer, improvements are being obtained based on cooperative communication, network coding, and modification of medium access protocols [36–39].

On the other hand, the wireless communications also presents issues in its media. The signal carrying information suffers from three different propagation effects: reflection, scattering, and diffraction [40]. The first effect occurs when the propagating signal meets a very large object in comparison with its wavelength. On the contrary, scattering effect happens when the propagation signal meets a very small object in comparison with its wavelength. Finally, the diffraction effect arises when the signal passes through a sharpened object. It is important to mention that reflection and diffraction enables the non-line-of-sight (NLOS) data communications. Besides the issues introduced by the aforementioned effects, the transmitted signal through wireless channel also is affected by interference, which is primarily generated by uncoordinated transmissions [41], which can also occur in PLC when noninteroperable PLC technologies perform data communication over the same electric power grid.

Currently, it has been recognized that PLC and wireless technologies may offer distinct advantages and disadvantages concerning a target application [42] due to the aforementioned problems. In order to deal with problems related to PLC and wireless media and also to fulfill the increasing demand for higher data-rate, reliability and coverage, investigations of advanced techniques at link and PHY layers, which maximize the use of the available resource under hardware resource constraints, among other advanced data communication techniques, are challenging issues to be pursued. In this context, cooperative communication was introduced [43]. At first, the cooperative communication aimed to improve reliability and coverage in wireless communication system [44–46]. Nowadays, it is also applied to improve PLC system performance in terms of reliability and coverage, focusing mainly on the PHY layer [47–50] than the link layer [51].

Recently, the exploitation of the existing diversity between both PLC and wireless channels together with the use of a cooperative protocol have been considered in order to benefits SG and IoT applications [16, 17, 41, 42, 52–56]. Concerning this topic, [42] discussed advantages and disadvantages of NB-PLC and low-power radio frequency (LP-RF) wireless communication. Also, [54] revealed that PLC enhances the performance of wireless communication, even using very low transmission power. Moreover, [54] highlighted that PLC is a promising candidate to improve wireless relaying schemes. In addition, [55] discussed that consistent performance improvements can be achieved by using an ideal multi-channel (PLC and wireless) receiver. Furthermore, [17] used link throughput analysis to show that the likelihood of low throughput links can be minimized exploiting the existence diversity between PLC and wireless channels. On the other hand, [56] showed

that parallel PLC and wireless communications (hybrid PLC/Wireless system) with multihop relaying enhances performance in comparison to the sole use of PLC or wireless communication. In sequel, [16] concluded that NB hybrid PLC/Wireless systems may improve the maximum achievable data-rate for a point-to-point transmission in comparison to the sole use of PLC or wireless system. The achievable data-rate in a NB hybrid PLC/Wireless single-relay channel model under a sum power constraint and for several relay locations were examined in [16, 57].

Based on the previous discussion, it is clear that the use of the concept of hybridism into data communication systems is recent and, therefore, comprehensive investigations about PHY and link layers designs for maximizing the usage of the existing diversity among two of them are very appealing research topics to come up with novel generation of data communication techniques for assisting SG and IoT massive deployments. Another very interesting investigation is to prototype a testbed that is capable of demonstrating the advantages and disadvantages that hybrid data communication technologies may offer to improve coverage, reliability and data-rate of current telecommunication infrastructures as well the hardware limitation to accomplish this aim. In fact, demonstrations of hybrid data communication technologies based on prototypes have the potential of bringing more attention to this subject and revealing important issues that must be carefully addressed in order to introduce these technologies into the market. In this regard, Section 1.1 discusses the objectives of this thesis.

1.1 Objectives

Aiming to verify the benefits of hybridism in data communication systems, this thesis addresses the prototype of a NB PLC/Wireless transceiver, which is based on a field-programmable gate array (FPGA) device. This investigation is carried out at frequency bands which covers low-bit-rate applications related to SG and industrial IoT, such as control applications [14], smart metering [58], and industrial sensor network [59]. In this regard, the main objectives of this thesis are as follows:

- To discuss adaptations and enhancements which must be introduced in the IEEE 1901.2 Standard to allow its use as the core standard at the PHY layer and medium access control (MAC) sublayer of the NB hybrid PLC/Wireless transceiver. The adaptations are based on the Hilbert transform, which allows the recovery of the quadrature component of the received signal and performs carrier frequency offset estimation and correction. On the other hand, the enhancements are a routing protocol and an error-correcting technique that are implemented in a MAC sublayer level. The former allows us to introduce a hybrid data network based on the IEEE 1901.2 Standard that can cover more than one hop, while the latter can reduce

packet error rates at the MAC sublayer level.

- To introduce and describe the NB hybrid PLC/Wireless transceiver prototype, which is constituted by a processor, PLC-analog front-end (AFE) (P-AFE), and wireless-AFE (W-AFE). Furthermore, to analyze the performance of the used error-correcting technique to recover received packets with error at the MAC sublayer, considering the IEEE 1901.2 Standard time constraints, in terms of hardware resource usage and time consumption. Also, to evaluate the hardware resource usage demands of an FPGA device, comparing NB PLC transceiver based on the IEEE 1901.2 Standard with the proposed NB hybrid PLC/Wireless transceiver.

1.2 Dissertation outline

This document is organized as follows:

- Chapter 2 formulates the problem addressed in this thesis, evaluating firstly the most suitable approach for accomplishing data communication using PLC and wireless media within the hybridism concept. Later, it addresses the most relevant standards on the market for PLC systems and their main differences and characteristics. Finally, a discussion concerning which standard seems to be a better choice, under some assumptions, is provided.

- Chapter 3 addresses the acknowledge necessary to construct the NB hybrid PLC/ Wireless transceiver prototype. Firstly, an IEEE 1901.2 Standard's overview is presented, highlighting important points to comprehend this thesis, specially the PHY layer. In sequel, a description of the proposed NB hybrid PLC/Wireless transceiver is depicted, discussing its characteristics based on a systematic description of its block diagram. Afterward, the proposed IEEE 1901.2 Standard's adaptations and enhancements are stated.

- Chapter 4 addresses the prototype of the NB hybrid PLC/Wireless transceiver in an FPGA device, detailing the implementation of the IEEE 1901.2 Standard PHY layer main blocks. Moreover, the components of the prototype are specified and discussed.

- Chapter 5 covers the performance analyses. The first analysis concerns the time constraints of the Decision Maker block. A maximum data-rate analysis is presented posteriorly, contemplating all digital modulation in the IEEE 1901.2 Standard. In sequel, a hardware resource usage analysis is shown, revealing the hardware resource usage per block and also comparing the NB hybrid PLC/Wireless transceiver with the NB PLC transceiver in terms of hardware resource usage and power consumption.

- Chapter 6 states the concluding remarks of this thesis, highlighting the most relevant results and pertinent remarks regarding the whole thesis.

2 Problem formulation

To implement a hybrid PLC/Wireless transceiver which is capable of transmitting data through both PLC and wireless media, in parallel, several aspects must be addressed. One of them is the decision of which approach would be used to accomplish it. In this regard, it may be pointed out that there are four approaches to implement such kind of transceiver.

The first approach is to choose the best standards for PLC and for wireless communication, as illustrated in Figure 1. Undoubtedly, this is the best solution when performance is of utmost matter, because the most suitable standard for each medium is adopted. In this context, there are several works addressing this approach [60, 61] and, recently, Semtech Corporation announced a single-chip dual modem PLC and wireless, called EV8600 [62], which supports several PLC and wireless standards and is able, in parallel, to send information through PLC and wireless channels. This approach is the most appropriate to quickly introduce a hybrid PLC/Wireless technology in the market. However, it is worth to mention that when we are discussing a transceiver for SG and IoT applications, solutions such as the EV8600 chip may not be the best option, having in mind that these applications seek low-cost solutions for reducing price and power consumption, something that may not be accomplished by implementing two distinct standards. Also, the description provided by the manufacturer shows that cooperation at both PHY and link layer are not used.

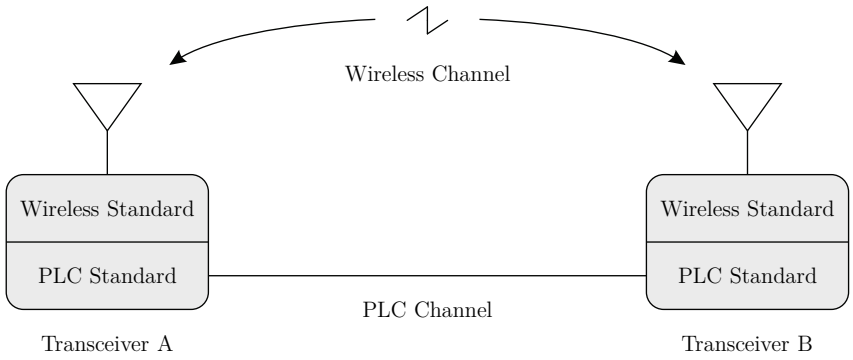


Figure 1: PLC and wireless approach.

The second approach is to develop a new standard contemplating both PLC and wireless media characteristics, as illustrated in Figure 2. This sounds to be very interesting because features from both channels can be, altogether, exploited to come up with an unique standard in the PHY and link layer. This approach is the most appropriate to design hybrid PLC/Wireless transceivers. However, there are obstacles to develop a new standard, such as the complex standardization process. Besides slow, this process requires independent implementations by third parties to validate the proposed standard. Another possible obstacle is the market acceptance, leaving the transceiver without interoperability

if it is not well-accepted. Note that the disadvantages aforementioned is much more related to acceptance than technological difficulties.

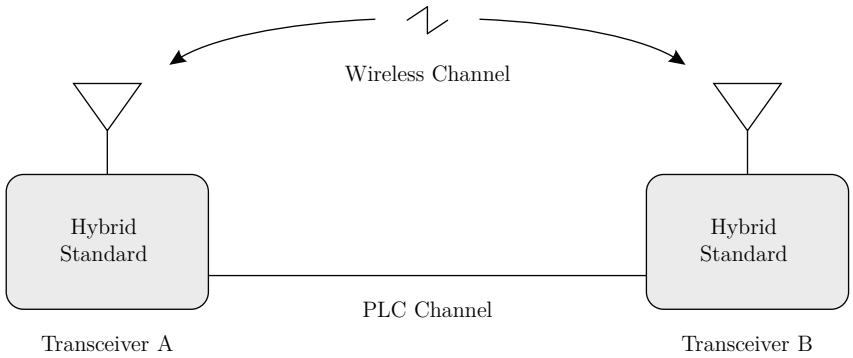


Figure 2: Hybrid approach.

The third approach is to extend a wireless communication standard to be used in both PLC and wireless media. This alternative presents drawbacks, such as the necessity of relevant adaptations for mapping of complex baseband signals of the wireless transceiver in real baseband signals of the PLC transceiver, which depending on the digital modulation scheme adopted in the wireless communication, may result in a considerable computational complexity. Besides, it will demand adjustments in the receiver. Another and, may be, the most important concern is the fact that PLC medium is considered to be worse than wireless one, consequently, applying a standard which is not robust enough for handling the hardness of PLC media could prevent the intelligent and effective usage of gains related to the existing diversity among both media for improving the data communication among nodes. This approach is shown in Figure 3.

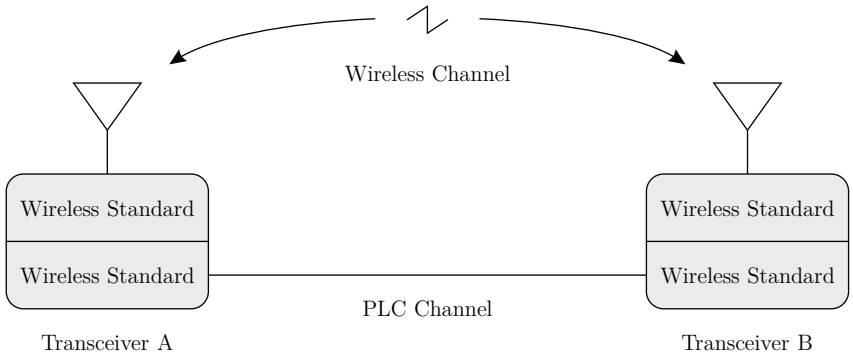


Figure 3: Wireless-only approach.

The fourth approach is to extend the use of a PLC standard to both PLC and wireless media, as shown in Figure 4. The reason for that is because PLC media are worse than wireless one in terms of signal propagation, because the presence of impulsive noises, the existence of impedance mismatching, the presence of dynamic of loads, among other issues. Due to these characteristics of electric power grids, PLC standards must be very robust. Similar to the third approach, it also presents obstacles and demands adaptations.

For instance, passband version of the PLC standard must be designed in order to transmit the signal through the wireless media. As a matter of facts, PLC channels are called as horrible channels [60]. As the hardness of PLC channel is handled by a PLC standard, than it can be advocated that its successful employment to deal with wireless channel is a great opportunity to be addressed.

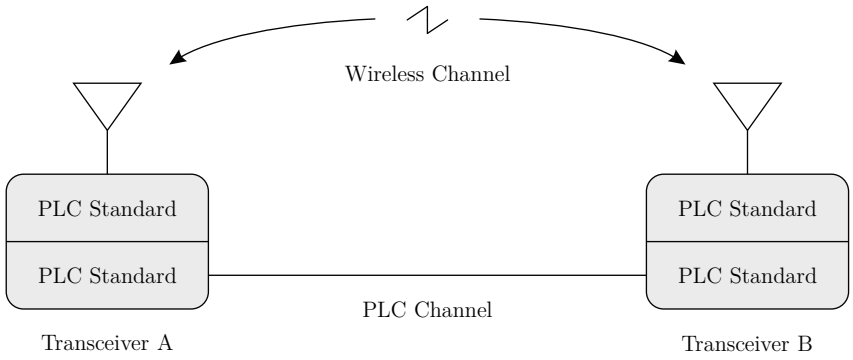


Figure 4: PLC-only approach.

Analyzing the four approaches, the fourth one seems to be an interesting choice for SGs and IoT applications. Indeed, PLC channels are hostile [60,61] and, as a consequence, the PLC standard is highly robust for providing data communication in comparison to the wireless one. In this regard, a NB-PLC standard is, in this thesis, considered for implementing the NB hybrid PLC/Wireless transceiver prototype. In other words, the thesis adopt the fourth approach.

Based on the literature, the NB-PLC technologies are based on single-carrier or multicarrier scheme. After a long monopoly of single-carrier scheme, G3-PLC and Power Intelligence Metering Evolution (PRIME), which are OFDM-based NB-PLC, came to market [63]. The multicarrier schemes offer higher data-rate, flexibility, and robustness against the hardness of PLC channels, such as frequency selectivity, which are vital for the success of SG and IoT applications. Later, it was realized the necessity of having an international PLC standard, in order to ensure worldwide interoperable products and avoid market fragmentation. With these purposes in mind, at the beginning of 2010, the IEEE Standard Association and ITU Telecommunication Standardization Sector (ITU-T) started the standardization of NB-PLC technologies based on OFDM scheme, releasing the IEEE 1901.2 Standard and ITU-T G.hnem projects, respectively. It is important to note that the USA and EU somehow introduced the market fragmentation by focusing on their own standard. It makes sense because behind the standard there is a group of companies working to introduce the standard-based technology into the market. Comparing the standards and protocols, the IEEE 1901.2 Standard is similar to ITU-T G.hnem and both add technological advances included in PRIME and G3-PLC. Furthermore, the IEEE 1901.2 Standard was designed to support SG applications, such as smart meters, electric vehicle to charging station, home area networking, and solar panel communications [6].

Also, the IEEE 1901.2 Standard offers data-rates up to 500 kbps, while ITU-T G.hnem, G3-PLC, and PRIME supports up to 1 Mbps, 208 kbps, and 130 kbps, respectively. The IEEE 1901.2 Standard is designed to work on low-voltage (LV) and medium-voltage (MV) lines and it supports data communication through transformers. Additionally, the IEEE 1901.2 Standard can interoperate with G3-PLC and PRIME. On the other hand, ITU-T G.hnem coexistence with other NB-PLC standards is under study.

Due to the fact that the IEEE 1901.2 Standard is designed to support SG applications and it can interoperate with G3-PLC and PRIME, added to the fact that IEEE's standards are well-accepted in Latin America, we considered the IEEE 1901.2 Standard to constitute the PHY layer and MAC sublayer of the proposed NB hybrid PLC/Wireless prototype. Based on this choice, the following research questions arise: *is that possible to adapt the IEEE 1901.2 Standard to make it the core data communication protocol of a NB hybrid PLC/Wireless technology? Which kind of changes must be implemented? And, most important, can it be prototyped?* Answers of these appealing research questions are presented in the following chapters.

3 The NB hybrid PLC/Wireless transceiver

The proposed NB hybrid PLC/Wireless transceiver is mainly composed of three main parts: user interface, processor, and analog front-end (AFE). Briefly, the user interface is the application which may use the transceiver for data communication, for instance, a smart meter; the processor is where all the transceiver's functionalities are implemented; and AFE provides interfaces between the processor and media (electric power grids and air).

The processor, which is the core structure of the proposed transceiver, is where the IEEE 1901.2 Standard, enhancements, and adaptations are implemented. It can be basically divided in PHY layer and MAC sublayer. More specific, the PHY layer implements all signal processing and data communication techniques to transmit and receive data. The MAC sublayer controls the transceiver, managing the access to the medium, packet error detection, among other functionalities. In order to increase the knowledge and understanding on the NB hybrid PLC/ Wireless transceiver prototype, this chapter aims to offer a detailed description of it, highlighting its most important components and techniques.

This chapter is organized as follows: Section 3.1 highlights important informations about the IEEE 1901.2 Standard, which are crucial to comprehend this thesis. Section 3.2 describes the main components of the transceiver. In sequel, Section 3.3 outlines the enhancements and adaptations. More specific, Subsections 3.3.1 and 3.3.2 present the proposed enhancements and Subsection 3.3.3 address the required adaptations.

3.1 The IEEE 1901.2 Standard

This section aims to briefly describe the IEEE 1901.2 Standard, defining its important characteristics and parameters for its implementation in a hardware. The IEEE 1901.2 Standard foresees the ability to communicate over both LV and MV electric power grids. When operating in LV electric power grids, it should also be able to communicate with nodes in the MV electric power grids and vice-versa. Due to that, the receiver must be able to detect the transmitted signal that has been severely attenuated as a result of going through a LV/MV transformer. Moreover, the IEEE 1901.2 Standard contemplates different band plans, as depicted in Figure 5, accommodating various country band regulations, such as Comité Européen de Normalisation Électrotechnique (CENELEC) [64], Association of Radio Industries and Businesses (ARIB) [65], and Federal Communications Commission (FCC) [66], which are European, Japanese, and American regulations, respectively.

In order to provide a systematic presentation of the important aspects related to the PHY layer and the MAC sublayer regarding a hardware implementation perspec-

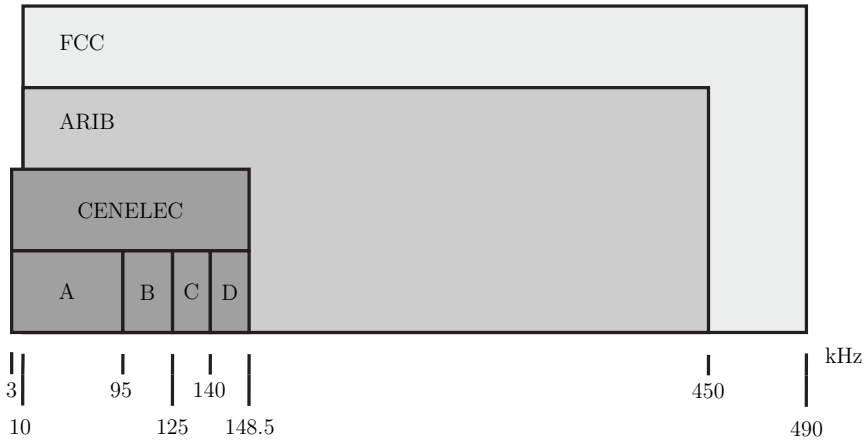


Figure 5: Regulatory frequency map

tive, Subsection 3.1.1 to 3.1.3 outlines general PHY layer informations, frame and packet structure, and channel access mechanism, respectively.

3.1.1 General information of the IEEE 1901.2 physical layer

Table 1 lists general information of the IEEE 1901.2 Standard that are relevant to the NB hybrid PLC/Wireless transceiver prototype. The band plan arbitrarily adopted in this work is the FCC, which covers the frequency band from 10 kHz up to 490 kHz.

For the FCC band plan, there are 72 subcarriers available, although, not all of them need to be used. The tone mask field in the frame control header (FCH) informs the set of subcarriers which may be used. Furthermore, the maximum number of OFDM symbols per frame that can be supported is 57, in which each OFDM symbol has 256 samples (128 subcarriers). The standard cyclic prefix (CP) length, defined by the IEEE 1901.2 Standard, is 30 samples and PLC transceivers operating in the FCC band plan may also support a long CP, which is 52 samples long. Figure 6 and Figure 7 illustrate the frame in frequency-domain and in time-domain, respectively. The data symbol and preamble symbol time intervals, which from now on will only be denoted by T_{Sym} and T_{SymPre}, respectively, is the time interval of one OFDM symbol and of one preamble sequence. The number of FCH bits per packet is fixed in 72 bits and the maximum valid bits per packet is 1912 bits, consequently, the longest packet available, according the IEEE 1901.2 Standard, is 1984 bits or 248 bytes long. It is important to mention that these parameters are concerning only with the FCC band plan with sampling frequency of 1.2 MHz. The other band plans possess different parameters, sampling frequency, and different frame structures, that will not be approached in this thesis.

The PHY layer, according to the IEEE 1901.2 Standard, can be divided into two main blocks, forward error correction (FEC) encoder and OFDM modulator in the transmitter and FEC decoder and OFDM demodulator in the receiver.

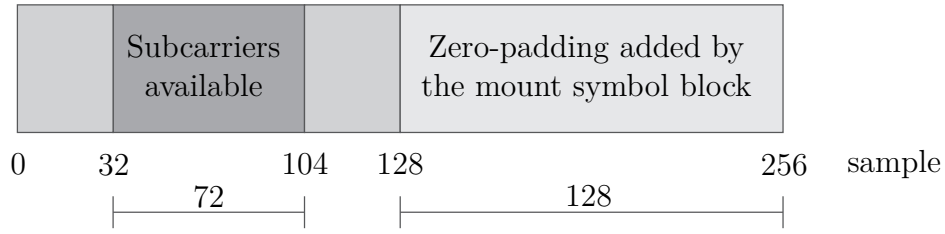


Figure 6: The OFDM symbol structure in frequency-domain.

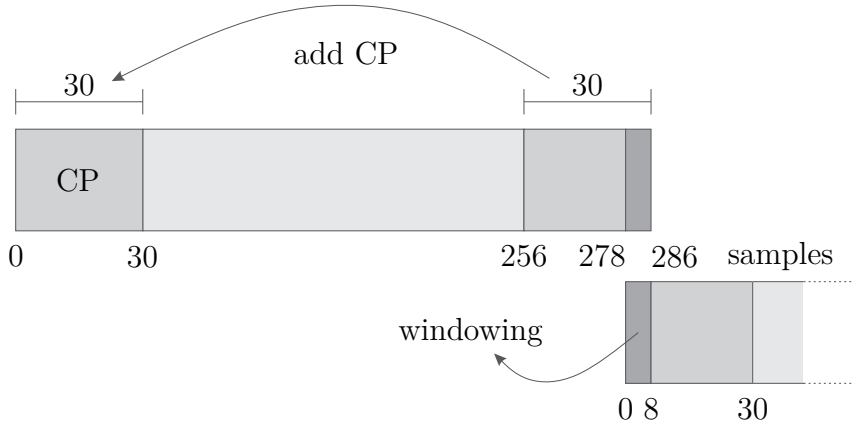


Figure 7: The OFDM symbol structure in time-domain.

The FEC encoder aims to encode the message in a redundant way, making it more robust against harsh channels. It is composed of a scrambler, which uses a polynomial to give bits an organization in the sequence of bits that avoids long sequence of zeros or ones, which has a negative impact on the channel decoding based on the Viterbi algorithm; a Reed-Solomon (RS) encoder and a convolutional code (CC), which are error-correcting codes; a repetition code (RC), which is an additional tool to protect data against impulsive noise, repeating the input bit one, four, or six times in normal, robust OFDM (ROBO), and super-robust OFDM (S-ROBO) modes, respectively; and an interleaver, which shuffles bits inside each OFDM symbol and spread OFDM symbols between each other in order to alleviate the hardness of burst of bit errors, which is the consequence of the impulsive noise occurrence and corrupt consecutive OFDM symbols, and deep fading in frequency that may corrupt adjacent frequency of several and consecutive OFDM symbols.

The OFDM modulator is responsible for encoding digital data on multiple carrier frequencies. It is composed of a digital modulator, which maps a binary message into a point belonging to one of the chosen constellations, which are listed as follows: binary phase-shift keying (PSK) (BPSK), differential binary PSK (DBPSK), differential quaternary PSK (DQPSK), differential eigth PSK (D8PSK) or other three optional schemes: quaternary PSK (QPSK), 8-PSK, and 16-quadrature amplitude modulation (QAM) digital modulation; a mount symbol, which performs zero padding to complete the OFDM symbol with the right number of samples; a inverse discrete Fourier transform (IDFT), which transforms a frequency-domain symbol into a time-domain symbol; an add CP

Table 1: General information of the IEEE 1901.2 Standard.

Parameter	**Details**
Band plan	FCC
PHY frequency band (kHz)	10 to 490
Frequency sample (MHz)	1.2
FEC encoder/decoder	Scrambler/Unscrambler, Reed-Solomon encoder/decoder, convolutional encoder/decoder, repetition encoder/decoder, and interleaver/deinterleaver
OFDM modulator/ demodulator	Modulator/demodulator, mount symbol, IDFT/DFT, reorder DFT, add/remove CP, and windowing
Repetition encoder modes	Normal, ROBO, and S-ROBO
Modulation	BPSK, DBPSK, DQPSK, D8PSK and optional QPSK, 8-PSK, 16-QAM
Cyclic prefix (samples)	30 or 52
Number of overlapped samples	8
Maximum subcarrier enable	72
Maximum OFDM symbols per frame	57
OFDM symbol length (samples)	256
Number of FCH bits per packet	72
Maximum valid bits of information per packet	1912
Time interval of one data symbol (μs)	232
Time interval of one preamble symbol (μs)	213

operation, which aims to introduce redundancy and avoid inter-symbol interference (ISI); and a windowing, which reduces out-of-band transmission of the OFDM symbol.

On the other hand, on the receiver side, the OFDM demodulator is responsible for decoding digital data on multiple carrier frequencies. It is constituted by a symbol synchronization technique, which informs the sample that starts the correct reception of

symbols, a remove CP operation, which removes the cyclic prefix; a discrete Fourier transform (DFT), which transforms a time-domain symbol into a frequency-domain symbol; a frequency domain equalization if coherent digital modulation is adopted; and a digital demodulator, which maps an estimate of the OFDM symbol, in the frequency-domain, into a binary sequence.

The FEC decoder, which is also in the receiver, is responsible for decoding the binary sequence, detecting and correcting eventual erroneous bits, under a certain capacity. It is composed of a deinterleaver, which reorders the OFDM symbols and reorganize bits inside each OFDM symbol; a RC, which eliminates the redundancy and decides which most likely bit was transmitted in case of ROBO and S-ROBO modes; a Viterbi algorithm and RS decoder, which are error-correcting codes; and an unscrambler, which reorders the bits.

3.1.2 The frame and packet structures

This section aims to describes the FCC band plan's frame structure and the packet structure in the MAC sublayer. A frame at the PHY layer is composed of a group of consecutive OFDM symbols. The FCC band plan frame structure, depicted in Figure 8, is divided in three main parts: the preamble, FCH, and PLCP Service Data Unit (PSDU), where PLCP stands for physical layer convergence protocol. Each part of the frame has its importance and function, which are described as follow:

Figure 8: The frame structure in the PHY layer.

According to the IEEE 1901.2 Standard, the preamble can be composed of 9.5 or 13.5 OFDM symbols for the FCC band plan. The first 8 or 12 symbols are identical and each of them is named SYNCP. The last one and a half symbol left is called SYNCM, as depicted in Figure 9. The SYNCP symbol is defined by the standard and has 256 samples. The SYNCM symbols are identical to the SYNCP ones except that all data in the subcarriers are π phase shifted or, in other words, each sample in the frequency-domain of a SYNCM symbol has an opposite signal of each sample in the frequency-domain of a SYNCP symbol. In the receiver, the SYNCP symbols are used for automatic gain control (AGC) adaptation, channel estimation, initial phase reference estimation, symbol synchronization, and physical carrier sense (PCS) purpose. The initial phase reference estimation is used by the FCH part, which employs a coherent demodulation and, as a consequence, it needs a reference phase to correctly demodulate the received data. The phase difference between SYNCP and SYNCM symbols is used for synchronizing the frame in the PHY layer on the receiver side, enabling the receiver to identify the frame structure.

Note that PCS is a mechanism responsible for determining the channel occupancy, in other words, if the channel is found busy or not. When the preamble part is detected by a receiver, it asserts the PCS flag high and does not allow data transmission by the node associated with this receiver, avoiding collision.

Figure 9: The structure of the preamble part.

The FCH part comes immediately after the preamble part. The length of the FCH part may vary depending upon the band plan. For the FCC band plan, the FCH length corresponds to 12 symbols. The FCH part shall be coherently demodulated using the S-ROBO mode and it has information regarding the current frame, e.g., type of frame, length of frame, the digital modulation used to transmit data in PSDU, the number of symbols for transmitting data in PSDU, among others. Due to its importance, the FCH part must be free of erroneous bits, which is verified by using a cyclic redundancy check - 8 (CRC-8). All the fields in the FCH part are shown in Figure 10. Moreover, details about each field is present in Table 2.

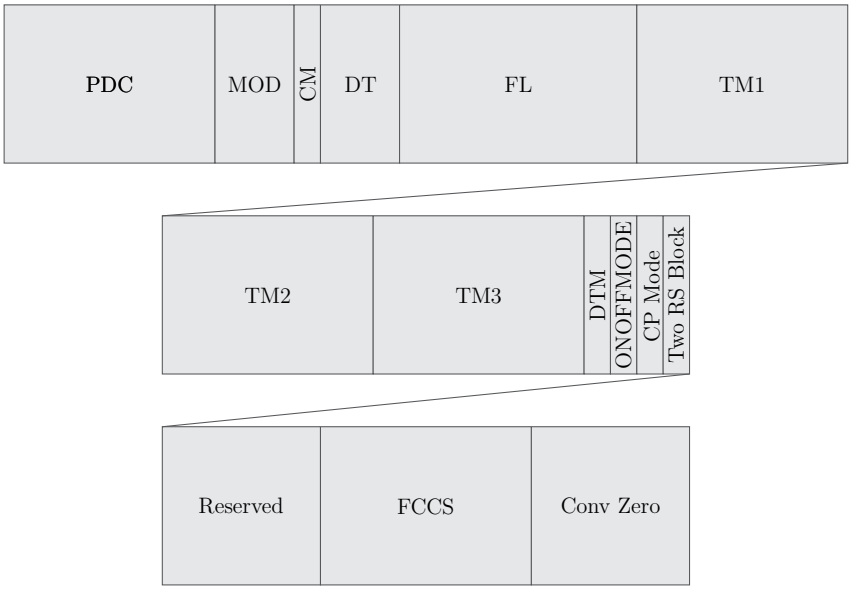


Figure 10: The structure of the FCH part.

The PLCP Service Data Unit (PSDU) data may or may not be present in the frame structure. For instance, acknowledgment (ACK) messages are only constituted by preamble and FCH parts.

Bear in mind that the PSDU part is constituted by the MAC frame, which in turn comprises a MAC header (MHR), MAC payload, and MAC footer (MFR). Note that the

Table 2: FCH fields description.

Field	Bits	Definition
PDC	8	The phase detection counter indicates that the zero-crossing detection is unsupported.
MOD	3	Indicates de modulation type: ROBO, S-ROBO, DBPSK/BPSK, DQPSK/QPSK, D8PSK/8-PSK, 16-QAM.
CM	4	The coherent mode indicates if the modulation is coherent or differential.
DT	3	The delimiter type field indicates if the frame is expecting a response or not, if the message is a positive or negative acknowledgment (ACK/NACK), or if it is a busy accept or negative busy acknowledgment.
FL	9	PSDU length in OFDM symbols.
TM1	8	The Tone Map fields define which frequencies were used during current transmission.
TM2	8	
TM3	8	
DTM	1	This field indicates if the Data Tone Mask is the same of the preamble/FCH or the indicated in the standard.
ONOFFMODE	1	It defines if the inactive sub-bands have no energy transmitted or dummy bits transmitted.
CP Mode	1	It defines if the standard CP mode or the long CP mode was used by PSDU.
Two RS Blocks	1	It defines if the transmitter is transmitting two or one RS blocks.
Reserved	6	Reserved
FCCS	8	Frame control check sequence (CRC-8).
Conv Zero	6	These bits shall be bypassed by the scrambler and only be added by the convolutional encoder.

MAC frame may be long enough to require segmentation. In this context, the original MAC frame can be replaced by several smaller MAC frames, in which the MAC payload is a fragment of the original MAC payload, see [67] for more details.

3.1.3 Channel access protocol

The channel access is accomplished by using the carrier sense multiple access/collision avoidance (CSMA/CA) mechanism (protocol) with a random backoff time [67]. This mechanism randomly spreads the transmission attempts of each node in a period of time. By reducing the probability of two nodes transmit data at the same time interval, the probability of collisions decreases. Each time a node wishes to transmit data, it waits for a random waiting time (random time interval). If the channel is found idle after the waiting time, the node may transmit its data. Otherwise, if the channel is found to be busy after the waiting time, the node may wait for another random waiting time before trying to access the channel again. If more nodes are trying to access the channel, then the probability of collision increases because the probability of two nodes draw the same random backoff time increases together. The channel occupancy is determined by PCS, which is provided by the PHY layer, as mentioned in Section 3.1.2.

The channel access by a node must be attempt at the correct time accordingly to the message priority. The IEEE 1901.2 Standard, basically, predicts three different contention window (CW), a ACK window, and two different time intervals, as depicted in Figure 11.

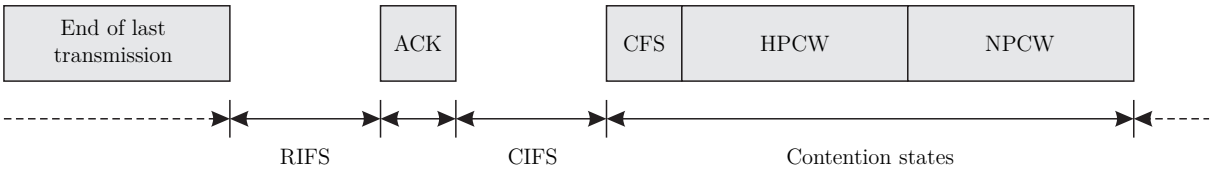


Figure 11: Priority contention Windows.

The ACK window is exclusive for acknowledge messages. As mentioned before, every ACK message is composed only of the preamble and FCH parts and due to that, the ACK window time interval can be expressed as

$$T_{ACK} = N_{PRE}T_{SymPre} + N_{FCH}T_{Sym}\ \mu s, \tag{3.1}$$

where N_{PRE} and N_{FCH} are the number of OFDM symbols used by preamble and FCH parts, respectively, while T_{Sym} and T_{SymPre} are the time intervals corresponding to one OFDM symbol and one preamble symbol, respectively, as specified in Table 1. The contention-free slot (CFS) is a time window intended to implement packet bursting without a backoff procedure, which prevents possible interruption from other nodes when a MAC frame requires fragmentation. The time interval of CFS is given by one time slot

(T_{slot}), which is expressed as

$$\begin{aligned} T_{CFS} &= T_{slot} \\ &= 2T_{Sym}\ \mu s. \end{aligned} \tag{3.2}$$

The high-priority CW (HPCW) and normal-priority CW (NPCW) are time windows intended for data communication. As the HPCW window is located before the NPCW window, nodes with high-priority message gets access to the channel before normal-priority nodes. The time interval of the HPCW is given by

$$T_{HPCW} = N_{MACHPWS} T_{slot}\ \mu s, \tag{3.3}$$

where $N_{MACHPWS}$ is a MAC sublayer parameter that defines the length of the HPCW in terms of number of slots, which by default is equal to 7. Finally, the maximum time interval for the NPCW is given by

$$T_{NPCW} = \left(2^{MAC_{MBE}} T_{slot}\right) - N_{MACHPWS} T_{slot}\ \mu s, \tag{3.4}$$

where MAC_{MBE} is the maximum value of backoff exponent, which default value is 8.

The contention interframe spacing (CIFS) time interval occurs after the end of the previous ACK message transmission, while the response interframe spacing (RIFS) time interval is the time interval between the end of the last transmission, which may covers the CFS window, HPCW, or NPCW, and the start of its association response. The CIFS and RIFS time intervals, defined by the IEEE 1901.2 Standard, are T_{CIFS} and T_{RIFS}, respectively, and correspond to the time interval associated to 10 OFDM symbols (10 T_{Sym}).

The aforementioned windows and time intervals repeat periodically during the time, which means that the ACK window is always followed by a CIFS time interval and a CFS window, HPCW, or NPCW is always followed by a RIFS time interval. It is important to highlight that only the CFS window does not execute the backoff procedure in order to prevent possible interruption from other nodes while executing packet bursting.

Finally, but not the least, to identify in which slot the data network is, each node keeps a counter, called CW counter. Each node may have its counter synchronized to the data network in order to ensure that the transceiver at the MAC sublayer level works properly. When a new node is inserted into the data network it must wait until its counter is synchronized to request a channel access.

3.2 The block diagram of the NB hybrid PLC/Wireless transceiver

The block diagram of the proposed NB hybrid PLC/Wireless transceiver prototype is shown in Figure 12. Basically, this transceiver is composed of the following three main parts:

- **User Interface:** through this interface an application is connected to the NB hybrid PLC/Wireless transceiver. This application can be a smart meter or an industrial sensor. Through this interface, the user sends and receives information from/to another device.
- **Processor:** it is where all the transceiver's functionalities are implemented, which in this case is an FPGA device. In this context, the main tasks of the processor are to provide an adequate hardware resources to implement the transceiver's logic, making available enough logic elements, memories, phase-locked loops (PLLs), among others. Also, it provides interfaces which can be used to connect external devices. By using the functionalities implemented in the processor, the incoming information from the User Interface is processed and prepared to be sent to the AFEs. Moreover, it receives frames from the AFEs, processes them, and sends the valid information to the User Interface. The processor, basically, comprehends the MAC sublayer, PHY layer, memories, and specifically designed interface blocks.
- **Analog Front-End:** it provides a highly integrated solution for data communication through PLC and wireless media. In other words, it is responsible for providing interfaces among the processor and the electric power grid and the air, inserting/extracting signals into/from these media. The AFE is constituted by analog signal conditioning circuitries which uses sensitive analog amplifiers, analog filters, digital-to-analog converter (DAC), and analog-to-digital converter (ADC).

Subsections 3.2.1 to 3.2.10 detail each component of the aforementioned parts of the proposed NB hybrid PLC/Wireless transceiver. Finally, Subsection 3.2.11 describes how the components work together.

3.2.1 Clock and PLL

The signal generated by the clock block is inserted into a PLL block of the FPGA device, which is responsible for yielding clocks with different frequencies from the original one. This variety of clocks is necessary to satisfy different requirement of processing signals in each block. For instance, the W-AFE block, see Figure 12, needs more clock cycles to process the same amount of information than the P-AFE block. Having in mind that the W-AFE and P-AFE blocks must align PLC and wireless signals in the time-domain, then the W-AFE block makes use of a higher frequency clock.

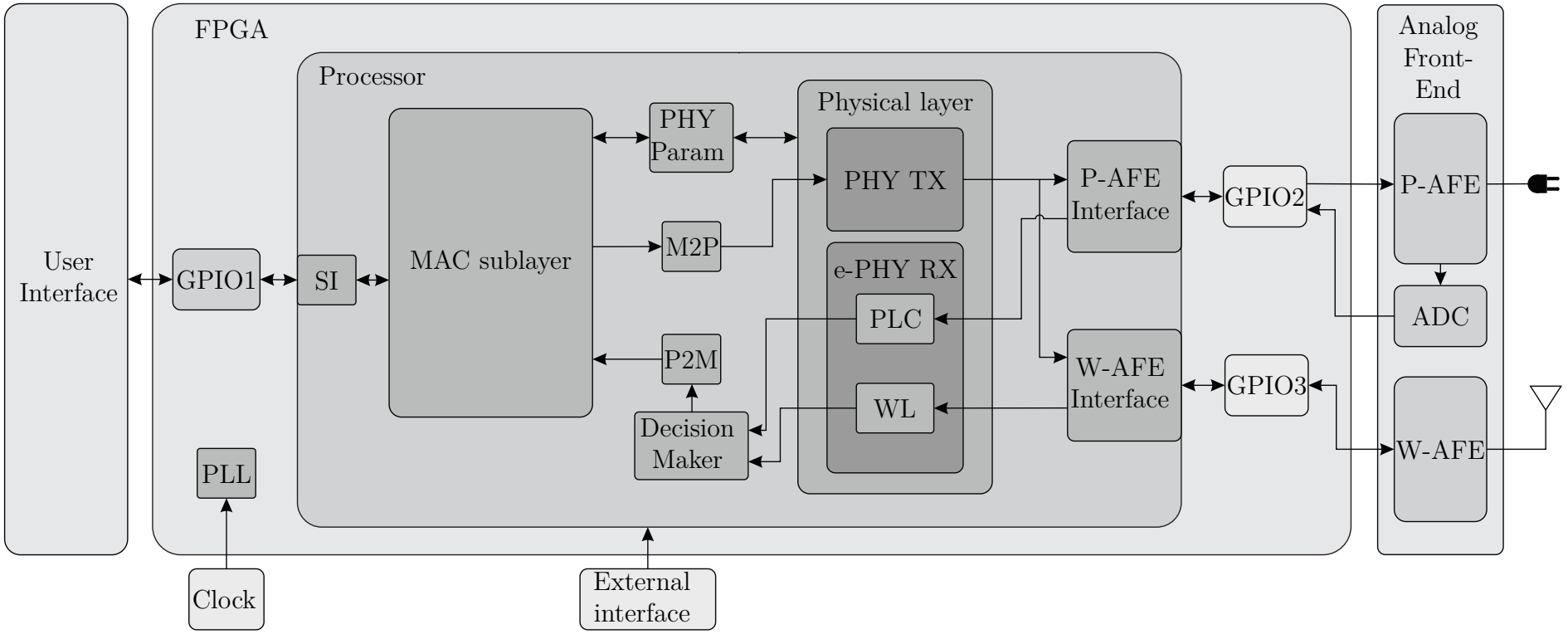


Figure 12: The block diagram of the proposed NB hybrid PLC/Wireless transceiver.

3.2.2 External interface

The External Interface block is composed of keys and switches. Each switcher has a configuration purpose. It can be used to bypass nonmandatory blocks in the PHY layer or to change a MAC sublayer configuration, for instance. The keys are used mainly for reset purpose.

3.2.3 GPIO

The general purpose input-outputs (GPIOs) blocks (GPIOi, $i = 1, 2, 3$) are used to interface the processor with an external device, such as the AFE interface and the User Interface. Each GPIO block is controlled by an interface block, located inside the processor, direct connected to digital pins of the FPGA device. The logic level of these pins values are manipulated to establish a proper data communication among the processor and external devices.

3.2.4 Serial interface

The serial interface (SI) block is responsible for sending data from the MAC sublayer to the User Interface or receiving data from the User Interface and sending it to the MAC sublayer. For the sake of simplicity, an universal asynchronous receiver/transmitter (UART) protocol is implemented. This implementation can be easily adapted to support other protocols.

3.2.5 Memories

The proposed NB hybrid PLC/Wireless transceiver was conceived to make use of the following types of memories: MAC-to-PHY (M2P), PHY-to-MAC (P2M), and PHY parameters. The M2P memory has the function of store data which comes from the MAC sublayer. Posteriorly, this memory is read by the PHY layer, which processes the received binary sequence from the MAC sublayer and enables it to be transmitted (e.g., to be sent to the AFE interfaces). On the other hand, the P2M memory follows the opposite direction, storing the binary sequence received from the Decision Maker block and, posteriorly read by the MAC sublayer. The M2P and P2M memories are able to store the longest packet supported by the IEEE 1901.2 Standard, which is 1984 bits long (or 248 bytes), as stated in Subsection 3.1.1.

The PHY Parameter memory aims to store important parameters, such as the PCS, Symbol Count, and P2M and M2P flags. The PCS parameter is read by the MAC sublayer when it is using the CSMA/CA mechanism to access the channel. The Symbol Count parameter is used by the MAC sublayer to execute the symbol synchronization. The P2M and M2P flags are responsible for informing if there is a valid packet in the

P2M and M2P memories, respectively. The P2M flag is asserted by the PHY layer when there is a packet available for the MAC sublayer and it is cleared when the packet is read by the MAC sublayer. On the other hand, the M2P flag is asserted by the MAC sublayer when there is a packet available for the PHY layer and it is also cleared after the packet is read by the PHY layer.

3.2.6 Decision Maker

The Decision Maker block is responsible for receiving the binary sequence, which were obtained from the enhanced-PHY RX (e-PHY RX). It verifies the bit error occurrences in the payload by using an error-detecting code, which is a cyclic redundancy check - 16 (CRC-16). If the binary sequence (packets) from both PLC and wireless communication are corrupted, an algorithm applies a technique to try to recover these packets and, most important, to avoid retransmission requests. Due to the importance of this block, a detailed discussion of it is presented in Subsection 3.3.2.

3.2.7 Media Access Control sublayer

The MAC sublayer controls the transceiver. Generally speaking, in any kind of transceiver, the functionalities of the MAC sublayer are multiple access, resource sharing, error detection, and traffic control. In fact, it manages the channel access. The MAC sublayer implemented in the proposed transceiver makes use of the CSMA/CA mechanism to perform channel access and also process the proposed routing protocol, see Section 3.3.1 for more details.

3.2.8 The physical layer

The PHY layer implements all signal processing and data communication techniques necessary to transmit or receive data from/to the MAC sublayer and AFE, respectively, following the IEEE 1901.2 Standard. As mentioned before in Section 3.1, it makes use of OFDM scheme, digital modulation and demodulation, FEC encoder and decoder, symbol synchronization, symbol detection, and sampling frequency correction. The frames generated in the transmitter or received by the receiver are composed of OFDM symbols. These symbols carry informations about preamble, FCH, and PSDU.

In this thesis, the transmitter part of the PHY layer process data from the MAC sublayer and its output is duplicated after the IDFT block. In sequel, one copy follows the P-AFE path while the other one follows the W-AFE path, details about it are discussed in Subsection 4.1.1. On the other hand, the receiver part of the PHY layer is duplicated to process the signal coming from the P-AFE and W-AFE. Due to the enhancements discussed in Section 3.3, the receiver part of the PHY layer is called e-PHY RX.

3.2.9 PLC and wireless analog front-end

Although AFE for PLC or wireless has its peculiarity, they are usually similar in terms of construction. In general, each AFE in the transmission path is firstly composed of a DAC, which converts discrete-time signals from the processor in continuous-time signals. An analog filter is applied posteriorly to remove out-of-band signals and, finally, they are amplified using programmable gain amplifiers (PGAs) or power amplifiers (PAs), enabling to be transmitted through PLC and/or wireless media/medium. On the other hand, in the reception path, the continuous-time signals, received from the PLC and/or wireless media/medium is firstly applied to PGA blocks, which amplify or attenuate them. Posteriorly, they are filtered to remove out-of-band signals and, finally, conditioned continuous-time signals are converted into discrete-time signals using an ADC, enabling the processor to work with them.

3.2.10 P-AFE and W-AFE interfaces

P-AFE and W-AFE interfaces are interface blocks used to receive/transmit frames from/to P-AFE and W-AFE. Both interface blocks are in charge of receiving data from the PHY transmitter (TX), encapsulate them with the AFE's protocol and send them to the intended AFE (P-AFE or W-AFE). On the opposite direction, they are also responsible for receiving data from P-AFE and W-AFE, interpreting and sending them to the e-PHY RX block.

Furthermore, these blocks allow the configuration of P-AFE and W-AFE, such as programming their analog filters, PA, PGA, desired band plan, among others.

3.2.11 The data flow

This subsection aims to describes the data flow from the transmitter node to the receiver node, in order to comprehend how the aforementioned components interact with each other, compounding the prototype of the NB hybrid PLC/Wireless transceiver.

The transmission starts in the User Interface. Through the Serial Interface, the MAC sublayer receives the packet to be transmitted. It is in the MAC sublayer that is decided which path the packet will take to reach the destination node. If the destination node is in the reachable nodes list, which is a list that enumerates which nodes can be directly reached without using cooperation of other nodes, the packet is sent directly to this node. Otherwise, the routing between nodes process will start, as described in Subsection 3.3.1.

Posteriorly, the MAC sublayer prepares the packet to be transmitted, be it an owning packet, coming from the User Interface, or a packet to be passed on (current node acting as a relay node), which is a packet generated by another node and, as a consequence,

it needs to be retransmitted by the current node. Reading the PHY Parameter memory, the MAC sublayer defines the best parameters to be used. It writes the proper parameters in FCH and the received packet in PSDU. After that, the M2P memory stores the data to be transmitted.

The PHY TX detects that there is available binary sequence (packet) to be transmitted, reading the M2P flag, and starts the data processing to generate the frames which are constituted by OFDM symbols. Posteriorly, the frame is sent to both PLC and wireless AFE interfaces.

The AFE interfaces send the discrete-time PLC and wireless signals, which is constituted by OFDM symbols, to P-AFE and W-AFE blocks. At the P-AFE and W-AFE, these discrete-time signals are digitally filtered, to ensure that the discrete-time signal is band limited. In sequel, these discrete-time signals (PLC and wireless), which are constituted by consecutive OFDM symbols forming frames, are submitted to DACs, to generate continuous-time signals (PLC and wireless) version. Finally, both continuous-time versions of discrete-time PLC and wireless signals are injected into the electric power grids and the air, respectively.

The continuous-time PLC and wireless signals are transmitted through their respective medium toward the receiver node. P-AFE and W-AFE in the receiver nodes are operating in the receiver (RX) mode, always receiving the continuous-time signals which arrive through both PLC and wireless media. In both AFEs, the received continuous-time signals are filtered and submitted to a gain, which is performed by the AGC block. After that, both continuous-time signals are submitted to ADCs, which convert the continuous-time signals into discrete-time signals and send them to the AFE interfaces.

The AFE interfaces forward the received data to the e-PHY RX, which is responsible for executing the symbol synchronization. When PLC or wireless discrete-time signal is synchronized, all the received and following OFDM symbols (frames) obtained from one medium is stored in a buffer and waits for the discrete-time signal coming from the other medium to be synchronized too. After the symbol synchronization of both discrete-time signals, PLC and wireless symbols are correctly demodulated using the information provided by the FCH part. In sequel, the data is sent to the Decision Maker block, which is responsible for checking and correcting erroneous bit under certain capacity, as described in Subsection 3.3.2. Then, the Decision Maker stores the frame in the P2M and informs the MAC sublayer that the memory contains valid information by asserting the P2M flag. The MAC sublayer reads the packet and defines if it is a packet for the User Interface or for itself, such as an ACK message. If the packet is for the User Interface, then it is sent to the SI. Finally, SI sends the valid information to the User Interface.

The receiver node must send an ACK message to the transmitter node. Due to that, the receiver node turns in a transmitter node and the transmitter nodes turns in

a receiver node. The whole process starts again to send the ACK packet, although this process starts at the MAC sublayer.

3.3 Enhancements and adaptations

This section aims to present the enhancements and adaptations implemented in the proposed prototype. The enhancements, which are the routing between nodes and the Decision Maker block are mandatory for the operation of the NB hybrid PLC/Wireless transceiver because it can remarkable increase performance in terms of reliability, having in mind that the first one may enable alternative routes to accomplish data communication among nodes that are not visible to each other and the second one tries to recovery corrupted packets received, reducing the number of retransmissions. On the other hand, the adaptation proposed is the Hilbert transform. This transform aims to recover the quadrature component of the received signal and performs carrier frequency offset estimation and correction. It is important to emphasize that the enhancements and adaptations are introduced in a way to guarantee compliance with the IEEE 1901.2 Standard. In other words, nodes with PLC and PLC/Wireless transceivers can operate (communicate with each other) in a PLC/Wireless data network.

3.3.1 Routing node process

The routing node process is a MAC sublayer feature that is incorporated in the IEEE 1901.2 Standard. This feature enables any node to work as a relay node, retransmitting packets, which is not addressed to the current node, for destination nodes in the data network that is two hops, at least, from the source node. Generally, these node relay constitute alternative paths for accomplishing data communication among nodes that are not visible to each other (e.g., are not one hop far from each other). In other words, the packet from the source node cannot reach the destination node with one hop. These nodes are called unreachable nodes, because the table of reachable nodes only cover nodes that are one hop of distance. This feature rises the data network reliability, having in mind that it increases the success of communications among nodes that are more than one hop of distance. It also offers more data network flexibility, enabling it to adapt easily to adverse scenarios.

The routing node process starts when a node, called node A, identifies that it needs to send a packet to an unreachable node, called node B, which is located at least two hopes far from the node A. A routing request (RREQ) message is broadcast and this message is resent to all nodes in the data network until it reaches node B. The node B identifies that the broadcast message is directed to it and generates a routing reply (RREP) message. The RREP message is sent in unicast through the reverse route built by the RREQ message, which means that in each node the message is fed back to

the node that originated the RREQ message. When the RREP message reaches node A, the route between nodes A and B is traced. After node A receives the RREP message, it sends a RREP acknowledge (RREP-ACK) to node B to ensure that the route was built correctly and certify that it is bidirectional. Only after the end of this procedure the packet can be sent from node A to node B using relay nodes. It is important to mention that the route between A and B remains stored and this process is only executed once.

3.3.2 Decision Maker block

The Decision Maker block, which is a block included between the PHY layer and the MAC sublayer (see the block diagram in Figure 12), implements a technique that is capable of recovering corrupted packets received from PLC and wireless channels. Basically, it verifies the occurrence of erroneous bits in the payload, which is the content of the PSDU part, by using an error-detecting code. Although other error-detecting code can be used, the CRC-16 was chosen due to its efficiency, simplicity, the number of bits that it can protect, and mainly because it is part of the IEEE 1901.2 Standard. As a matter of fact, the idea is to ensure full compatibility among hybrid and non-hybrid transceiver in a data network.

Figure 13 depicts the flowchart of the tasks performed by the Decision Maker block. According to this flowchart, if both PLC and wireless frames are correctly received, it is highly probably that they are the same frame originated by the source node. If just one of them is received correctly, this one is sent to the MAC sublayer and the other discarded. And, finally, if both of them are received with erroneous bits, then a technique, proposed in [68], will be applied to correct them.

The bit error correction technique compares both payloads from the frames received from PLC and wireless media and it detects the bits that are different in each payload. The possible erroneous bits are the bits which, in the same bit position, are different in each payload. After detecting the possible erroneous bits and its positions in the payload, all possible combinations to correct the payload will be listed. For instance, if two erroneous bits are detected, there are three possible combinations of two bits that will replace the erroneous bits to correct the payload. If three erroneous bits are detected, there are seven possible combination of three bits to be tested. Generalizing, the number of combinations to be tested is equal to $2^N - 1$, where $N \in \mathbb{N}^+$ is the number of erroneous bit. After the list is completed, each combination is replaced in its bit position and the CRC-16 is tested. If the test works, the payload is corrected and the process is ended. If all combinations are verified and the payload is not correctly recovered, it is possible that different payloads are being compared or that at least two bits, one in the PLC payload and the other in the wireless payload, in the same bit position are erroneous. In this last case, the erroneous bit will not be detected, because they will hold the same value at

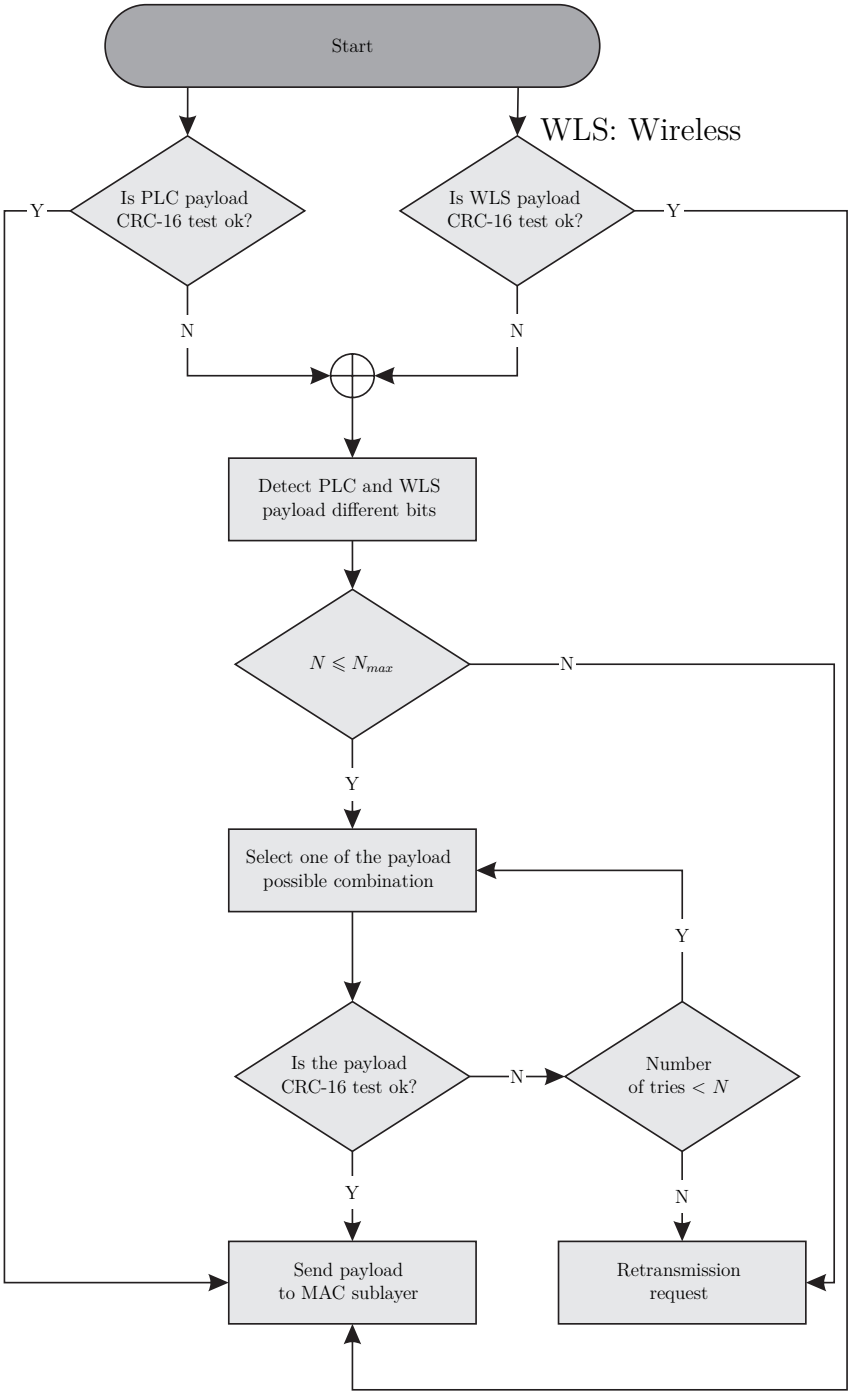


Figure 13: Decision maker block flowchart.

the same bit position in each payload. Furthermore, it is important to mention that this technique should only be used if the number of erroneous bits is lower than a predetermined value ($N_{\max} \in \mathbb{N}^+$), having in mind that with more bits, exponential time interval is spent trying to obtain the error free payload. In fact, if it takes a long time to perform this technique, the payload information may not be more relevant to the receiver due to end-to-end delay constraint. In this case, a retransmission request (automatic repeat request (ARQ) message) is sent instead of using $N > N_{\max}$.

According to [68], this technique is capable of reducing the number of retransmission request from the receiver, having in mind that a long number of corrupted payloads can be recovered at the receiver side without the need of sending a ARQ message to the transmitter. With a lower number of ARQ messages, the channel access will be disputed by less nodes because, in the majority of the cases, only nodes with new data to be transmitted will be requesting the use of the data network resource, consequently the probability of collision decreases, as verified in [68], and the data network throughput increases.

3.3.3 The Hilbert transform

The Hilbert transform, implemented in the PHY layer, is an important adaptation proposed in this work. It is composed of a digital filter, called Hilbert filter [69], a multiplier j block, where j is the symbol for complex numbers, a sum operation, and a multiplier operation. The Hilbert transform block diagram is depicted in Figure 14. Note that $\mathbf{x} \in \mathbb{R}^{N\times 1}$ is the input vector, $\check{\mathbf{x}} \in \mathbb{R}^{N\times 1}$ is the Hilbert transform of vector $\mathbf{x}$, and $\mathbf{f} \in \mathbb{C}^{N\times 1}$ is the sum of the input vector $\mathbf{x}$ and $j\check{\mathbf{x}}$. Note that $\mathbf{k} \in \mathbb{C}^{N\times 1}$ is the multiplication of $\mathbf{f}$ and $\mathbf{u} \in \mathbb{C}^{N\times 1}$, where $\mathbf{u}$ executes a frequency shifting and the variable $\Delta\Omega_C$ in $\mathbf{u}$ is the carrier frequency offset. For more details, see [70]. Finally, $\mathbf{y} \in \mathbb{R}^{N\times 1}$ is the real part of $\mathbf{k}$.

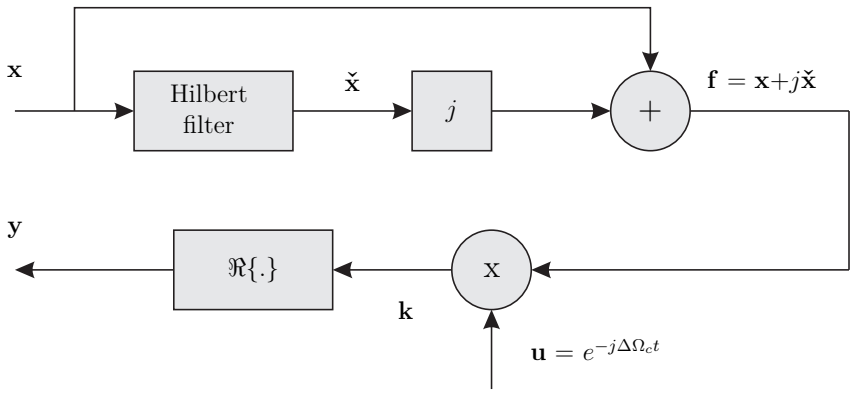


Figure 14: Hilbert transform block diagram.

This transform is the first block of the e-PHY RX. It receives a real discrete-time signal in time-domain, or vector $\mathbf{x}$, and outputs a real discrete-time signal, or vector $\mathbf{y}$, also in time-domain.

The main function for using the Hilbert transform is to the recovery of in quadrature components of the preamble associated with the signal coming from the PLC or wireless interface, which allows to estimate the frequency deviation of the received signal. Posteriorly, this estimation is used to correct the in phase component of the received signal, which allows to extract the frame more precisely, and, as a consequence, providing

better estimative of the OFDM symbols to the digital demodulator, avoiding errors in the mapping process.

4 Prototyping the NB hybrid PLC/Wireless transceiver

This chapter focuses on the construction of the the NB hybrid PLC/Wireless transceiver prototype, detailing the implementation in an FPGA device and presenting the main components. In this regard, the implementation of the PHY layer described in the IEEE 1901.2 Standard using a hardware description language (HDL) is approached, detailing the connections between each block and their functions on the transceiver. Furthermore, the Avalon interface from the chosen FPGA device, used for data control, is introduced and elucidated, highlighting its main features.

Overall, this chapter presents the implementation of the main components that constitute the NB hybrid PLC/Wireless transceiver prototype, which are the processor, P-AFE, and W-AFE. The processor is implemented in an FPGA device, which was specified for processing all the IEEE 1901.2 Standard at the PHY layer and MAC sublayer levels. While P-AFE is based on the AFE032 chip, which is capable of receiving and transmitting data from/to electric power grid supporting different band plans and standards, the SX-1257 chip was chosen to implement the W-AFE, which enables the data communication through the wireless medium.

This chapter is organized as follows: Section 4.1 describes the transceiver implementation in an FPGA device. More specific, Subsection 4.1.1 presents the PHY layer implementation and Subsection 4.1.2 addresses the data control interface adopted. Finally, Section 4.2 presents the components of the NB hybrid PLC/Wireless transceiver prototype.

4.1 FPGA implementation

This section has the purpose to describe the implementation of the NB hybrid PLC/Wireless transceiver prototype in an FPGA device. To implement the logic of each block, a Verilog language, which is an HDL [71], is used, with exception of the MAC sublayer. This language, commonly used to model electronic systems, is chosen because it provides flexibility for the programmer to describe exactly how the circuit must behave. This language also allows the programmer to extract the best feature of the FPGAs: the parallel processing. It means that each implemented logic is running in parallel with all the others, something that is different in microcontrollers because the processing is sequentially executed or with a reduced level of parallelism when structure takes place. As a result, FPGA devices possess a great power of data processing capacity. The MAC sublayer is totally implemented in a Nios II processor [72]. Note that the Nios II is a very versatile soft processor developed by Altera, due to its flexibility, high performance, and low hardware cost. To integrate the MAC sublayer and PHY layer, the Qsys system integration tool is used [73]. This tool simplifies the interconnecting logic between the

PHY layer, MAC sublayer, M2P, P2M, and PHY parameter memory, saving design time and avoiding possible mistakes.

For the sake of simplicity, this section is divided into two subsections. Subsection 4.1.1 aims to depict the PHY layer implementation, illustrating the bus width between each block in the transmitter, while Subsection 4.1.2 approaches the control data standard used in both PHY layer and Qsys tool.

4.1.1 Physical layer implementation

Figure 15 illustrates the bus length used to connect each block from the M2P memory towards the P-AFE and W-AFE in the transmitter. The PHY TX is mainly composed of a FEC encoder and an OFDM modulator, for more details, see Subsection 3.1.1. Also, it is composed of a Signal Conditioning block, which is responsible for receiving data to be transmitted, storing it, applying a gain if necessary, and sending it properly to each AFE.

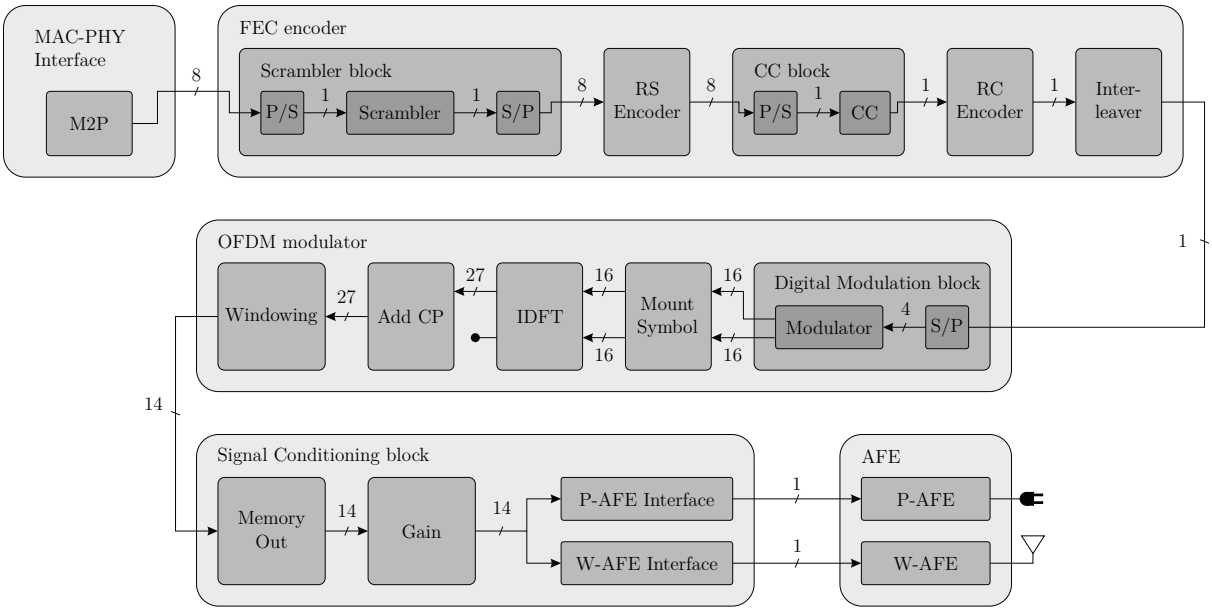


Figure 15: PHY TX FPGA implementation.

For the sake of simplicity, this explanation will follow the data flow shown in Figure 15, which begins in the M2P memory and ends in the AFEs. The data flow begins when the M2P flag is asserted by the MAC sublayer and the FEC encoder starts to read each byte from the M2P memory. At a first step, the data is serialized by the Scrambler block, using a parallel-to-serial (P/S) block, enabling the data to be processed using the Scrambler's polynomial. Posteriorly, the data is parallelized again forming words of eight bits or one byte, using a serial-to-parallel (S/P) block, allowing it to be inserted into the RS encoder. Afterward, the RS encoder's processing, the data is introduced in a P/S block before it is inserted into the CC block. The CC sends its processed data using a

1-bit bus to the RC encoder, which in turn also sends its processed data to the Interleaver using a 1-bit bus.

The OFDM modulator receives data through the 1-bit bus from the FEC encoder. This bus is connected into a S/P block, which gathers bits in group of four, using a 4-bits bus transmits words to the digital modulator. The digital modulator maps a binary sequence into a complex signal, resulting in two output values, one real and the other imaginary, with 16 bits of word width each. These two 16-bits words are sent to the Mount Symbol block, which only accomplish the zero-padding operation to properly complete the OFDM symbol, keeping the bus word width unchanged. In a next step, the two 16-bits buses are connected to the IDFT block, which processes the signal and outputs two 27-bits discrete time-domain signals. Only the real 27-bits time-domain signal bus is inserted into the add CP block and posteriorly in the Windowing block.

The Signal Conditioning block only stores the 14 most-significant bits (MSBs) from the OFDM modulator in the Memory Out, aiming to save resources, having in mind that the DAC used in AFEs only accept words of this width. A 14-bits bus is connected to the Gain block, which rescales the signal if necessary to use signal full-scale amplitudes and outputs 14-bits words to be sent to the P-AFE and W-AFE interfaces. Both P-AFE and W-AFE interfaces serialize the signals and send to the AFEs each one using its proper serial communication protocol. Finally, P-AFE and W-AFE receive the discrete-time signal to be transmitted, convert them into continuous-time signal, and injected them into the electric power grid and the air, respectively.

On the other hand, Figure 16 shows the bus length used to connect each block from P-AFE and W-AFE towards the P2M memory in the receiver. Note that, the e-PHY RX is mainly composed of an OFDM demodulator and a FEC decoder. Furthermore, it is also composed of a Signal Processing block, which is responsible for receiving data from AFEs, recovers the signal component in quadrature using the Hilbert transform, and for performing the symbol synchronization.

The data flow in the receiver starts when both continuous-time signals from the PLC and wireless media are received. The P-AFE and W-AFE interfaces receive discrete-time signal from each respective AFE and interpret it using their serial communication protocol. Posteriorly, the discrete-time version of the received signal is sent to the Hilbert transform block using a 14-bits bus, which in turn recovers the signal component in quadrature. In that way, the PLC and wireless synchronism block receive two 14-bits buses each from their respectively Hilbert transform, one bus for in phase component and another one for in quadrature component. The synchronism block performs its processing techniques using both in quadrature and in phase components and detects the synchronism point. Then, the valid information is extracted from the received data and sent to the OFDM demodulator using two 14-bits buses, one for each channel.

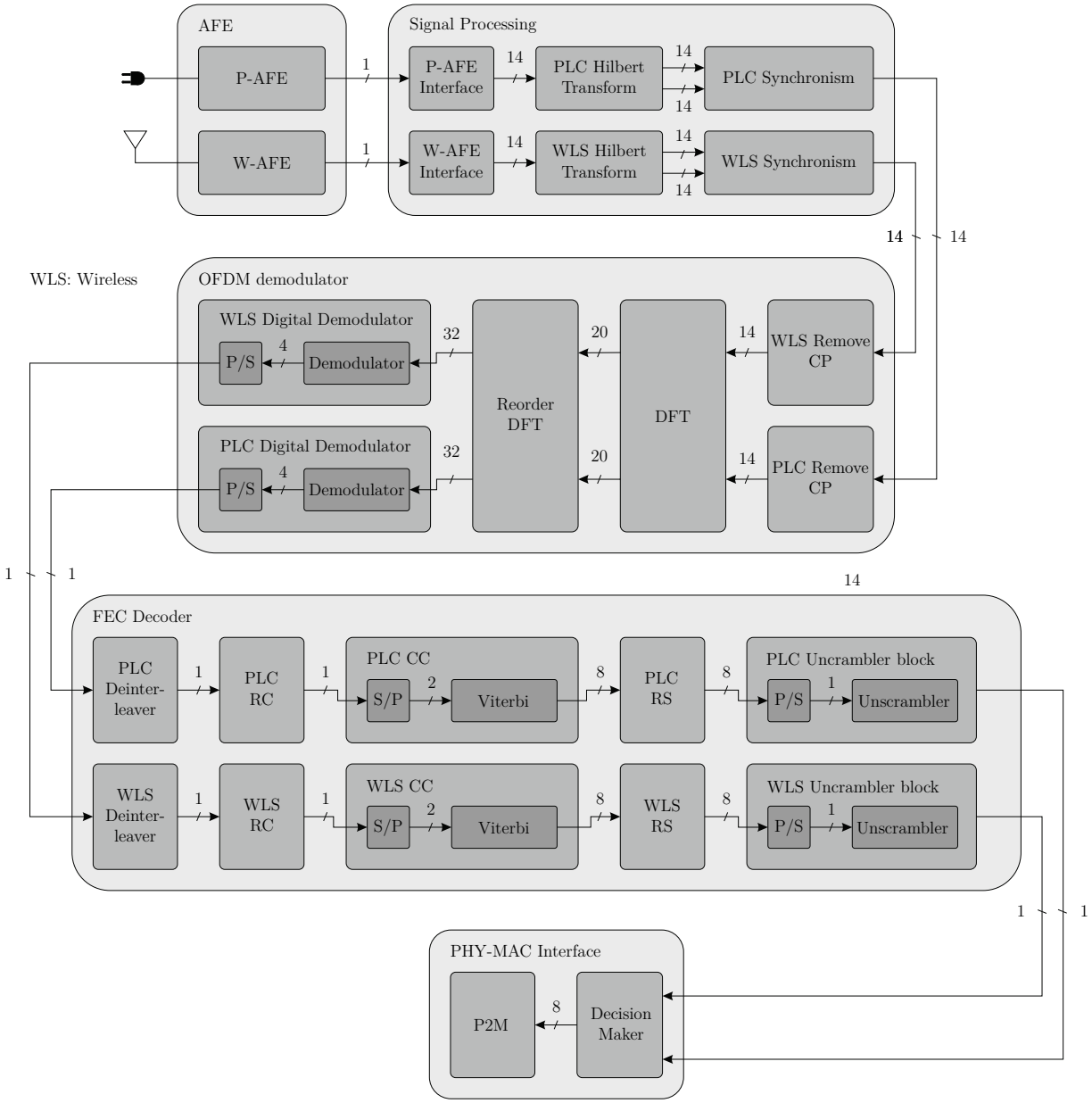


Figure 16: e-PHY RX FPGA implementation.

The OFDM demodulator receives bits through two 14-bit buses and inserts them into the remove CP block, which is responsible for removing the cyclic prefix. Afterward this processing, each remove CP block outputs 14-bit words, which are sent to the DFT block. In order to save resource, a technique is utilized, using a single DFT to transform the PLC and wireless time-domain signals into frequency-domain signals. To perform that, the PLC's 14-bit bus is inserted in the real input and the wireless' 14-bit bus is introduced in the imaginary input. After its processing, the DFT outputs two discrete-time signals in the frequency-domain with 20-bits each. At this point, the frequency-domain PLC and wireless signals are mixed. Due to that, these two buses are introduced in the Reorder DFT block, which is responsible for separating the PLC and wireless frequency-domain signals. This block uses two 32-bit buses, one for each channel, to transfer data and

these buses are inserted into two digital demodulators. Each digital demodulator receives the signal and detects a estimated version of the sent message. Having in mind that the largest constellation available is 16-QAM, which needs 4-bits to represent each of its constellation points, a 4-bit word is used. Thereafter, the P/S block serializes the binary sequence constituted by the FCH and PSDU parts and sends it to the FEC decoder block using two 1-bit buses.

The FEC decoder block receives these two binary sequences from the OFDM demodulator and introduces each in the Deinterleaver block, which in turn outputs a 1-bit word that is sent to the respective RC block. Posteriorly, each RC block outputs a 1-bit word, which are sent to the CC block. These 1-bit words are parallelized, generating two 2-bits words, then they are sent to the Viterbi block, which is responsible for performing channel decoding. After the Viterbi algorithm carried out, each one outputs an 8-bit word, which are directly sent to the RS block. Finally, each RS block also outputs two 8-bit words to be sent to the Unscrambler block. Before the bits be received by the Unscrambler block, it is serialized and then each Unscrambler block outputs a 1-bit word, finishing the FEC decoder processing.

The two 1-bit words from the FEC decoder are received by the PHY-MAC interface. These two 1-bit buses inputs are directed to the Decision Maker block, which checks the data integrity and outputs an 8-bit word after its processing, respecting the conditions detailed in Subsection 3.3.2. The 8-bit word is sent to the P2M memory and the P2M flag is asserted to inform the arrival of a new packet to the MAC sublayer.

It is important to mention that in both PHY TX and e-PHY RX, the trade-off between hardware resource usage and data quantization were analyzed to determine each bus width.

4.1.2 Data control standard

This subsection aims to present the interface used for data control. The Avalon interface [74] is chosen due to its simplicity and easiness of use. This interface simplifies system design by allowing the easy connection of its components. The PHY layer blocks uses this standard interface, as the MAC sublayer and memories, enhancing and facilitating the interoperability of the components of the processor inside the FPGA device.

There are seven different Avalon interfaces, which are listed as follows:

- Avalon Streaming (Avalon-ST) interface.
- Avalon Memory-Mapped (Avalon-MM) interface.
- Avalon Conduit interface.

- Avalon Interrupt interface.
- Avalon Clock interface.
- Avalon Reset interface.
- Avalon Tri-State Conduit (Avalon-TC) interface.

Only the last interface is not used in the NB hybrid PLC/Wireless transceiver prototype. The first six are used by the Qsys tool to integrate the PHY layer, MAC sublayer, and memories. More specifically, the first two are extensively used in the PHY layer. The Avalon-ST interface is used for data control between each block and the Avalon-MM interface is used to connect the PHY layer with the M2P and P2M memories. Due to that, only these two interfaces are discussed. For more details about the others Avalon interfaces, see [74].

4.1.2.1 Avalon Streaming interface

The Avalon-ST interface is a complete interface which provides low latency and high throughput. This interface also affords several optional control signals which may or may not be used, depending on the system requirements. This subsection will only aboard the signals utilized in the transceiver, for more details about the other control signals, see [74].

Basically, the interface is composed of sink and source connections. When two components using an Avalon-ST interface are connected, the data flows from the source to sink interface. Table 3 describes the signals which composes the Avalon-ST interface used in data control of the NB hybrid PLC/Wireless transceiver prototype and Figure 17 illustrates an Avalon-ST interface with an N-bit data word width.

Table 3: Avalon-ST interface signals role.

Signal name	Direction	Description
data	Source $\rightarrow$ Sink	The data signal from the source to the sink carriers the information being transferred.
ready	Source $\leftarrow$ Sink	Asserted high to indicate that the sink can accept data. The source may only assert *valid* and transfer data during *ready* cycles.
valid	Source $\rightarrow$ Sink	Asserted by the source to indicate that valid data are being transferred from source to sink. Data transferred out of *valid* cycles are ignored by sink.

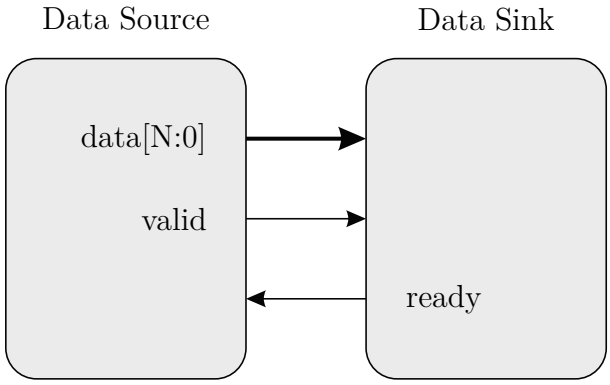
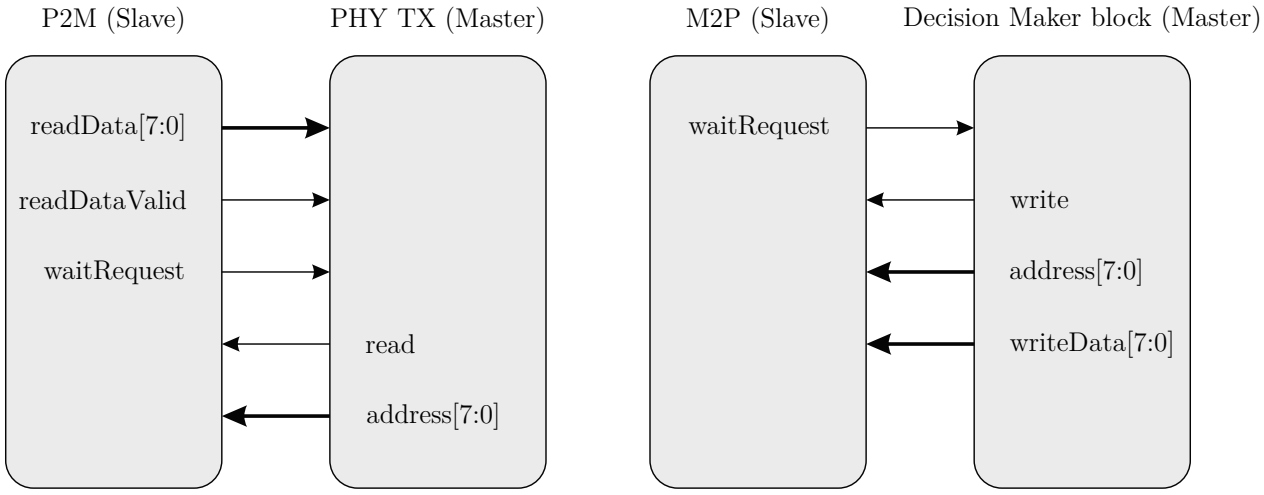


Figure 17: Avalon-ST interface.

4.1.2.2 Avalon Memory-Mapped interface

Avalon-MM is an interface used to implement read and write operations for master and slave components. Generally, a slave component is a microprocessor, memories, timer components, between others. The PHY layer of the NB hybrid PLC/Wireless transceiver prototype is only connected to memories, which are the M2P and P2M memories. These memories behave as slaves while the PHY layer and the MAC sublayer as masters.

Similar to the Avalon-ST interface, the Avalon-MM is a complete interface for the purposes aforementioned and due to that presents a lot of control signals, although just a few of them apply in the transceiver's context. Due to that, only the used control signals are described in Table 4. See [74] for more information about this interface. Figure 18(a) and Figure 18(b) illustrate the two applications of the Avalon-MM in the NB hybrid PLC/ Wireless transceiver prototype.



(a) Transmitter direction.

(b) Receiver direction.

Figure 18: Avalon-MM interface.

Table 4: Avalon-MM interface signals role.

Signal name	Direction	Description
address	Master → Slave	In reading operations, this signal indicates which address is being read and in writing operations this signal indicates which address is being write.
read	Master → Slave	Asserted to indicate a read transfer.
readData	Master ← Slave	This signal driven from the slave to the master in response to a *read* flag.
readDataValid	Master ← Slave	When asserted, indicates that the *readData* stream contains valid data.
write	Master → Slave	Asserted to indicate a write transfer.
writeData	Master → Slave	This signal driven from the master to the slave in response to a *write* flag.
waitRequest	Master ← Slave	Asserted by the slave when it is unable to respond to a *read* or *write* request. Forces the master to wait until the interconnect is ready to proceed with the transfer.

4.2 The NB hybrid PLC/Wireless transceiver prototype

This section describes the components which comprehend the transceiver prototype, see Figure 19. As can be seen in the picture, the setup is composed of two NB hybrid PLC/Wireless transceiver prototypes, which in turn is mainly composed of a processor, P-AFE together with ADC, and W-AFE, which are highlighted in the picture by the numbers #1 to #4, respectively.

4.2.1 Processor

The processor is the main block of the proposed transceiver, which is implemented in an FPGA device. The EP4CE115F29C7 [75] FPGA chip from Cyclone IV family, designed by Altera, was chosen because it offers enough resources to implement the proposal prototype. In fact, this chip has 114,480 logic elements (LEs), 432 M9K memory blocks, 3,888 Kbits embedded memory and 4 PLLs blocks.

An external crystal of 50 MHz with 20 ppm is connected to the FPGA device and it is responsible for providing the transceiver's source clock. Using the PLL blocks, five different frequency clocks are generated: 19.2 MHz for the PHY layer and the MAC sublayer, 36 MHz for the W-AFE, 37.5 MHz and 24 MHz for the P-AFE's DAC and the serial peripheral interface (SPI) protocol, respectively, and 1.2 MHz which is used for sampling the continuous-time signals, complying with the Nyquist theorem.

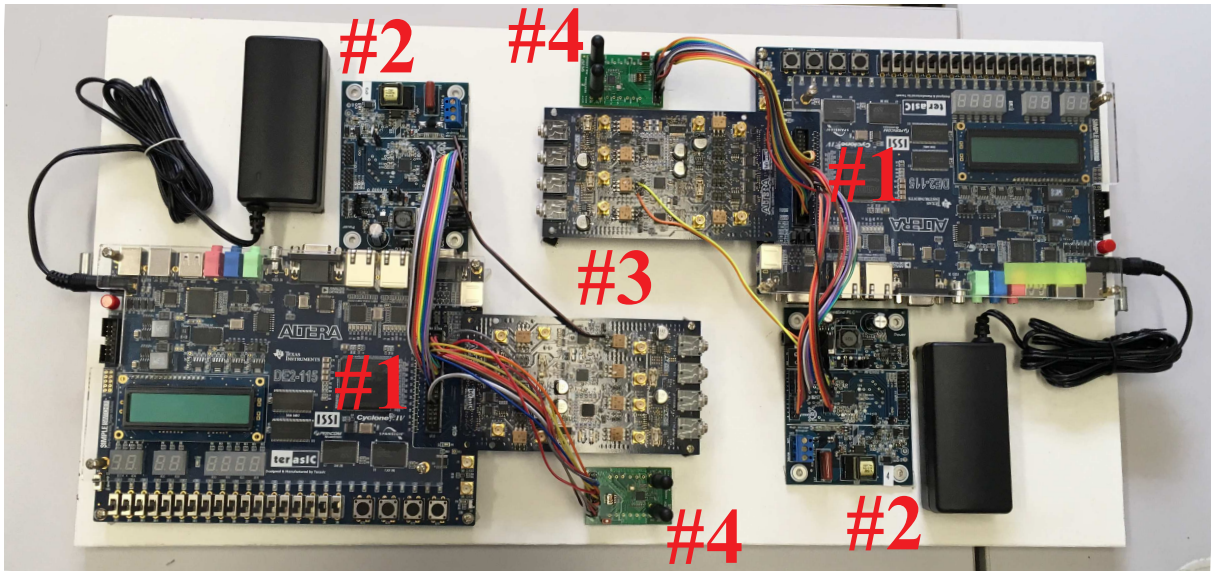


Figure 19: Setup of the NB hybrid PLC/Wireless transceiver prototype.

4.2.2 The PLC analog front-end

In this prototype, P-AFE is based on the AFE032 chip [76]. The AFE032 chip is a low-cost, integrated, and half-duplex AFE device for PLC transceiver that is capable of receiving and transmitting data from/to electric power grids. The AFE032 chip is totally controlled by the FPGA device. The AFE032 chip supports CENELEC A, B, C, and D, ARIB, and FCC band plans. Also, it complies with G3-PLC, PRIME, IEEE 1902.1, and ITU-G.hnem Standards. Figure 20 depicts the P-AFE based on the AFE032 chip.

In the transmission path, the device is composed, firstly, of a DAC, which is responsible for receiving the discrete-time signal from the FPGA device and converting it into a continuous-time signal. The following block is a PGA, which can be programmed to introduce a gain in the continuous-time signal. A programmable bandpass filter comes next, which must be properly designed in accordance with the used band plan desired, in this work, the FCC band plan. Finally, the last block is a PA, also programmable. The PGA and PA blocks must be programmed to provide an appropriate gain to the continuous-time signal taking into account the distance between the transceivers. The farther the destination node is, the greater the amplification gain must be. The continuous-time signal is injected through a narrowband, capacitive, single-input single-output (SISO), and low-voltage PLC coupling circuit, located outside the AFE032 chip into the electric power grids. It is important to mention that the coupling circuit is basically constituted by a transformer, which provides galvanic isolation between electric power grids and AFE [8].

On the other hand, in the receiving path, the continuous-time signal is received from the electric power grid through the PLC coupling circuit, identical to that used in the transmission path. Posteriorly, the signal at the output of the PLC coupling circuit

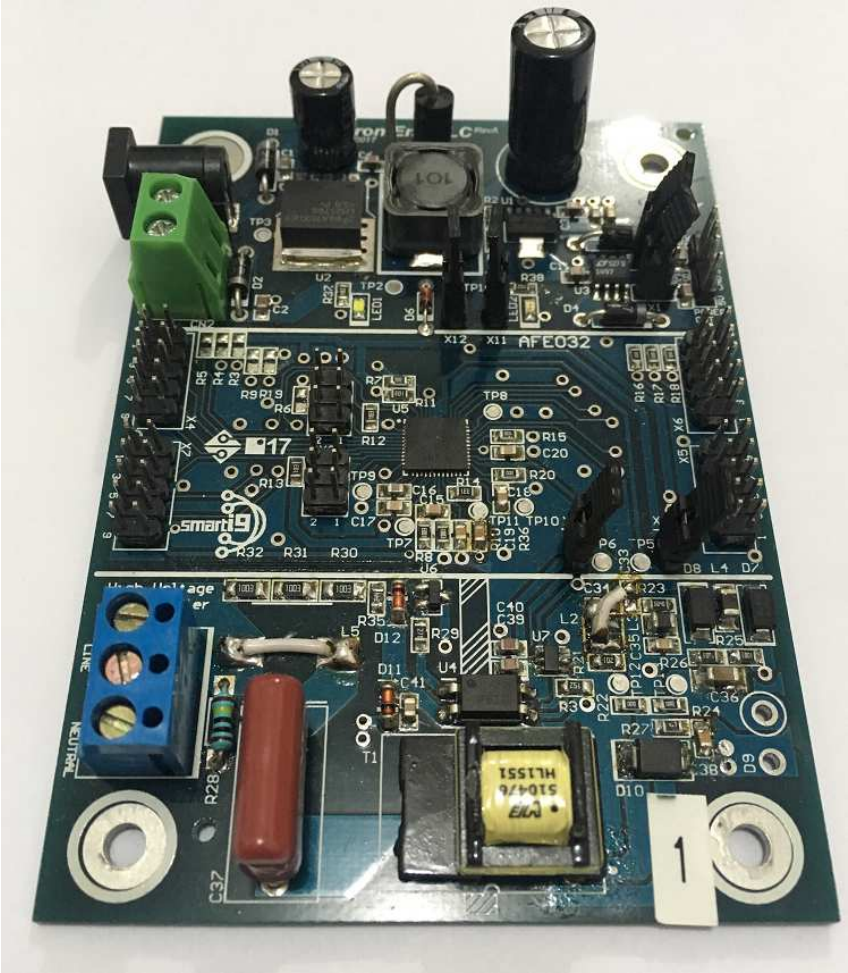


Figure 20: PLC analog front-end.

is filtered by a bandpass filter which removes unwanted out-of-band signals. After that, inside the AFE032 chip, the continuous-time signal is inserted into a PGA block, which is programmable and capable of providing gain or even attenuation to the continuous-time signal. Configuring the PGA as an attenuator is useful for applications in which large interference signals are presented within the signal band. The next block in the receiver path is the programmable bandpass filter, which, as well as in the transmission path, must be programmed according to the used band plan. After that, another PGA block is included. The continuous-time signal at the output of the last PGA block is submitted to an ADC, located outside the AFE032 chip. The arbitrarily chosen ADC is AD9254 [77], which is a monolithic, single 1.8 V supply, 14-bits, 150 Msps ADC, featuring a high-performance sample-and-hold amplifier. This external ADC converts the continuous-time signal into a discrete-time signal. After the conversion, the discrete-time signal is sent to the FPGA device.

4.2.3 The wireless analog front-end

Regarding the wireless branch, the choice of the AFE device for W-AFE was in favor of the SX-1257 chip [78]. The SX-1257 is designed to operate from 862 MHz to 960 MHz frequencies. Its highly integrated architecture demands a minimal of external components whilst maintaining maximum design flexibility. All major radio frequency (RF) communication parameters are programmable and most of them can be dynamically set. For instance, it allows narrowband (single carrier or multicarrier) communication modes without the need to modify external components. This chip satisfies the European Telecommunications Standards Institute (ETSI), ARIB, and FCC band plans. Furthermore, the SX-1257 chip is optimized for low power consumption while offering the provision of high output power. The SX-1257 chip can operate in half or full-duplex mode. Similar to P-AFE, the FPGA device controls the SX-1257 chip. Figure 21 illustrates the W-AFE.

Figure 21: Wireless analog front-end.

The transmission path is mainly composed of two DACs, which receives the in-phase and in quadrature discrete-time signal from the FPGA device and convert them into two continuous-time signals. After that, the signals are filtered by two lowpass filters, which smooth the signals and remove quantization noise generated by the DACs. In sequel, the RF carrier frequency signal is mixed with the continuous-time baseband signal. In this stage, a programmable gain can also be applied. Posteriorly, the continuous-time passband signal is inserted into a PA, which provides at its outputs two amplified version

of the signals at its inputs. These two amplified signals are inserted in the RF antenna to be transmitted.

On the other hand, in the reception path, the continuous-time passband signal received is inserted into a low-noise amplifier (LNA) which can be programmed to provide an AGC. Also, in this stage the in phase and in quadrature continuous-time passband signals are recovered using a single-to-differential buffer. After that, the continuous-time passband signals have their spectrum down converted by an analog demodulator, generating two continuous-time baseband signals. Further, the received continuous-time signals are filtered by two lowpass analog filters, improving the selectivity of the receiver. Finally, the two continuous-time passband signals are inserted into the two channel ADC, converting them into discrete-time signals and sent to the FPGA device which will make use of the processor to process them.

5 Performance analyses

This chapter focused on the performance analyses of the NB hybrid PLC/Wireless transceiver prototype. The discussed analyses are driven in terms of Decision Maker block time analysis, PHY layer data-rate analysis, and hardware resource usage analysis. The Decision Maker block time analysis aims to define the $N_{\max}$ value, firstly mentioned in Subsection 3.3.2, taking into account the time constraints imposed by the IEEE 1901.2 Standard. The PHY layer data-rate analysis defines the achievable data-rate of the NB hybrid PLC/Wireless transceiver prototype considering all the available digital modulations. Finally, the hardware resource usage analysis firstly presents the hardware resource usage of the main blocks of the proposed prototype. Later, a comparison in terms of hardware resource usage and power consumption between the NB hybrid PLC/Wireless transceiver and NB PLC transceiver prototype based on the IEEE 1901.2 Standard is presented. Moreover, in order to carry out performance analyses regarding the NB hybrid PLC/Wireless transceiver prototype, we assume that the signal transmission occurs in the frequency covered by the industrial, scientific, and medical (ISM) band for wireless communication (915-915.5 MHz) and the narrowband frequency for PLC (0-500 kHz) because SG and IoT applications require data communication with low power consumption and low-data-rate. It is important to mention that all the parameters mentioned in this chapter and their values are defined in the IEEE 1901.2 Standard.

This chapter is organized as follows: Section 5.1 performs a time-analyze of the Decision Maker block. In sequel, Section 5.2 shows the data-rate of the NB hybrid PLC/ Wireless transceiver prototype. Finally, Section 5.3 provides a hardware resource usage comparison between the NB PLC transceiver prototype and the NB hybrid PLC/Wireless transceiver prototype, both based on the IEEE 1901.2 Standard.

5.1 Decision Maker time analysis

This section aims to analyze the complexity of the Decision Maker block and evaluates which is the maximum number of corrections, $N_{\max}$, that the implementation can support. This analysis takes into account the constraints presented in the IEEE 1901.2 Standard.

In order to perform this analysis, it is important to express the maximum time interval in which the NB hybrid PLC/Wireless transceiver has to decide between sending an ACK or ARQ message. According to the IEEE 1901.2 Standard, it is given by

$$T_{macAckWait} = (T_{RIFS} + T_{CIFS})T_{Sym} + T_{ACK}\ \mu s, \tag{5.1}$$

where T_{RIFS} and T_{CIFS} are RIFS and CIFS time intervals. Note that both time intervals

are equal to 10 T_{Sym}, where T_{Sym} is the time interval of one OFDM symbol and its value is 232 μs, as stated in Table 1. According to (3.1) and adopting N_{PRE} and N_{FCH} equal to 13.5 and 12 symbols, respectively, the T_{ACK} time interval is 5.6595 ms long and, as a consequence,

$$T_{macAckWait} \cong 10.2995\ ms. \tag{5.2}$$

In other words, the NB hybrid PLC/Wireless transceiver must be able to receive, interpret, and correct the erroneous packet in less than 10.2995 ms to agree with the timing constraints associated with the IEEE 1901.2 Standard.

In order to carry out the analysis, the worst case is adopted. The worst case occurs when the longest packet with 1984 bits is received and the Decision Maker block only correct the packet by finding its correct bits combination in its last attempt, see Subsection 3.3.2 for more details. However, the transceiver's processing time interval to receive and interpret the packet, denoted by the variable P_{time}, must be taking into account. Consequently, the remaining time interval, denoted by the variable R_{time}, for the Decision Maker block to perform its task, is given by

$$\begin{aligned} R_{time} &= T_{macAckWait} - P_{time} \\ R_{time} &= 3.8445\ ms. \end{aligned} \tag{5.3}$$

where $T_{macAckWait}$ is given by (5.2) and P_{time} interval is 6.455 ms long and it was acquired in a practical way, using the built-in setup.

Furthermore, Figure 22 shows the time interval demanded by the Decision Maker block to correct erroneous bits. In this plot, 19.2 MHz frequency clock of the PHY layer and another arbitrary clock twice faster generated by a PLL are considered for comparison purpose. As can be seen in these curves, using a 19.2 MHz frequency clock it is possible to correct at most five erroneous bits ($N_{\max} = 5$) without exceeding the time interval ($T_{macAckWait}$) to send the ACK or ARQ message. Moreover, using a clock twice faster, the $N_{\max}$ is increased only by one bit. Analyzing the trade-off between hardware resource usage and $N_{\max}$, we came up with the conclusion that it is not worth using another PLL to generate a twice-faster clock. In other words, being able to correct one more bit is not worth the hardware resource usage increasing, having in mind that there is a limited number of available PLLs in an FPGA device. Furthermore, a data control complexity must be included in order to connect two blocks using different clocks.

5.2 Physical layer data-rate analysis

The first parameter to calculate the data-rate is based on the number of PHY symbols (N_{Sym}) and the number of carriers per symbol ($N_{Carriers}$). We can calculate the

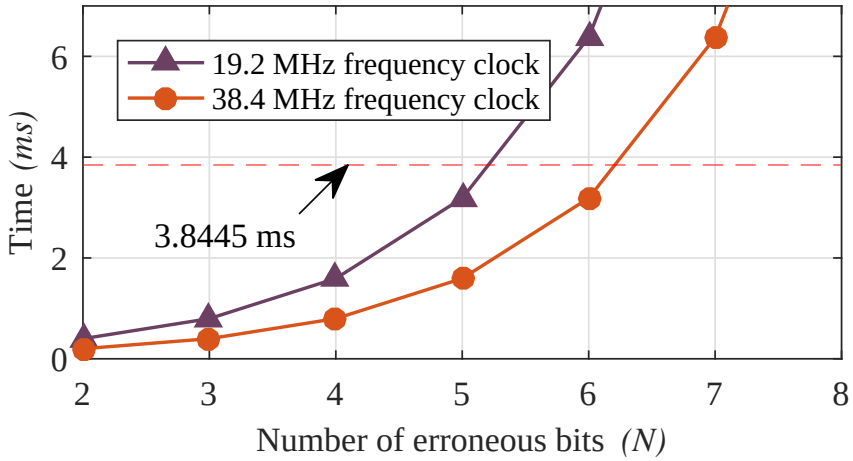


Figure 22: Time interval demanded by the Decision Maker block.

total number of coded bits carried by the whole PHY frame according to the following expression:

$$N_{TotalBits} = N_{Sym} N_{Carriers} N_b, \tag{5.4}$$

where N_b is the number of bits per modulated symbol and is given by $N_b = \log_2(M)$, where M is the constellation size, which is 2, 4, or 8 for BPSK, QPSK, and 8-PSK, respectively. However, we also need to consider the operation mode in this calculation (normal, ROBO, or S-ROBO). Due to that, the number of bits at the output of the CC encoder is expressed by

$$N_{CC} = N_{TotalBits} R_{Mode}, \tag{5.5}$$

where R_{Mode} is the operation mode rate, which can be 1, 1/4, or 1/6 for normal, ROBO, or S-ROBO mode, respectively. Consequently, the number of bytes in the RS encoder output is given by

$$N_{Bytes,RS} = \left\lfloor \frac{(N_{CC} R_{CC} - N_{ZerosTail})}{8} \right\rfloor \tag{5.6}$$

where $R_{CC} = 1/2$ is the convolutional code rate and $N_{ZerosTail} = 6$ is the number of zeros to reset the convolutional encoder state. Also, $\lfloor \cdot \rfloor$ is the floor function which receives a real number and gives as output the greatest integer that is less than or equal to this input real number, which is mathematically defined by $\lfloor x \rfloor \triangleq \max\{m \in \mathbb{Z} \mid m \leq x\}$. Finally, we can obtain the total number of data bits which will be transmitted, L_{Data}, using the following expression:

$$L_{Data} = 8(N_{Bytes,RS} - 2N_{maxSym}) \; bits, \tag{5.7}$$

where N_{maxSym} is the maximum number of correctable symbols by the RS code, which its value can be four for ROBO and S-ROBO, and eight for normal mode.

These L_{Data} information bits are carried within the time interval of a PHY frame, which is calculated by

$$T_{Frame} = \frac{N_{Samples}}{F_S}, \tag{5.8}$$

where F_S is the adopted frequency sample in accordance with the chosen band plan and $N_{Samples}$ is the number of samples in the frame, which is given by

$$N_{Samples} = (N_{Sym} + N_{FCH})(N_{CP} + N_{IDFT} - N_O) + (N_{PRE}N_{IDFT}), \tag{5.9}$$

where N_{FCH}, N_{CP}, N_{IDFT}, N_O, and N_{PRE} are the number of FCH symbols, the number of samples in the cyclic prefix, the length of IDFT, the number of samples overlapped at each side of one symbol due to the windowing process, and the number of preamble symbols, respectively.

Therefore, the data-rate is calculated by

$$R = \frac{L_{Data}}{T_{Frame}}. \tag{5.10}$$

In order to show that the NB hybrid PLC/Wireless transceiver prototype fulfills the IEEE 1901.2 Standard, the data-rate was calculated using the parameters determined by the IEEE 1901.2 Standard, which are $F_S = 1.2$ MHz, $N_{CP} = 30$, $N_O = 8$, $N_{Carriers} = 72$, $N_{IDFT} = 256$, $N_{PRE} = 13.5$, and $N_{FCH} = 12$. Furthermore, the number of data symbols are set to $N_{Sym} = 57$, which is the maximum value respecting the standard constraints. To carry out this analysis, all the available modulations are contemplated. The data-rate achieved by each modulation is presented in Table 5.

Table 5: Data-rates of the NB hybrid PLC/Wireless transceiver.

Modulation	Data-rate (kbps)
S-ROBO (BPSK)	14.4182
ROBO (BPSK)	23.3236
BPSK	101.3517
QPSK	210.3366
8-PSK	318.8974

As can be seen in Table 5, the data-rate increases with the constellation size. The BPSK modulation using ROBO and S-ROBO modes present lower data-rate compared

with the normal mode due to the fact that ROBO and S-ROBO modes are robust forms of the BPSK/DBPSK modulation scheme. In this robust mode, every bit at the output of the convolutional encoder is repeated four or six times, respectively. These two robust modes are commonly used for increasing the data communication reliability over harsh medium. It is worthy to mention that the NB hybrid PLC/Wireless transceiver prototype follows the IEEE 1901.2 Standard, then the aforementioned data-rate are also obtained in practical terms.

Moreover, to achieve the aforementioned data-rates and the proper behavior of the proposed transceiver with respect to the IEEE 1901.2 Standard constraints, the CW and the time intervals, present in Figure 11, must be taken into account. In other words, it means that the proposed transceiver must process (when operating in TX mode) or interpret (when operating in RX mode) a packet in time to keep the transceiver respecting the IEEE 1901.2 Standard's time constraints.

Observing Figure 11, it is easily verified that the shortest time between two consecutive transmission occurs when the proposed transceiver proceeds packet bursting, which means that the second fragment onwards will be transmitted at the CFS window, as stated in Subsection 3.1.3. Consequently, the transceiver must be capable of processing the fragments to be transmitted in a time interval shorter than the sum of the time intervals associated with RIFS, ACK window, and CIFS, see (5.1).

On the other hand, when the proposed transceiver is operating as a receiver, the time interval to process the received packet and send the ACK message, complying with the IEEE 1901.2 Standard, was already calculated in Subsection 5.1 and it is also given by (5.1). Table 6 lists the time interval required for the transceiver to mount and to process the longest packet available by the IEEE 1901.2 Standard (packet with 1984 bits).

Table 6: Operating modes time interval analysis.

Operation mode	Time interval (ms)
TX mode	6.735
RX mode	6.455

As can be seen in Table 6, the time interval taken to mount and process the longest packet allowed by the IEEE 1901.2 Standard, which is the worst case possible, agrees with the time constraints imposed by the IEEE 1901.2 Standard, guaranteeing the proper work of the proposed transceiver.

5.3 Hardware resource usage analysis

A hardware resource usage analysis, using the EP4CE115F29C7 FPGA chip, is another meaningful result to be discussed. This analysis aims to present the hardware

resource usage of each main block implemented. Furthermore, based on this preliminary analysis, a comparison between the NB hybrid PLC/Wireless transceiver prototype and the NB PLC transceiver prototype is presented.

To carry out this analysis, we considered the total number of LEs (which is divided into look-up table (LUT)-Only LEs, Register-Only LEs, and LUT/Register LEs), Memory bits, M9Ks, digital signal processing (DSP) 9×9 elements, DSP 18×18 elements, and the maximum frequency ($f_{\max}$). Moreover, a power consumption analysis is also considered.

Before proceeding to the analysis, the aspects aforementioned must be addressed for a better understanding of the results. LEs are the smallest units of logic in the Cyclone IV device architecture [75]. Each LE is mainly composed of a four-input LUT which can implement any function of four variables and a programmable register. In order to fulfill each logic requirement, the LE can use only the LUT, only the register, or use both LUT and register. The combination of many LEs enable any logic to be implemented. Another hardware resource aspect is the memory bits. They are used to implement memories, such as random-access memory (RAM), read-only memory (ROM), firts-in first-out (FIFO) memory and the combination of 8192 memory bits constitute a M9Ks block. Embedded multipliers are dedicated blocks specialized in performing multiplication operations, reducing hardware resource usage, and lowering the power consumption. A embedded multiplier is configured as either one 18×18 multiplier or two 9×9 multipliers. Finally, the $f_{\max}$ is the maximum frequency that the clock can achieve. In this analysis, only the 19.2 MHz frequency clock of the PHY layer, MAC sublayer, and Decision Maker block will be analyzed, having in mind that this is the most critical one. The criticality of a clock is related with the number of instructions in parallel that it must execute at the same cycle. Additionally, a power consumption analysis is also provided, which consists of an estimation of the FPGA power consumption to perform the implemented logic.

The number of used LE, Memory bits, M9Ks blocks, DSP 9x9 elements, and DSP 18x18 elements per block are summarized in Table 7. It is important to mention that the MAC sublayer comprehends also the M2P, P2M, and PHY parameters memories.

Observing Table 7, we can see that PHY TX and PHY RX are the most expensive blocks in terms of hardware resource usage. It can be easily explained because the whole IEEE 1901.2 PHY layer is implemented in these two blocks. The synchronism block, which its procedure is not specified in the IEEE 1901.2 Standard, uses a considerable amount of hardware resources due to its complex math. The Hilbert transform spends a small amount of hardware resources compared with the aforementioned blocks, having in mind that it is mainly composed of only one digital filter.

Moreover, the MAC sublayer consumes a considerable amount of memory although does not need many LE elements. It is only possible because the MAC sublayer is implemented using the Nios II processor, which enables us to choose the best set of resources

Table 7: Hardware resource usage per block.

Block	LE				Memory bits	M9Ks	DSP 9×9	DSP 18×18
	LUT-Only LEs	Register-Only LEs	LUT/Register LEs	Total LE				
Hilbert transform	833	315	765	1913	60	1	0	0
Synchronism	2971	671	1853	5495	290634	52	0	27
RX IEEE 1901.2	7624	2792	7556	17972	146232	55	0	20
TX IEEE 1901.2	4910	2007	5523	12440	676800	114	0	12
Decision Maker	170	104	205	479	3968	2	0	0
P-AFE	88	84	154	326	0	0	0	0
W-AFE	232	82	275	589	0	30	0	0
MAC sublayer	6140	2002	5778	13920	990726	152	0	29

to fulfill our needs.

The number of used LE, memory bits, M9Ks blocks, DSP 9×9 elements, DSP 18×18 elements, $f_{\max}$, and power consumption are summarized in Table 8 for NB PLC transceiver and NB hybrid PLC/Wireless transceiver prototypes. Note that the prototype of NB PLC transceiver based on the IEEE 1901.2 Standard is composed of a MAC sublayer, synchronism, PHY TX IEEE 1901.2, PHY RX IEEE 1901.2, and a P-AFE blocks. On the other hand, besides the aforementioned blocks, the NB hybrid PLC/Wireless transceiver prototype is also composed of the Hilbert transform, the Decision Maker block, a second PHY RX IEEE 1901.2, and a W-AFE. The ρ column of Table 8 is the relative hardware resource usage increase, where ρ is given by

$$\rho = \frac{C_b}{C_a} - 1, \tag{5.11}$$

where C_b and C_a are the hardware resource of the NB hybrid PLC/Wireless transceiver prototype and NB PLC transceiver prototype, respectively. It can be seen that to implement the NB hybrid PLC/Wireless transceiver prototype, we do not need to double the NB PLC transceiver prototype resources. This occurs due to the fact that only the receiver needs to be duplicated as mentioned before, having in mind that the transmitter is exactly the same for both PLC and wireless data communication. Furthermore, a few receiver blocks can be shared by both PLC and wireless receiver parts, saving, even more, hardware resources. Regarding the $f_{\max}$ analysis, both prototypes presented a maximum clock frequency greater than the minimum required of 19.2 MHz. Another interesting result is the power consumption analysis. As can be seen, the NB hybrid PLC/Wireless transceiver prototype spends only a small fraction of energy more than the NB PLC transceiver prototype.

Table 8: Hardware resource usage for NB PLC and NB hybrid PLC/Wireless transceiver prototypes.

Hardware resource		PLC	PLC-Wireless	ρ
LE	LUT-Only LEs	22566	34396	0.524
	Register-Only LEs	7871	11835	0.503
	LUT/Register LEs	21629	32283	0.492
	Total LE	52066	78514	0.508
Memory		2104452	2545346	0.209
M9Ks		374	514	0.374
DSP 9×9		0	0	-
DSP 18×18		88	135	0.534
$f_{\max}$ (MHz)		19.68	19.67	-0.005
Power consumption (mW)		311.92	348.4	0.117

6 Conclusions

Due to the fast growth of SGs and IoT, the necessity of introducing data communication technologies that enable their widespread deployments is being recognized as a timely and challenging research problem. Solutions based on PLC and wireless communication technologies are strong candidates to fulfill this necessities, specially when low cost and low installation complexity come to matter. In this regard, this thesis have presented a NB hybrid PLC/Wireless transceiver prototype, which jointly uses parallel power line and wireless channels for low-data-rate communication, aiming to fulfill the data communication demands related to SG and IoT.

Chapter 2 have formulated the problem discussed in this thesis. It is concluded that one of the most important aspects to prototype a hybrid transceiver concerns the standard to be used in each medium and the necessary adaptations to overtake possible limitations. It has been concluded that the best choice concerning the approach to be adopted is to use a PLC standard and extend it to be used in the wireless medium. Among PLC standards and based on the presented promises, the IEEE 1901.2 Standard showed up as the most promising standard.

Chapter 3 has discussed the block diagram of the proposed NB hybrid PLC/ Wireless transceiver, describing their functionalities and importance. Furthermore, it has discussed the adaptation necessary to enable the proper operation of a hybrid transceiver, which is based on the use of the Hilbert transform. This transform allows the recovery of the quadrature information from the received signal, allowing to estimate and correct the frequency deviation between the transmitter and receiver's clock. Moreover, some enhancements are proposed, which are the routing between nodes and the Decision Maker block. The routing between nodes process enhanced the transceiver enabling every node to work as a relay node, rising system coverage and reliability. Another remarkable enhancement was provided by the Decision Maker block, which reduces the necessity of ARQ messages and, consequently, increasing the data network throughput.

Chapter 4 has overviewed the NB hybrid PLC/Wireless transceiver prototype, by discussing the IEEE 1901.2 Standard PHY layer implementation using an FPGA device. The implementation has focused on the blocks used in the transmitter and receiver, highlighting their importance. Also it has presented details about the implementation, such as bus length between blocks and data control standard adopted. Finally, this chapter has addressed the components which comprehend the prototype, describing their main features and functionalities.

Chapter 5 has focused on performance analyses of the NB hybrid PLC/Wireless transceiver prototype. Regarding the Decision Maker block time analysis, it is shown that it is not worth rising the PHY layer clock frequency in order to be able to correct

a great number of bits. According to this analysis, doubling the clock frequency would allow only one more bit correction at the cost of rising the computational complexity by adding another PLL. Concerning the data-rate analysis of the NB hybrid PLC/Wireless transceiver prototype, it can be seen that it varies from a few tens of kbps using S-ROBO, which is a very robust mode, up to a few hundred of kbps. These data-rates can perfectly satisfy the needs of SG and IoT applications. Finally, regarding the results using an FPGA device, the hardware resource usage of the NB PLC and NB hybrid PLC/Wireless transceiver prototypes are compared. Based on the results, it could be verified that even being capable of supporting data communication in PLC and wireless media, the hardware resource usage and power consumption of the FPGA device by the NB hybrid PLC/ Wireless transceiver is less than twice the hardware resource usage and power consumption of the NB PLC transceiver, which supports data communication from only one medium (PLC). Therefore, saving hardware resource, the power consumption decays too. It is a reasonable result, having in mind that the NB hybrid PLC/Wireless transceiver was implemented aiming to increase performance and save hardware resources, always sharing the processing blocks between the PLC and wireless media when possible.

6.1 Future works

A list of future works are as follows:

- To test the NB hybrid PLC/Wireless transceiver prototype in the field, facing more realistic and variety situations. These conditions will enable to validate specially the routing between nodes process when using a network of transceivers. Furthermore, this test will enable to adjust several MAC sublayer parameters in order to enhance the transceiver's performance.
- To verify under which channel conditions the Decision Maker block can provide a maximum and a minimum performance.
- To improve AFE interface blocks, making them able to automatically reconfigure the AFEs to adapt to current channel conditions. Although, firstly, the P-AFE and W-AFE's behavior in several channel conditions must be study.

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Appendix A – Publications

The list of journal papers under review and published during the graduate period is as follows:

- DA COSTA, VINÍCIUS LAGROTA R.; SCHETTINO, HUGO VIVEIROS; CAMPONOGARA, ÂNDREI; DE CAMPOS, FABRÍCIO P.V.; RIBEIRO, MOISÉS VIDAL. "Digital filters for clustered-OFDM-based PLC systems: Design and implementation". *Digital Signal Processing*, v. 70, p. 166-177, 2017.
- COSTA, LUIS GUILHERME DA SILVA; DE QUEIROZ, ANTÔNIO CARLOS MOREIRÃO; ADEBISI, BAMIDELE; DA COSTA, VINICIUS LAGROTA RODRIGUES; RIBEIRO, MOISÉS VIDAL. "Coupling for Power Line Communications: A Survey". *Journal of Communication and Information Systems (JCIS)*, v. 32, p. 8-22, 2017.

The list of conference papers published during the graduate period is as follows:

- COSTA, V. L. R.; MIRANDA, C. R.; SOUZA, S. A.; MARTINS, C. H. N.; CAMPOS, F. P. V.; OLIVEIRA, T. R.; RIBEIRO, M. V. "Front-End Analógico para Power Line Communication na faixa entre 1.7 e 50 MHz". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.
- COSTA, L. G. S.; PICORONE, A. A. M.; COSTA, V. L. R.; RIBEIRO, M. V. "Projeto e Caracterização de Acopladores para Power Line Communication". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.
- COSTA, L. G. S.; PICORONE, A. A. M.; QUEIROZ, A. C. M.; COSTA, V. L. R.; RIBEIRO, M. V. "Caracterização da Impedância de Acesso à Rede de Energia Elétrica Residencial para Uso em Sistemas Power Line Communications". In: *XXXIII Simpósio Brasileiro de Telecomunicações*, 2015, Juiz de Fora. SBrT, 2015.